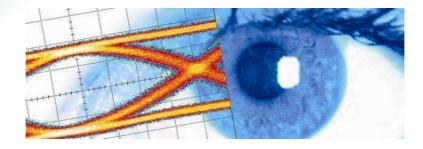


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Application Note

SHF Pattern Generator Skew Control



A skew control function helps to simplify all test and measurement arrangements involving multiple lanes of data signals such as multi-port modules or higher order modulation formats such as DQPSK, DP-QPSK or QAM, where precise control of relative signal delay is critical.

The relative delay (or skew) between two or more signal lanes becomes a very important factor in high speed communication as soon as independent transmitted binary signals are combined to higher order signals while keeping the symbol rate.

This application note describes how the alignment of the output signals from the Pattern Generator SHF 12103A could be adjusted greatly over many bit periods (integer bit delay) and fine-tuned within tenth of a picoseconds (skew control).

Integer bit delay

The SHF 12103A Bit Pattern Generator could be equipped with a variety of different output channel combinations. Each of these outputs can transmit its own individual pattern sequences (either PRBS or user defined patterns).

In case two or more channels of the same speed are transmitting patterns of the same length it is possible to define how these patterns are aligned with respect to each other. In other words, the first bit of pattern sequence B can be transmitted a defined number of bits after the first bit of pattern sequence A. This defined number of bits is called bit delay at the SHF 12103A Pattern Generator.

Such a definition is only possible for pattern of the same length since the alignment of different sized patterns will change every time a full pattern cycle is transmitted.

The pattern selection menu of the graphical user interface, the SHF BERT Control Canter (BCC), is shown below.

Pattern Generation Mode 🔘 100Gbps 🔘 2x56 Gbps 💿 4x32Gbps							
	Channel A	Channel C	Channel B	Channel D			
Pattern	PRBS 2^31 - 1 💌						
Invert	V	v	v	V			
Error Inj.	Off 💌	Off 🔻	Off 💌	10E-10 🔻			
Bit Delay	0	0	6	12578			
	DQPSK	(Precoding AxC	DQPSK I	Precoding BxD			
User Pattern: No user pattern uploaded							

Figure 1: Pattern Control of the SHF 12103A GUI

Once two or more of the chosen pattern sequences are of the same length the bit delay adjustment function is enabled. By the above settings the patterns from channel A and C will be transmitted simultaneously, i.e. the BPG will send the same bits at the same time. Channel B and D are shifted by 6 or 12578 bits, respectively.

The maximum number of the bit delay is only restricted by the word length of the transmitted patterns.

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In addition to the above described logical or coarse function of bit delay, it is also possible to define and perform a fine timing delay between two transmitted signals in the sub-rate output channels; the so called skew. This skew might be only a small fraction of the bit length.

All SHF Pattern Generators are optimized to provide the lowest possible skew between the different output channels. However, even a perfectly balanced Pattern Generator could not compensate for any mis-alignment caused by cables or other interconnecting modules. Therefore SHF introduced a more accurate and flexible method to adjust and modify the skew between the transmitted signals: the option SC (Skew Control).

This optional feature of the SHF 12103A Bit Pattern Generator enables control of the skew of each of the individual sub-rate outputs relative to one another.

2x56Gbps Outputs			4x32Gbps Outputs	
2x56Gbps Duty Cycle Adj.		4x32Gbps Duty Cycle Adj.		4x32Gbps Skew Adj.
Skew Adjust	Channel A 0.0 + 44 4 b bb	Channel C	Channel B	

Figure 2: Output Signal Control of the SHF 12103A GUI

Figure 3 shows the outputs signal control menu of the graphical user interface, the SHF BERT Control Center (BCC), from the SHF 12103A pattern generator. The skew could be modified with a resolution of 0.1 ps within a maximum skew difference of 50 ps (\pm 25 ps from zero position) between two channels.

The usefulness of this skew control function is exemplified through the generation of a 4-level signal from two binary data streams. In Figure 3 a four-level signals is created by combining two 20 Gbps binary signals with a passive combiner. The left eye diagram is distorted due to a small timing misalignment caused by the pattern generator, the cables and the power combiner. The right diagram was taken after balancing this timing mis-alignment by a few clicks in the BCC software control.

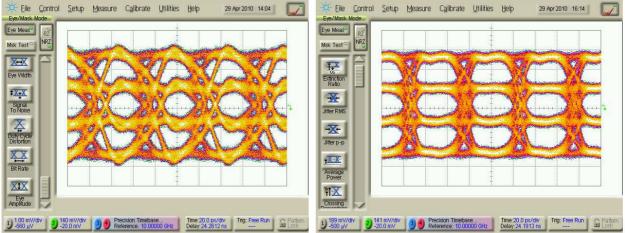


Figure 3: 20 Gbps four level signals

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The 50 ps total skew adjustment range equals full bit length at 20 Gbps. This means for signals with a bit rate \ge 20 Gbps any possible shift between two signals could be achieved (together with the integer bit delay).

Figure 4 below shows possible delay settings by utilizing a combination of the skew control function and / or the integer bit delay.

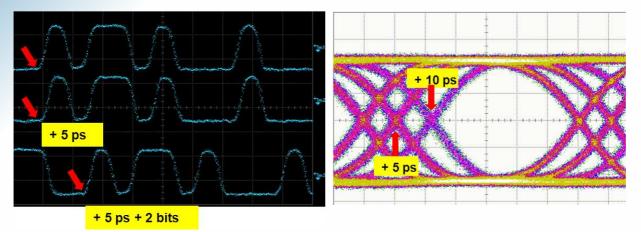


Figure 4: Shifted output signals of the SHF 12103A subrate outputs

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