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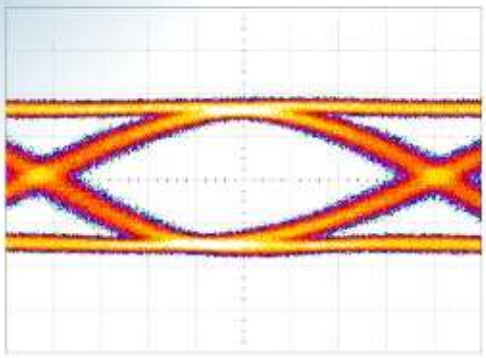

# Application Note

# DQPSK

## Bit Error Test Solution

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# Introduction

DQPSK modulation, in spite of its implementation complexity compared to Amplitude Shift Keying (ASK), has become increasingly important for high speed transmission because of its efficiency and its robustness against dispersion and non-linear effects.

This application note is intended to provide a general overview of the optical DQPSK functionalities including its mathematical basics, the generic structure of the SHF DQPSK optical transmitter and receiver modules and the application of these modules in combination with SHF's 50G electrical bit pattern generator (BPG) and error analyser (EA). A proprietary software module (DQPSK Editor) has been developed to enable the user to predict the corresponding demodulated bit sequence for BER measurements. This software is fully integrated into the SHF BERT Control Center (BCC) software.

# DQPSK Theory

Differential Quadrature Phase Shift Keying (DQPSK) is a four-level modulation format. Two orthogonal phases of the same optical carrier are used to double the spectral efficiency by transmitting two bits at a time. This is done by converting two incoming electrical data streams into a four phase optical data signal.

A typical DQPSK transmission scheme is shown in figure 1. The incoming data streams *u, v* are pre-coded according to the algorithm described below and sent to the DQPSK transmitter. After transmission the DQPSK receiver de-correlates the phase-shifted signal to the output signals *r, s* which should be equivalent to the incoming *u, v*.


**Figure 1: Typical DQPSK transmission system configuration**

## Transmitting DQPSK Optical Data

A DQPSK optical transmitter converts two incoming electrical data streams into a four phase optical data signal. Different implementations are:

- A phase modulator (PM),
- A Mach-Zehnder modulator and a phase modulator (MZ-PM) or
- Two parallel Mach-Zehnder modulators in a nested structure (dual MZM) plus an integrated quadrature phase element.

The implementation of SHF optical DQPSK transmitters is based on the dual MZM approach. Details of other DQPSK implementations can be found in reference [1].

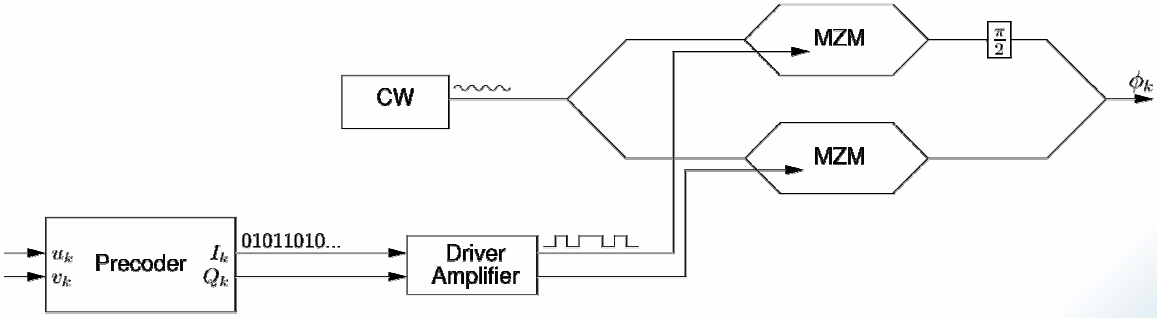


**Figure 2: Pre-coder and dual Mach Zehnder modulator.**

Figure 2 shows the driving principle of the nested modulator structure. The electrical data streams *u* and *v* are converted into the *I* and *Q* channel by pre-coding. One modulator within the nested structure is driven by the I and one by the Q channel. The incoming CW laser light is split and equally distributed in the two modulators. The signals on the individual channels modulate the CW light in the following way:

- The I and Q signal generate a phase shift of 0 or π in each modulator,
- One arm of the nested structure is further phase shifted by π/2,
- The addition of both optical signals results in one out of four phase shifted symbols: π/4, 3 π /4, 5 π /4, or 7 π /4.

The optical signal at the output of the nested modulator structure is now DQPSK modulated and carries one symbol at the same speed as one of the electrical input signals. Each symbol comprises the information of two bits; one from the I and one from the Q channel. The following equation is a mathematical analogy for the dual MZ modulator.

$$E(t_k) = E_0 \cdot \cos\left[\frac{\pi\cdot(I_k - Q_k)+\frac{\pi}{2}}{2}\right] \cdot e^{j\left(\frac{\pi\cdot(I_k+Q_k)+\frac{\pi}{2}}{2}\right)} \quad (1)$$

Due to the binary control of the modulator, the resulting phase can be determined using a simplified correlation:

| $I_k$ | $Q_k$ | $E(t_k)$ | $\phi_k$ |
|---|---|---|---|
| 0 | 0 | $\cos\left(\frac{\pi}{4}\right)\cdot e^{j\frac{\pi}{4}} \approx e^{j\frac{\pi}{4}}$ | $\frac{\pi}{4}$ |
| 0 | 1 | $\cos\left(-\frac{\pi}{4}\right)\cdot e^{j\frac{3}{4}\pi} \approx e^{j\frac{3}{4}\pi}$ | $\frac{3}{4}\pi$ |
| 1 | 0 | $\cos\left(\frac{3}{4}\pi\right)\cdot e^{j\frac{3}{4}\pi} \approx e^{j\frac{7}{4}\pi}$ | $\frac{7}{4}\pi$ |
| 1 | 1 | $\cos\left(\frac{\pi}{4}\right)\cdot e^{j\frac{5}{4}\pi} \approx e^{j\frac{5}{4}\pi}$ | $\frac{5}{4}\pi$ |

## Receiving DQPSK Optical Data

Receiving of optically transmitted data using ASK is done by using a single photodiode. The demodulation of DQPSK signals more complex. For detecting the phase change which is imposed onto the optical carrier a dual Mach-Zehnder Interferometer is used to convert the phase changes to electrical signals. This interferometer consists of two DBPSK① one symbol delay demodulators with the phase offset of ± π/4 (an exemplary structure is shown in figure 3). Thus, a DQPSK receiver can be seen as two bit-synchronized DPSK receivers; one for each of the two DQPSK channels.

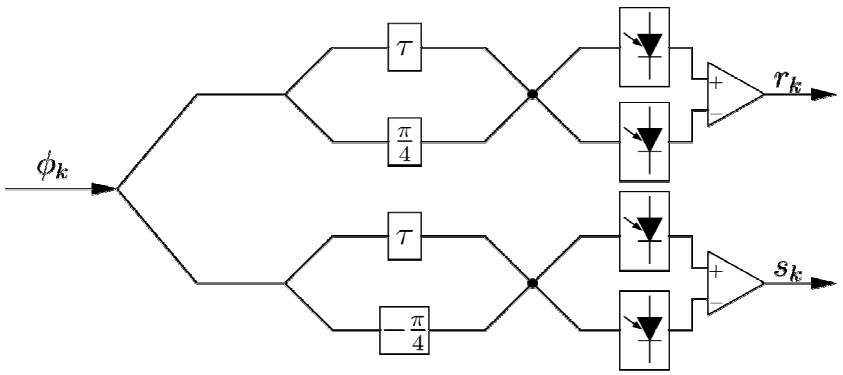


**Figure 3: DQPSK demodulator structure (according to [1]).**

The incoming light $\phi_k$ is split into two arms with two sub-paths each. In each arm the upper path is delayed by the transmission time of one symbol. The lower path is phase shifted by +π/4 or - π/4 respectively. When re-combining the two paths, constructive and destructive path, interferences occur. For optical-electrical signal conversion simple photodiodes can be used. The superposition

① Dual Binary Phase Shift Keying, for further information see [1].

of the sub-paths causes an interrelation between consecutive symbols; thus DQPSK demodulation is no longer bit transparent. To ensure that the received data is equal to the transmitted data the usage of a pre-coder is necessary (see section DQPSK Pre-coder below).

The mathematical definition of DQPSK demodulator's balanced receiver is, according to figure 3 and [1]:

$$r(t_k) = -R\frac{E_0^2}{2} \cdot [\cos(\Delta\phi_k) - \ sin(\Delta\phi_k)] \quad (2)$$

$$s(t_k) = -R\frac{E_0^2}{2} \cdot [\cos(\Delta\phi_k) + \ sin(\Delta\phi_k)] \quad (3)$$

with $\Delta\phi_k = \phi(t_k) - \phi(t_{k-1})$ as the phase difference between two consecutive symbols and R as photodiode responsivity. Again, a simple tabular correlation is obvious:

| $\Delta\phi_k$ | $r_k$ | $s_k$ |
|---|---|---|
| $0$ | $-1$ | $-1$ |
| $\frac{1}{2}\pi$ | $+1$ | $-1$ |
| $\pi$ | $+1$ | $+1$ |
| $\frac{3}{2}\pi$ | $-1$ | $+1$ |

## Pre-coding DQPSK signals

Due to the correlation of consecutive symbols done by the DQPSK demodulator a pre-coder is necessary to receive exactly the data that has been transmitted. This requires a recursive pre-coder structure as shown in figure 4. While this is unproblematic for serial implementations of DQPSK pre-coders parallel implementations (which are necessary for a contemporary transmission rates) require some more considerations in regard to the implementation's structure.

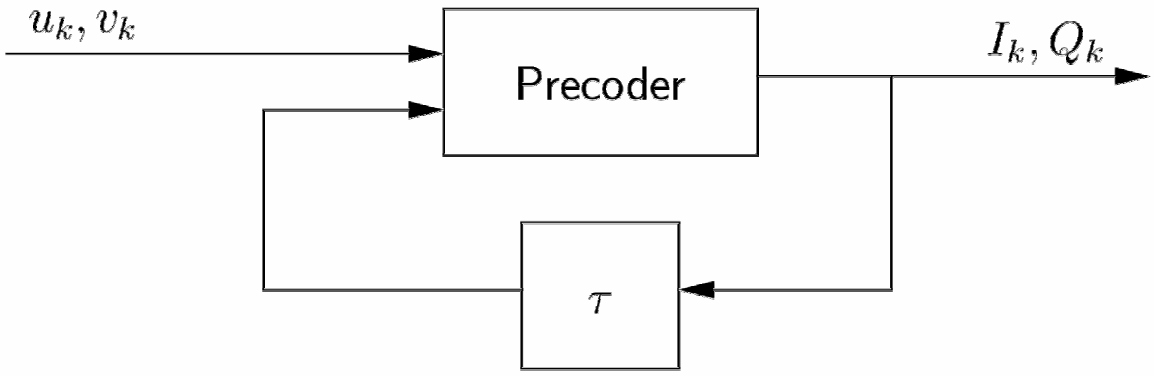


**Figure 4: Generic DQPSK pre-coder structure.**

In theory (serial) pre-coding is not that difficult (as described by the equations 4 and 5).

$$I_k = \overline{(u_k \oplus v_k)} \cdot (u_k \oplus I_{k-1}) + (u_k \oplus v_k) \cdot (v_k \oplus Q_{k-1}) \quad (4)$$

$$Q_k = \overline{(u_k \oplus v_k)} \cdot (v_k \oplus Q_{k-1}) + (u_k \oplus v_k) \cdot (u_k \oplus I_{k-1}) \quad (5)$$

Practical implementation of a DPSK pre-coder for speeds up to 40 Gbps are feasible but higher speed capable implementations require parallel structures for reaching transfer rates of 100 Gbps [11].

# Solutions for DQPSK system research

## DQPSK Optical Transmitter

SHF offers two optical DQPSK transmitter for transmission speeds of up to 40 Gbps (SHF 46213A) and up to 100 Gbps (SHF 46214A). Both are designed as plug-in modules to be hosted by the mainframe SHF 10000B or SHF 10001A.

In both transmitter modules a dual MZ modulator with an integrated phase modulator (operating at DC) to set the quadrature phase is used for the E/O conversion. The DC bias of the two data MZMs within the parallel structure is automatically controlled to provide a proper and stable DPSK modulation in both arms of the nested modulator structure. For fine tuning manual DC bias is also allowed. The quadrature phase is set manually through a DC bias via the control software.

The SHF 46214A is for NRZ modulation only, whereas the SHF 41213A supports NRZ, 33% FWHM RZ and 67% FWHM CS-RZ modulation formats.

Detailed information of these instruments is available in the according datasheets (SHF 46213A [2], SHF 46214A [3]).

## DQPSK/DPSK Optical Receiver

To enable the reception of the DQPSK optical signals up to 100 Gbps SHF can provide several DPSK receivers operating at bit rates of up to 10, 20, 40, and 50 Gbps. With these plug-in modules② receiving, demodulation and conversion into an electrical signal of one selectable D(Q)PSK channel (I or Q) is supported. Demodulation is realized by adjusting the optical phase delay within the one-bit delay MZ interferometer to select either the I or Q channel. Thus tests for optical DQPSK transmission can be performed very efficiently.

For more information about the SHF DPSK receivers please refer to the appropriate data sheets (SHF 47210A [4], SHF 47211A [5], SHF 47213A [6], SHF 47214A [7]).

## Bit Error Analysis for DQPSK transmission

To complete the DQPSK test and measurement suite an SHF bit pattern generator (BPG) and the corresponding error analyzer (EA) should be used. Figure 5 shows such a sample test configuration.

The BPG (SHF 12100B) provides a high speed differential output of up to 56 Gbps③. In addition, sub-rate outputs to support other applications such as high speed multiplexer testing are available as an option. True PRBS sequences at several pattern lengths④ or user-patterns of up to 128 Mbit can be generated. The EA (SHF 11100B) is used to perform the bit error ratio analysis of the incoming data from the D(Q)PSK receiver. It operates at the same transmission (sub-)rates as the BPG and supports bit error analysis in real-time for PRBS and computer based user patterns. The entire system is controlled by the Bert Control Center (BCC) software package. The BCC enables easy and efficient controlling of all available SHF plug-in modules from one platform and offers advanced measurement utilities apart from simple control capabilities. To help our customers for BER analysis for DQPSK transmission, an integrated DQPSK coding software is provided. This software tool supports the following applications:

a) **pre-coding** the output data streams (only when using the BPG sub-rates) and

b) generation of the expected data received by the DQPSK demodulator (**decoding**).

② available for the mainframe type SHF 10000B or SHF 10001A
③ full channel sub rates up to 28 Gbps
④ currently supported PRBS patterns: $2^7$-1, $2^9$-1, $2^{11}$-1, $2^{15}$-1, $2^{20}$-1, $2^{23}$-1, and $2^{31}$-1

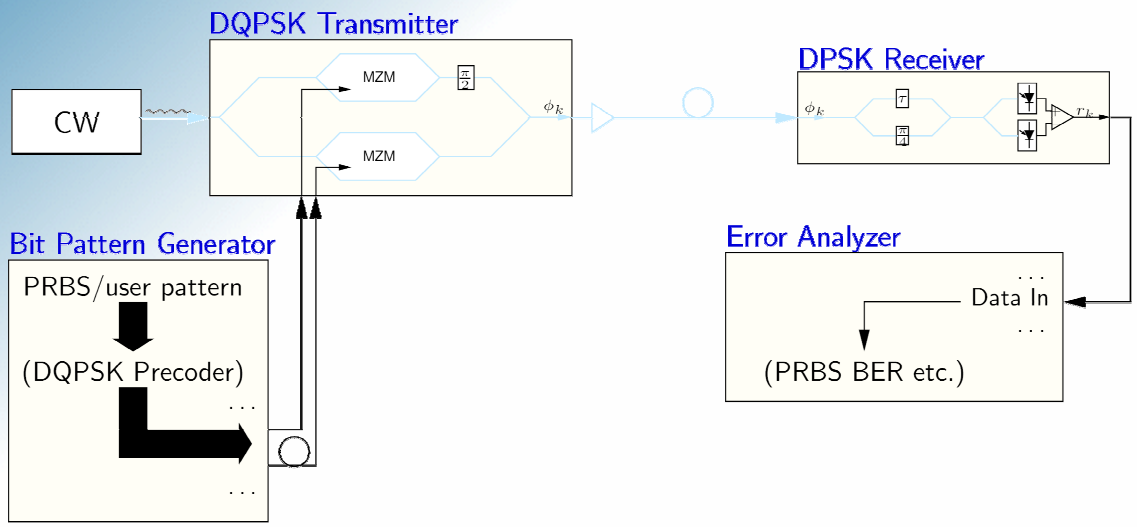


**Figure 5: DQPSK transmission test with BPG, DQPSK transmitter and receiver, and EA.**

## DQPSK Editor

Although in theory it is possible to implement a hardware pre-coder for this purpose the most convenient and flexible approach for transmission studies is to predict the demodulated bit sequence for BER measurements. For this purpose SHF has developed a software coding module integrated into the BCC control software which controls the operation of the SHF BERT system plug-in modules.

Two different approaches are implemented.

**Decoding:**
The DQPSK Editor software allows to use PRBS or user pattern sequences from the BPG and predicts the expected bit sequence after demodulation by the D(Q)PSK receiver. This scenario is most common in the laboratories as the only requirement is a differential high speed data signal and an error analyzer (detector) which can handle an arbitrary user pattern with sufficient memory size.

**Pre-coding:**
This mode of operation is only possible in conjunction with the sub-rate outputs and user pattern generation of the SHF BPG. It allows the user to run the error analyzer under PRBS mode and the DQPSK Editor predicts the required user pattern to be generated at the BPG and applied to the sub-rate outputs. The maximum system symbol rate is limited to the maximum bit rate of the sub-rate channels (which is 28 Gbps).

The following two sections provide specific examples for BER measurements based on decoding and pre-coding in typical laboratory DQPSK transmission system experiments.

## Optical Transmitter and Receiver Setup

Before starting BER measurements a proper setup of the DQPSK transmitter and DPSK receiver is required. It is recommended that the automatic modulator DC bias function in the DQPSK transmitter is enabled for both MZMs. In the DQPSK transmitter's settings window (DQPSK-TX), the drivers for data A and B can be turned on or off individually as shown in figure 6. With one channel switched off the transmitter works in DPSK mode. Operating the DQPSK transmitter in this mode while demodulating the signal with a DPSK receiver and displaying the pulse train of the demodulated signal on a suitable high speed oscilloscope will enable to determine the electrical differential delay between the two modulated data channels. This information will be needed for setting up the DQPSK Editor for decoding or pre-coding operations.

For DQPSK operation both drivers need to be enabled. Automatic DC bias settings for the data channels should be sufficient for most experiments. The best approach to ascertain that the quadrature phase bias is correctly set, is to detect the DQPSK signal with a high speed optical detector first followed by using the DPSK receiver for fine tuning.

Figure 7 shows the directly detected eye patterns when the quadrature phase modulator is correctly biased to 90° or not. If required, the qu adrature phase can be set by adjusting the phase modulator DC bias voltage via the transmitter's BCC control window. Figure 8 shows the demodulated signal with optimum quadrature phase modulation at the transmitter.

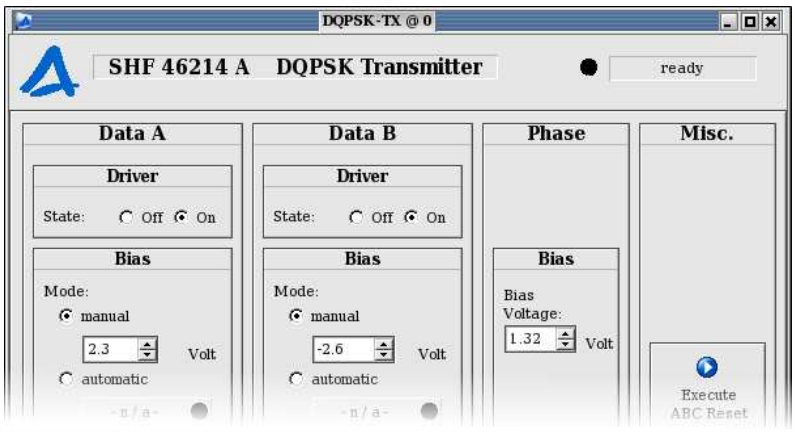


**Figure 6: DQPSK transmitter control**

Non-optimum 90° phase

Optimum 90° phase setting

**Figure 7: Transmitter quadrature phase bias for DQPSK modulation**

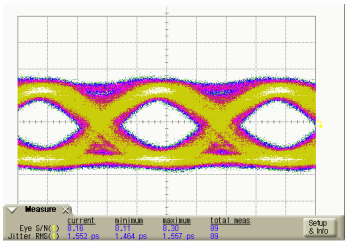

**Figure 8: Demodulated signal with optimum quadrature phase setting**

By adjusting the heater power control in the SHF DPSK receiver it is possible to rotate the phase sequentially to demodulate the I, Q, then /I and /Q channels for testing. Figure 9 shows the BCC control window of the 50 Gbps DPSK receiver SHF 47214A.

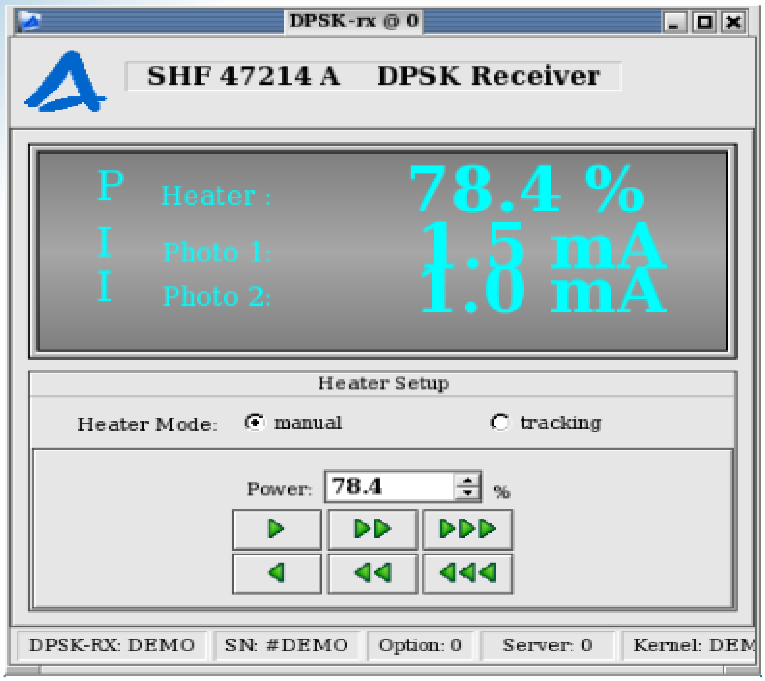


**Figure 9: BCC control window of the SHF optical DPSK receiver**

Before measuring BER for DQPSK transmitted signals it should be verified that the DPSK transmission (either channel A or B in the transmitter) works error free.

## DQPSK Decoder functionality

This example covers the most common DQPSK system testing in R&D: Using the differential BPG outputs Data and /Data with PRBS or user data, feeding these signals into a DQPSK transmitter and receiving either the I or the Q channel by a DPSK receiver. The BER of the selected and demodulated DQPSK channel can be measured with the EA in user pattern or user real time mode. The DQPSK Editor implemented in the BCC software provides the interface for creating the pattern which is expected to be detected by the EA.

In the example below the BPG is set to PRBS $2^{9-1}$; therefore the DQPSK editor's Data1 and Data2 should both be loaded to PRBS $2^{9-1}$ and in addition Data2 has to be inverted.

The DQPSK Editor window can be opened via the Module menu of the BCC by selecting the DQPSK Editor. In the DQPSK Editor the “DQPSK Decoder” tab has to be chosen. Clicking on “Load Data1” pops up the pattern select dialog (figure 10). Select PRBS $2^{9-1}$ ⑤ and repeat for Data2.

⑤ PRBS or user patterns can be selected with the BPG's/EA's memory limitations in mind

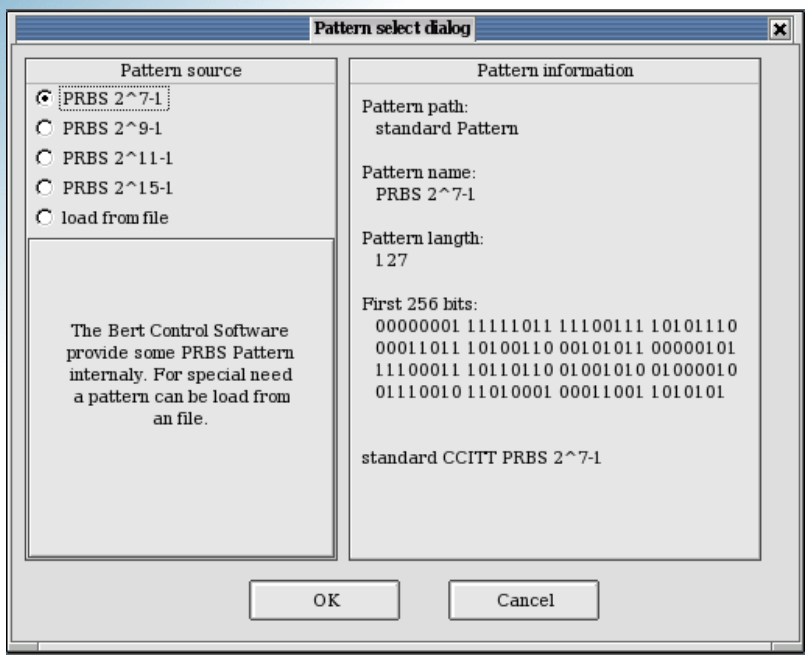


**Figure 10: DQPSK Editor's Pattern select dialog**

To invert the Data2 path the invert checkbox near the Data2 arrow in the main DQPSK Editor window has to be activated. The necessary decorrelation between the Data and \Data channel can be achieved by connecting the BPG to the DQPSK Tx by two RF cables of different length. The resulting differential bit delay has to be put into the “relative Bit delay” box (2 bit in the example below). Fitting delay matched cables with an extreme accurate delay accuracy are also available at SHF.

The channel I or Q to be BER measured by the EA can be selected in the dotted DQPSK RX box (here channel Q).

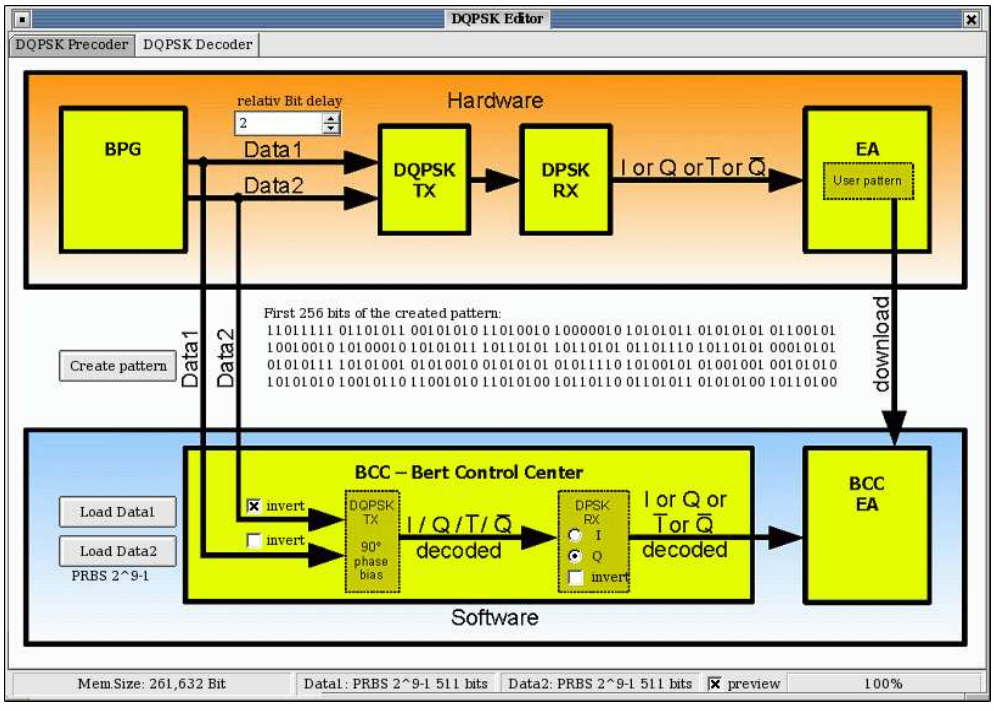


**Figure 11: DQPSK Editor's DQPSK Decoder tab**

A final click on “Create pattern” starts the pattern generation and opens the created DQPSK decoded pattern in the Pattern editor.

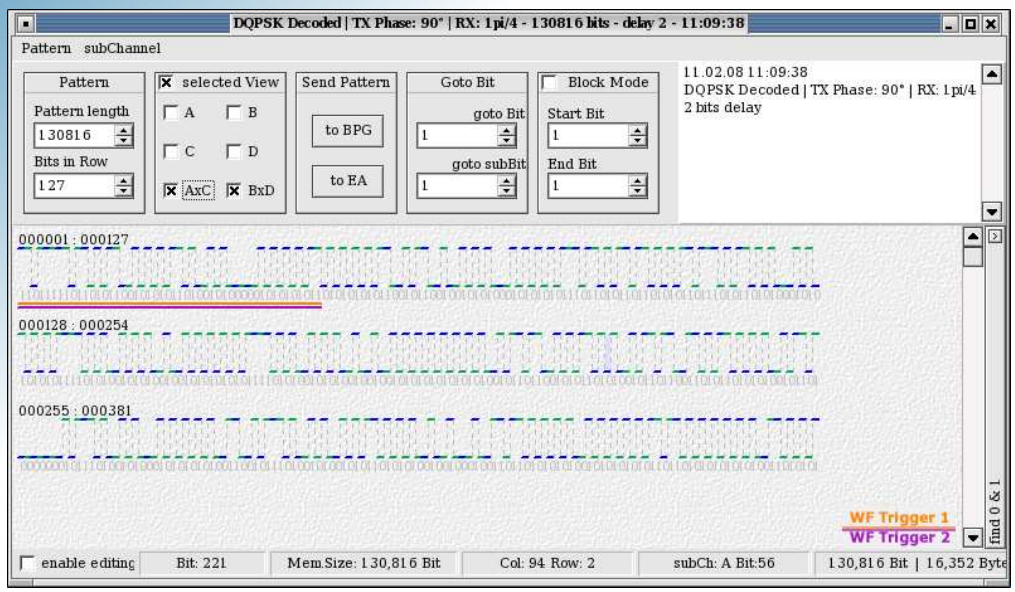


**Figure 12: Pattern Editor**

## Setup of Pattern Generator and Error Analyzer

The Pattern Editor's “Send Pattern to EA” button opens a file save dialog requesting a filename for the current pattern. When the name is entered the pattern is automatically loaded into the EA. If the BPG’s high speed outputs are being used the bit rate of BPG and EA has to be set to the same value.

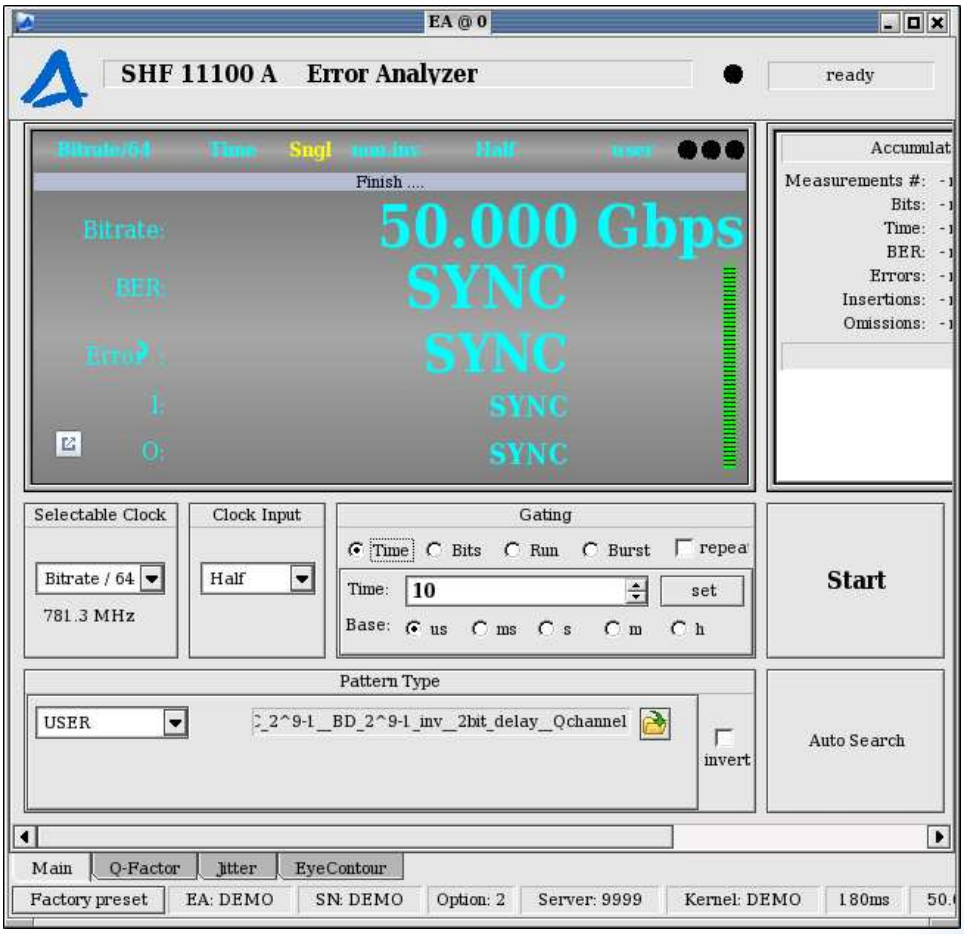


**Figure 13: Error Analyzer's graphical representation (User Pattern mode)**

Finally, the BPG has to be set to the appropriate bit rate and PRBS sequence:


**Figure 14: BPG's graphical representation (PRBS mode)**

Now all instruments should be set up correctly and the BER measurements at the BPG's full bit rate can be started.

Instead of transmitting PRBS sequences (as mentioned in the example above) any kind of user data can be transmitted, provided that the selected user pattern does not exceed the instrument's memory limitation described in the section "Memory Size and User Pattern Restrictions".

In addition, the sub-rate outputs (e.g. at 28 Gbps) can be used for transmitting the data. In this case the inherent pattern length delay must be treated as physical delay and entered into the DQPSK Editor in bits. The value of the receiving bit rate at the EA needs to be set to value of the bit rate which is send out from the BPG.

## DQPSK Pre-coder functionality

This example describes how the transmitter input sequence can be predicted (pre-coded) for BER measurement to be carried out in PRBS mode of the error analyzer. This setup requires two independent input data streams coming from the sub-rate outputs of the BPG. For DQPSK expecting a PRBS pattern at the receive side implicates a non PRBS pattern being transmitted. Thus the BPG needs to send out user defined patterns. The maximal possible transmission rate is determined by the limitation of the sub-rate outputs and can go up to 28 GSymbol/s or 56 Gbps total capacity.⑥

Using the DQPSK Pre-coder tab of the DQPSK editor, a DQPSK Pre-coder is simulated. Two independent and pre-coded input data streams are generated in the software and sent to the user pattern memory of the BPG. The EA will capture either the I or the Q channel's data from the DPSK receiver and performs the BER analysis. If all transmission units are set up correctly the original input data of one of the DQPSK channels should be received by the EA. The related DQPSK Editor settings are shown in figure 15.

In this example the EA shall be setup to receive PRBS $2^{7-1}$ and PRBS $2^{9-1}$ for the demodulated I and Q sequences. The BPG's 28 Gbps sub-rate outputs are used as the data source. It is further assumed that there is no differential delay between the sub-rate outputs and the data inputs of the DQPSK transmitter. This can be ensured by using a set of two cables having an identical electrical length. If a differential delay cannot be avoided it needs to be quantified and entered into the Editor in bits. Similar to the decoding example, both, the hardware transmitter as well as the software transmitter implementation assumes quadrature (90°) phase bias.

⑥ Unless two independent, bit-synchronised channels are provided which can output odd/even bits of the generated DQPSK precoded pattern respectively.

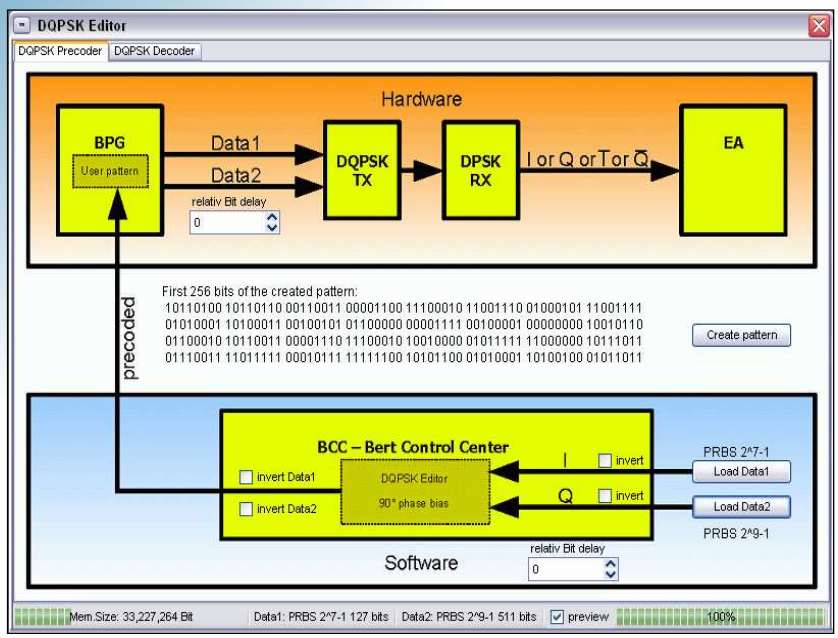


**Figure 15: DQPSK Editor's DQPSK pre-coder tab setting for PRBS output sequences**

When the physical and software simulated system is set up correctly a click on “Create pattern” starts the pattern generation process according to the settings of the DQPSK Editor and the generated pattern is displayed in a Pattern Editor window.

Once the pre-coded BPG pattern is created it can be transferred to the user pattern memory of the BPG by clicking on “Send Pattern to BPG”. A system depended file dialog will show up asking for a filename for saving the generated pattern.

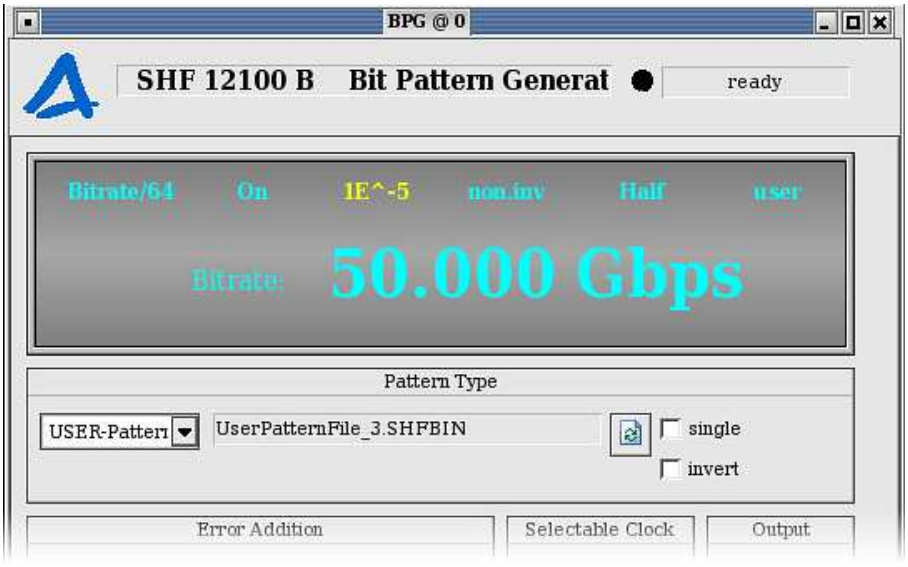


**Figure 16: BPG's graphical representation (User Pattern mode)**

## BPG settings

After downloading the created pattern to the BPG, the BPG has to be set to send out this pattern by choosing the USER Pattern mode and selecting the file name of that pattern. The bit rate value of the EA has to be set to the expected value (keeping in mind that the BPG's sub-rate outputs are used to transmit the data). Referring to figure 16 where the BPG is running at 50 Gbps means that the sub-rate outputs operate at 25 Gbps. Thus the EA has to be set to 25 Gbps.

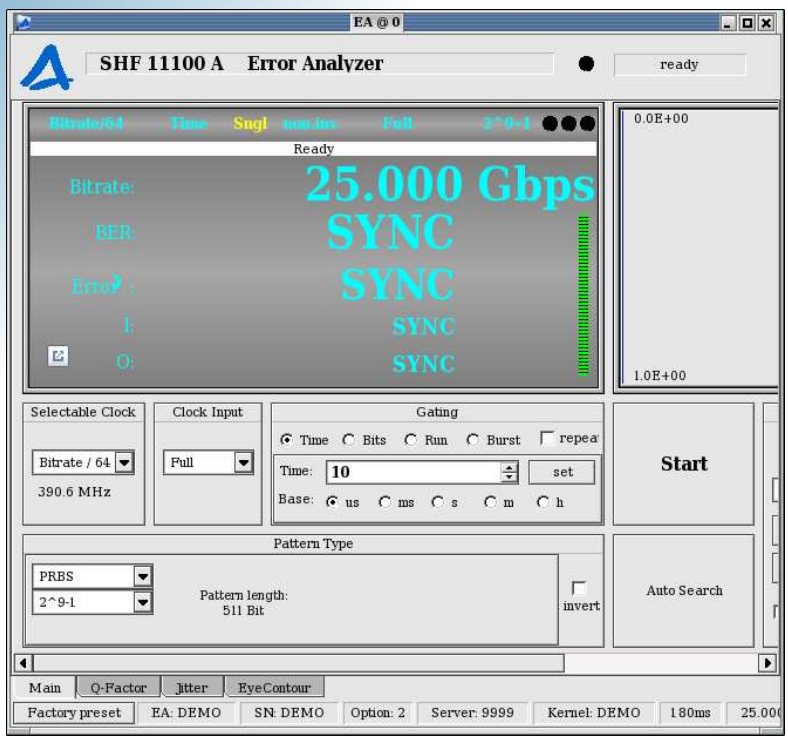


**Figure 17: Error Analyzer's graphical representation (PRBS mode)**

## EA settings

Since the data comes from the sub-rate outputs of the BPG and since the EA is connected to a DPSK receiver adjusted to receive either I or Q channel the EA has to run at half of the BPG's bit rate. To enable a proper BER analysis the pattern type of the EA should be set to PRBS with the right pattern length (in this example PRBS $2^{9-1}$). If the EA does not synchronize properly a problem during signal transmission might have been occurred.

In that case please:

- Ensure good eyes at the output of the DQPSK transmitter. Try to optimize the output signal by changing the transmitter's Phase Bias Voltage. If this is not successful a manual Driver Bias change might be necessary.
- Ensure good eyes at the output of the DPSK receiver. Optimize the signal by adjusting the receivers Heater Power value.
- The correct DQPSK channel is selected and received. After clicking on “Start”, try to select another DQPSK channel, by tracking it trough varying the DPSK receiver's Phase Bias setting. Alternatively, try to adjust the settings made in the DQPSK Editor.

Now everything is set up for BER testing.

# Memory Size and User Pattern Restrictions

The amount of data to be used for user patterns is determined by the built-in memory size (which is 134,217,728 bits). Furthermore, the internal configuration of the BPG (and EA) requires the user pattern to have a granularity of 256 bits, which is the amount of data being processed per operation under user pattern mode. Thus the length constraints for the user pattern are:

$$L_{pattern} \leq 134{,}217{,}728\,bit \quad (1)$$

$$L_{pattern} \bmod 256 = 0 \quad (2)$$

Constraint (1) is straight forward. There is no way to exceed the maximum pattern length as it is defined by the maximum available memory of the instruments.

Constraint (2) implies that after division of the pattern length by 256 the remainder must be zero. I.e. the pattern length must be exact multiples of 256. For sequences which do not fit into that scheme this constraint can be circumvented by repeating the user pattern several times until the resulting pattern length is divisible by 256. The following two examples help to clarify this approach.

- **Example 1: User pattern with a word length of 384 bits**
  384 is not divisible by 256 i.e. constraint (2) is not met. By repeating this pattern a second time we will get a pattern length of 768; which is divisible by 256 and constraint is met. Thus the resulting user pattern used for the BERT system will consist of two times the original pattern length.
- **Example 2: PRBS $2^{7-1}$**
  PRBS $2^{7-1}$ has a pattern length of 127 bit which is obviously not divisible by 256. Applying the previously described approach will yield that we will have to repeat the pattern 256 times until constraint (2) is met; thus resulting in a user pattern length of 32512 bits.

For ease of use this repetition of the user pattern will be automatically handled by the BCC.

A simple way to maximize the usage of the limited internal memory size is to make the user pattern length an exact multiple of 256 (whenever possible).

When looking for example at a user pattern of 524,289 bits it is obvious that constraint (1) is met. Since 524,289 mod 256 is 1 constraint (2) is not met, i.e. the BCC software tries to repeat the pattern until if meets constraint (2). This is the case after 256 repetitions which results in a total pattern length of 134217984. This would be too large to fit into the available memory and therefore constraint (1) is not met anymore. However, it would be easy to meet both constraints in the first place by making the user pattern 1 bit shorter. This means a user pattern of 524,288 fits perfectly into the scheme.

# DQPSK Pre-coding

Referring to the above thoughts, the below table can be worked out to show possible PRBS patterns used in the EA resulting in user patterns for the BPG fulfilling memory size as well as the granularity of 256 bits.

| | | I- Channel | | | |
|---|---|---|---|---|---|
| | | PRBS $2^{7}$-1 | PRBS $2^{9}$-1 | PRBS $2^{11}$-1 | PRBS $2^{15}$-1 |
| Q-Channel | PRBS $2^{7}$-1 | ✓ | ✓ | ✓ | |
| | PRBS $2^{9}$-1 | ✓ | ✓ | | |
| | PRBS $2^{11}$-1 | ✓ | | ✓ | |
| | PRBS $2^{15}$-1 | | | | ✓ |

# Decoding

In case of user pattern prediction for BER measurement in EA there is a further restriction due to the limited memory allocated for User Real-time measurement. As a result, the maximum length that can be used in the EA input is limited to 2^11 -1.

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