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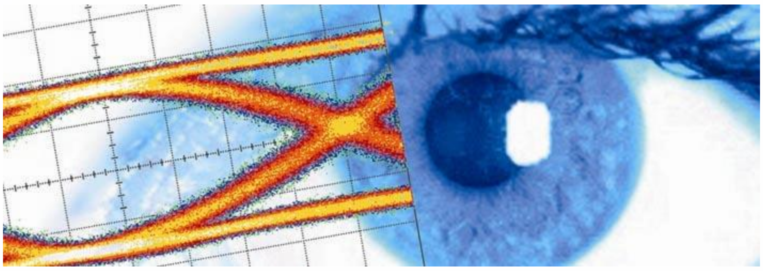
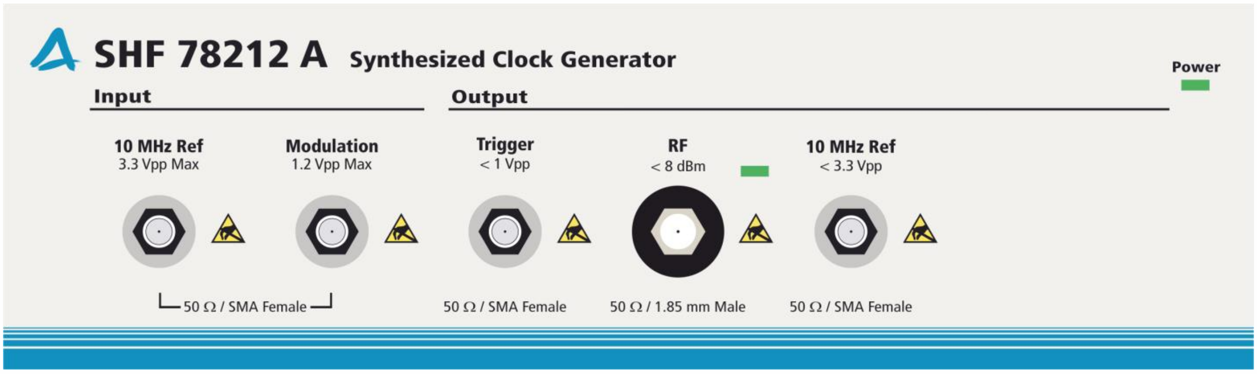


Datasheet

SHF 78212 A

Synthesized Clock Generator



Description

The Synthesized Clock Generator SHF 78212 A is designed to provide our BERT system customers with a suitable internal clock source at reasonable cost. It is a field replaceable plug-in module which needs to be installed in an SHF mainframe. Together with other plug-in modules from this instruments series, a modular and scalable measurement system can be put together.

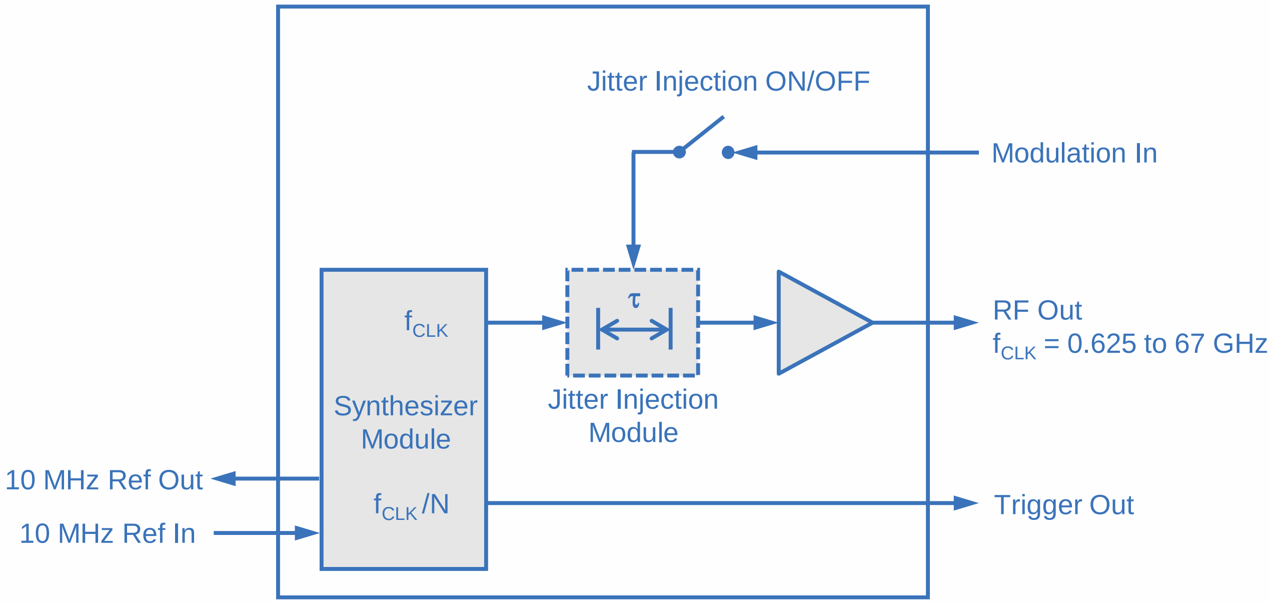
It features a wide frequency range **from 0.625 to 67 GHz with a 1 kHz resolution** and a large output power (**typically 8 dBm up to 60 GHz and 3 dBm up to 67 GHz**). The output power can be adjusted in 0.1 dB steps.

The clock source generates clock signals with low jitter and low phase noise. For frequencies above 10 GHz, additional band-pass filtering ensures low harmonic levels. Below 10 GHz, short rise time clock signals are generated resulting in an increased level of higher-order harmonics.

The **jitter injection** functionality is integrated for jitter stress test applications. Arbitrary jitter types may be applied to the clock signal by connecting an external signal source to the **modulation input**, enabling various test scenarios such as compliance testing.

An additional **trigger output** provides a trigger signal whose frequency can be switched to a quarter (CLK/4 mode) or half the output frequency (CLK/2 mode). Above 40 GHz, the trigger is limited to CLK/4 mode.

Block Diagram



Features

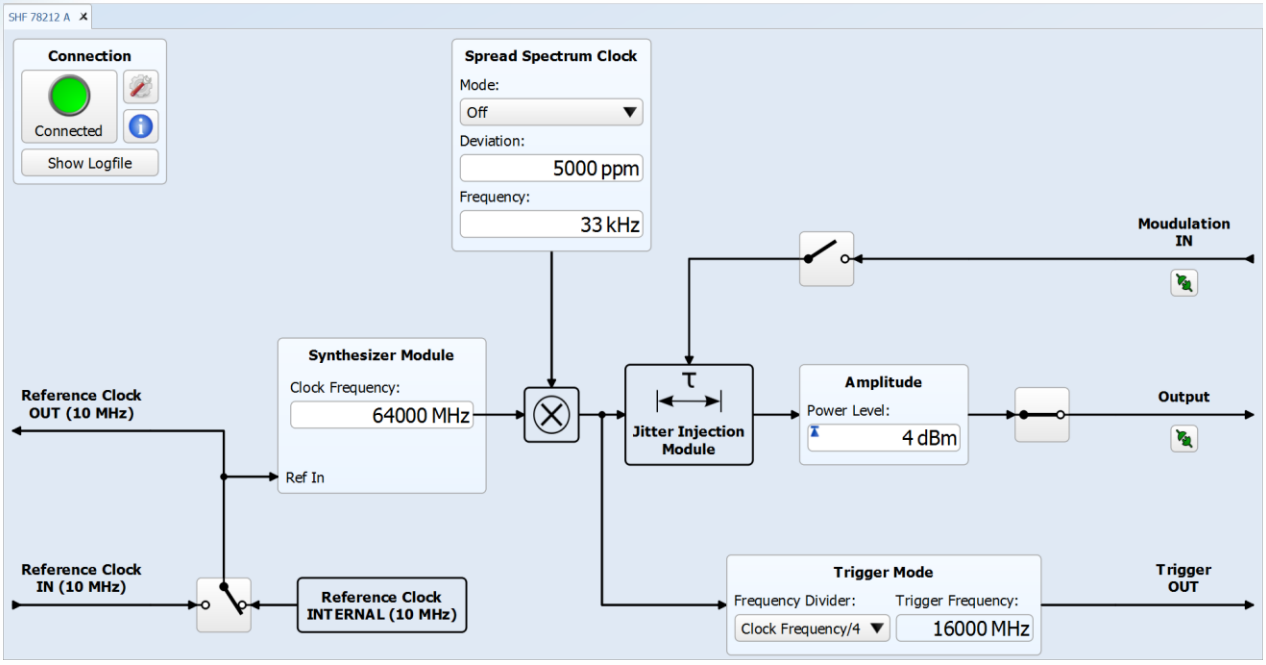
- Output clock frequency ranges from f_{CLK} = 0.625 to 67 GHz with 1 kHz resolution
- Output power adjustable with 0.1 dB resolution from –10 to +8 dBm
- External jitter injection using an external signal source such as SHF 19120 AWG
- Supports three spread-spectrum clocking (SSC) modes
- 10 MHz reference input and output for phase locking to other instruments
- Remote programming interface (Ethernet, USB) for automated measurements

Ease of Use

The SHF 78212 A is operated inside an SHF mainframe and controlled by an external computer. Every system comes along with the intuitive, easy to use SHF Control Center. It provides the interface for changing the device parameters.

Additionally, the instrument may be programmed remotely over the Ethernet connection for automated tests and measurements. Please refer to the *SHF BERT Programming Manual*.

Note that SHF also offers the compact standalone Synthesized Clock Generator SHF 78122 B. Please visit www.shf.de for further details.



SHF Control Center window for the SHF 78212 A

Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Clock Output (RF Out)						
Operating Frequency	f_{CLK}	GHz	0.625		67	
Frequency Resolution		kHz	1			
Frequency Accuracy		ppb	–1000		+1000	Using internal reference
Frequency Stability		ppb	–50		+50	Ambient temperature 21°C
Frequency Stability Aging		ppb	–500		+500	per year
Minimum Output Power	$P_{out,min}$	dBm			–10	
Maximum Output Power	$P_{out,max}$	dBm	8 6 3	 8 4		f_{CLK} ≤ 38 GHz f_{CLK} ≤ 62 GHz f_{CLK} ≤ 67 GHz
Output Power Resolution		dB	0.1			
Output Power Accuracy		dB	–1		1	Ambient temperature 21°C
Output Power Temperature Drift		dB/°C			0.1	
Harmonic Signals		dBc			–20	For f_{CLK} ≥ 10 GHz
Phase Noise		dBc/Hz		 –90 –92 –85 –109		f_{CLK} = 10 GHz 1 kHz offset 10 kHz offset 100 kHz offset 1 MHz offset
Jitter (RMS)	J_{RMS}	fs			400	For f_{CLK} ≥ 10 GHz; On scope display (not deconvolved)
Output Impedance		Ω		50		
Connector						1.85 mm (V) male

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Trigger Out						
Frequency		GHz	0.15625		21	
Output Amplitude		mVpp	400		1000	
Output Impedance		Ω		50		
Connector						SMA female

External Jitter Injection						
Modulation Frequency		MHz	0.5		1000	
Modulation Amplitude		mVpp	0		1200	
Jitter Amplitude		ps	0		50	Peak-to-peak
Input Impedance		Ω		50		
Connector						SMA female

Spread Spectrum Clocking						
Modulation Frequency		Hz	10		100 k	
Deviation		ppm	0		20,000	Up/down/center

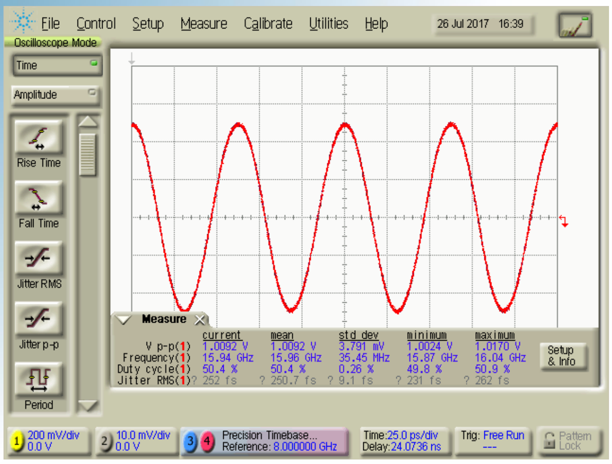
10 MHz Ref Input						
Reference Frequency	f_{ref}	MHz		10		
Amplitude		Vpp	0.2		3.3	
Input Impedance		Ω		50		
Connector						SMA female

10 MHz Ref Output (using internal reference setting) [1]						
Reference Frequency		MHz		10		
Amplitude		Vpp			0.8	
Output Impedance		Ω		50		
Frequency Accuracy		ppb	–250		250	
Frequency Stability		ppb	–50		+50	Ambient temperature 21°C
Frequency Stability Aging		ppb	–300		+300	per year
Connector						SMA female

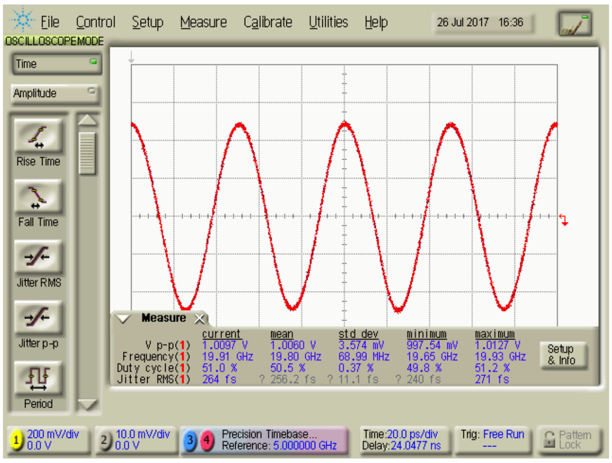
General						
Power Consumption		W			25	Power supplied by SHF Mainframe
Weight		kg		4		
Operating Temperature		°C	10		35	Ambient temperature

[1] The specifications in this datasheet are only valid if the internal reference is activated. If the external reference setting is activated the signal at Ref In is fed through to Ref Out. In this case the parameters frequency, stability and amplitude depend on the Ref In signal.

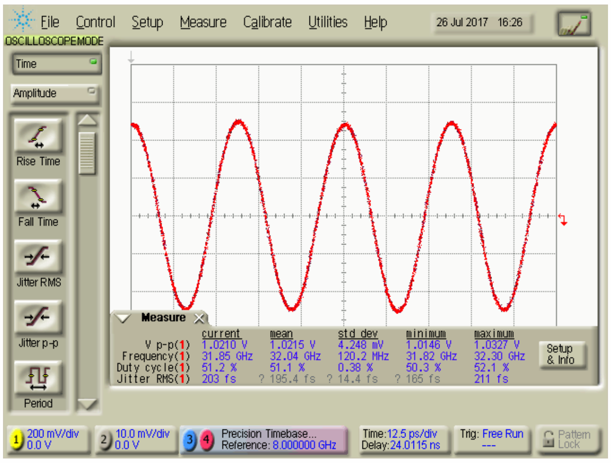
Typical Output Waveforms



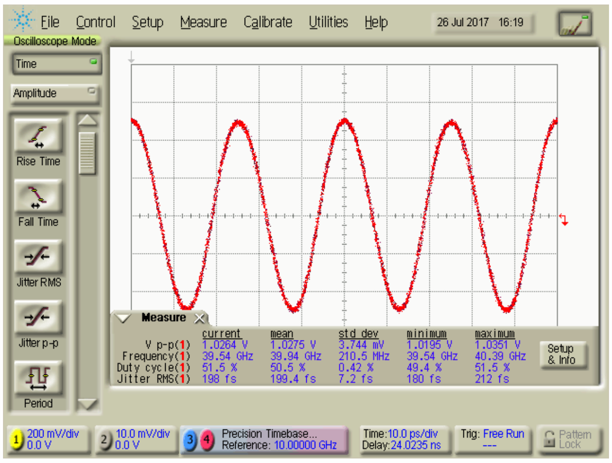
16 GHz clock output at 4 dBm



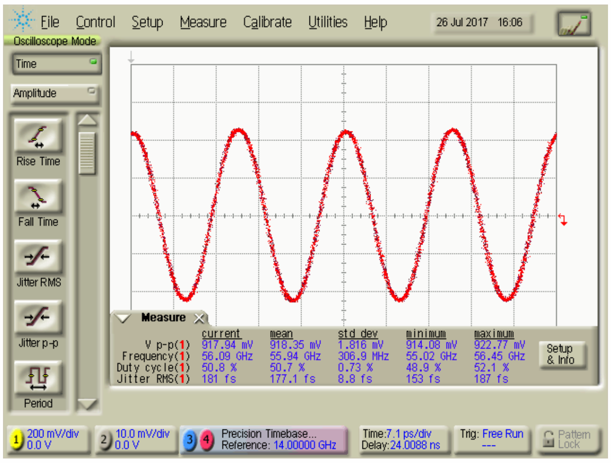
20 GHz clock output at 4 dBm



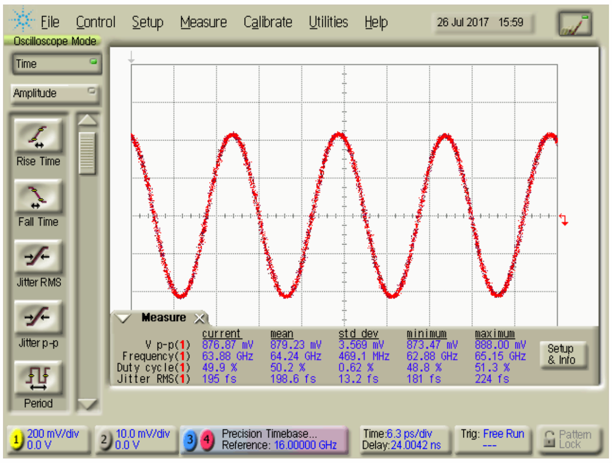
32 GHz clock output at 4 dBm



40 GHz clock output at 4 dBm



56 GHz clock output at 4 dBm



64 GHz clock output at 4 dBm

Note that for clock frequencies above 10 GHz, the signal is band-pass filtered to achieve low harmonics and a nearly pure sinusoid. Below 10 GHz, however, the clock signals are amplified with subsequent amplitude clipping to shorten the rise time. In the frequency range below 10 GHz, this generates noticeable higher-order harmonics. The SHF 78212 A is optimized for clock source applications in combination with SHF BERT instruments, where a short rise time is preferred.

Output Amplitude

The output amplitude can be varied from -10 to +8 dBm. By default, the amplitude is software-limited to +4 dBm to prevent damage on connected devices. If required the instrument can be configured to set the amplitude to the available hardware maximum. The typical hardware maximum is +8 dBm up to 62 GHz and +4 dBm up to 67 GHz. The amplitude can be set in 0.1 dB steps.

For clock frequencies above 10 GHz, the amplitude value in dBm, P_{dBm}, can be converted from and to V_{pp} using the following equations which are valid in a 50 Ω system:

$$P_{dBm} = 20\log_{10}(V_{pp}) + 4 \quad \text{(Eq. 1)}$$

$$V_{pp} = 10^{(P_{dBm}-4)/20}. \quad \text{(Eq. 2)}$$

Note that below 10 GHz, the measured V_{pp} will be slightly smaller than the value calculated from (Eq. 2) since the clock signals in that frequency range contain higher order harmonics rather than being a single-tone sinusoid.

External Jitter Injection

For additional flexibility, arbitrary jitter modulation may be applied to the high-speed clock signal. Jitter is injected by connecting a signal source such as an arbitrary waveform generator to the external modulation input. The maximum jitter amplitude is 50 ps peak-to-peak with a modulation bandwidth of up to 1 GHz. As an example, the jitter amplitude of 50 ps corresponds to a relative jitter amplitude of 1.6 unit intervals (UI) at a bit rate of 32 Gbit/s.

The jitter amplitude needs to be calibrated by the user.

In combination with an SHF Bit Pattern Generator and an Error Analyzer, the SHF 78212 A enables a test solution for jitter tolerance tests as required by many telecommunication standards such as 100G Ethernet and 40 GBit/s OTN, FibreChannel, InfiniBand®, PCI Express®, and Serial ATA. For further details please refer to the SHF application note „Jitter Injection using the Multi- Channel BPG“, available online at www.shf.de.

Typical Jittered Signal Waveforms

The external modulation input can be driven by a function generator such as the SHF 19120 Arbitrary Waveform Generators (AWG). The waveform characteristics of the AWG determine the jitter type.

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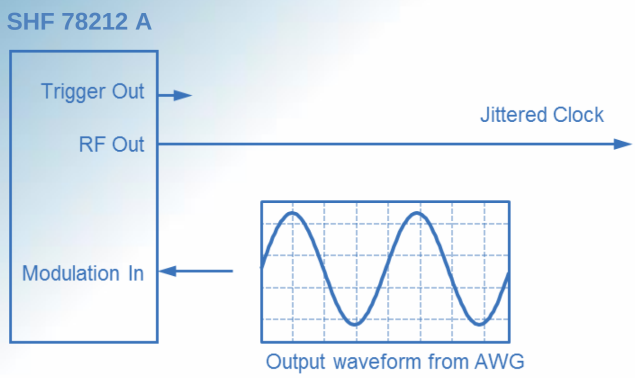
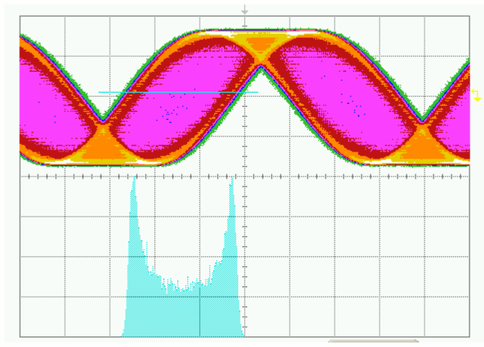
Sine Wave on Modulation Input



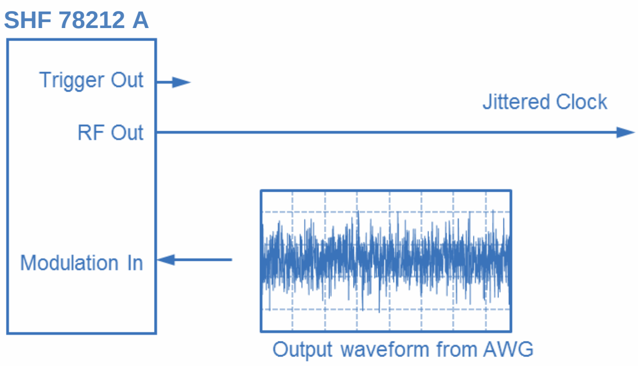
AWG Setting

Waveform Sine wave



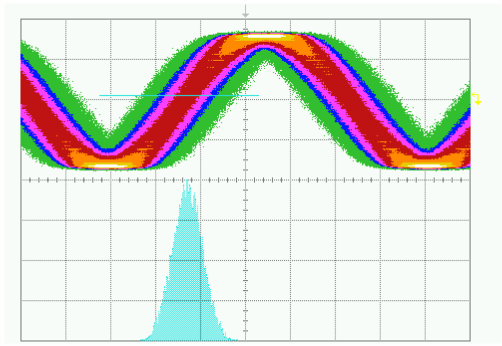
Sinusoidal jitter on 28 GHz clock.

Gaussian-Distributed Noise on Modulation Input



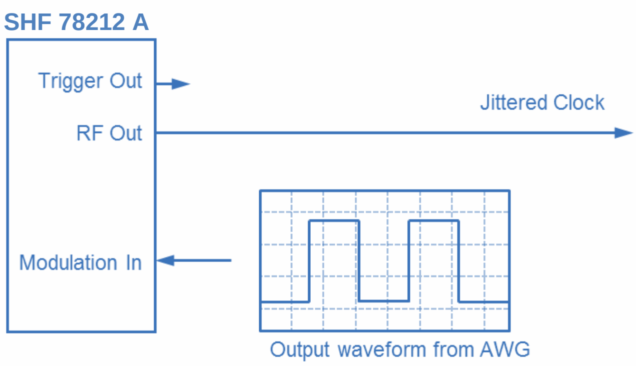
AWG Setting

Waveform: Noise



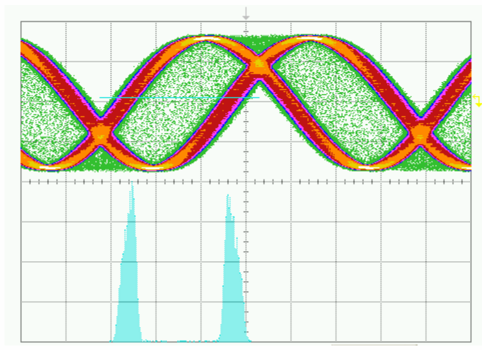
Random jitter on 28 GHz clock.

Square Waveform on Modulation Input



AWG Setting

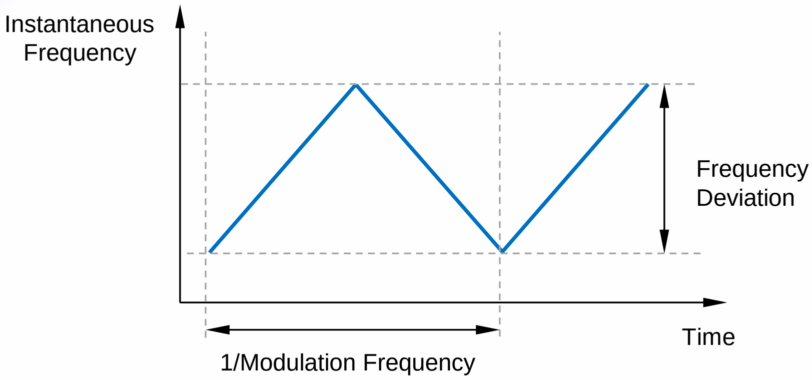
Waveform: Square



Peak-to-peak jitter on 28 GHz clock.

Spread Spectrum Clocking

To meet the regulatory demands of electromagnetic interference several high-speed bus systems use a spread spectrum clocking (SSC) method. When SSC is enabled, the instantaneous frequency of the clock signal varies periodically with time by a small amount, i.e. the clock signal is frequency-modulated. The figure below illustrates the SSC frequency modulation with a triangular shape.



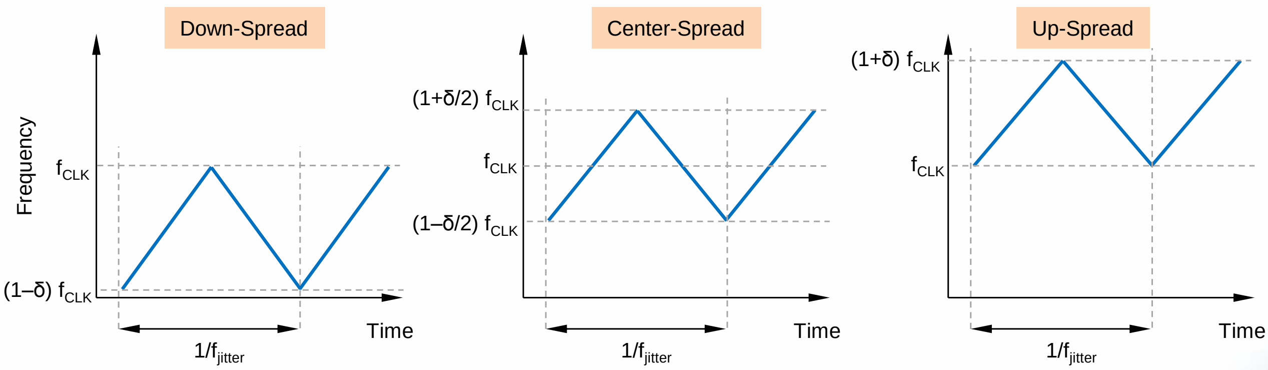
The principle of SSC is the periodic frequency modulation of a clock signal.

The key SSC parameters are the following:

- f_{CLK} original clock frequency without SSC
- δ relative frequency deviation (often given in percent or ppm, parts per million)
- f_{jitter} modulation frequency.

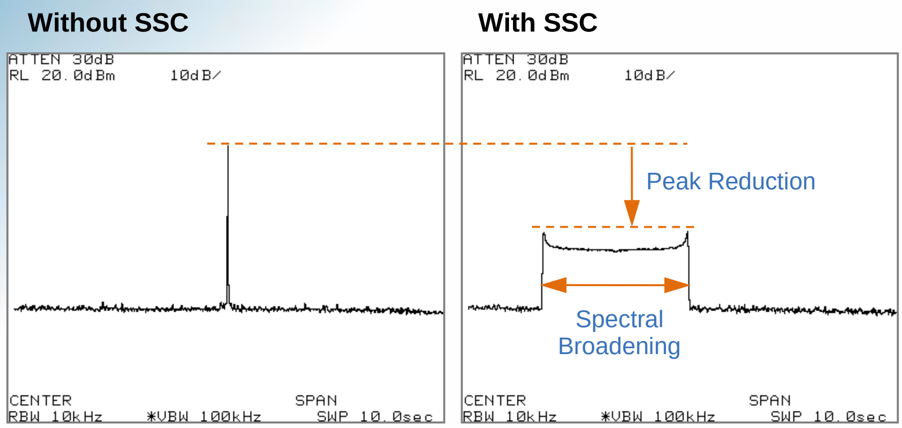
The parameters are directly accessible in the BERT Control Center software GUI or through remote programming.

Depending on the relative position of the clock frequency and the frequency deviation, SSC can be classified into three types: down, center, and up-spread. The figure below illustrates the three configurations.



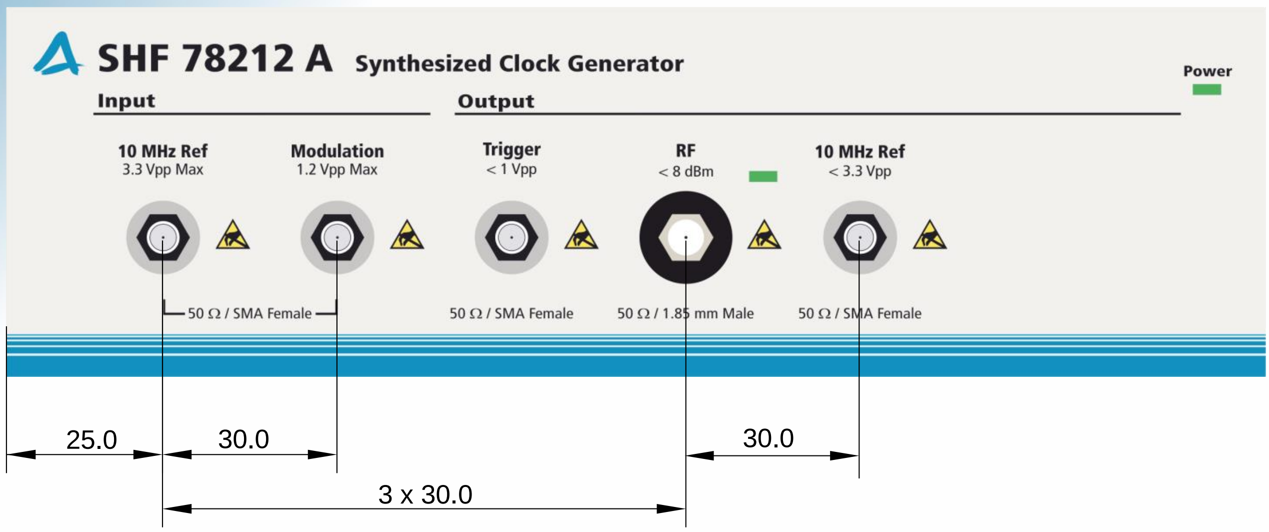
Three types of SSC.

SSC, effectively, broadens the spectral peak of a clock signal so that the maximum of the power spectral density is reduced leading to less radiated emission. This is illustrated in the following spectra measured at the output of the SHF 78212 A for a 25 GHz clock with 30 kHz modulation frequency and 0.5% deviation. Note that SSC does not reduce the total signal power of the clock. Rather, it redistributes the clock's spectral components as shown in the figure below.



SHF 78212 A clock spectrum with and without SSC.

Mechanical Drawing



All dimensions are specified in millimeters (mm).

Input Connectors

Connector Name	Description
10 MHz Ref	External 10 MHz reference input
Modulation	External jitter modulation input

Output Connectors

Connector Name	Description
Trigger	Trigger output
RF	Clock output
10 MHz Ref	10 MHz reference output

SHF Communication Technologies AG
the bandwidth company