Datasheet
SHF 11126 A
51 to 65 Gbps Clock Recovery

For illustration only, actual product may vary
Description

The SHF 11126 A clock recovery is designed to extract the clock from a serial NRZ input data stream. It covers a wide range of input data rates from 51 Gbps to 65 Gbps. The required internal reference clock is provided by an integrated synthesizer module.

The instrument is controlled remotely by Ethernet connection from a PC running the SHF BERT Control Center software (BCC) or the SHF Control Center (SCC). Its programming features allow automated measurements.

The compact size of the clock recovery allows placement very close to the DUT in the test setup.

Features

- Operating data rate range from 51 to 65 Gbps
- Operates also at sub-rates of 51 to 65 Gbps but extracted clock refers to full data rate
- Clock output frequency at half and optionally full rate of the data rate set in the GUI
- Remote operation via Ethernet connection from a host PC (SHF BERT Control Center)
- Compact size: 221.4 mm (W) x 50.8 mm (H) x 177 mm (D)

Applications

- R&D for characterization of chips, devices, transceiver modules and sub-components
- Characterization of high speed optical and electrical links
- Research, development, production tests, on-wafer testing
- OIF CEI - 56G, InfiniBand®
- Proprietary interfaces (chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables)

Options

Option FC – Full Clock Out

Adds a frequency doubler providing a clock at the frequency of the nominal input data rate.

Block Diagram

![Block Diagram](Diagram)
## Specifications – SHF 11126 A

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bit Rate</td>
<td>Gbps</td>
<td></td>
<td>51</td>
<td></td>
<td>65</td>
<td>NRZ data format</td>
</tr>
<tr>
<td>Input Level</td>
<td>mV</td>
<td>$V_{\text{eyeamp}}$</td>
<td>200</td>
<td></td>
<td>600</td>
<td></td>
</tr>
<tr>
<td>Connector Type</td>
<td>Ω</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>2.92 mm (K) female</td>
</tr>
<tr>
<td><strong>Clock/2 Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Frequency</td>
<td>GHz</td>
<td>$f_{\text{out,clock}}$</td>
<td>25.5</td>
<td></td>
<td>32.5</td>
<td></td>
</tr>
<tr>
<td>Output Level</td>
<td>mVpp</td>
<td>$V_{\text{out,clock}}$</td>
<td>550</td>
<td></td>
<td>750</td>
<td></td>
</tr>
<tr>
<td>Output Jitter (RMS)</td>
<td>fs</td>
<td>$J_{\text{RMS}}$</td>
<td>300</td>
<td></td>
<td>450</td>
<td>with low jitter reference input signal</td>
</tr>
<tr>
<td>Connector Type</td>
<td>Ω</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>2.92 mm (K) female</td>
</tr>
<tr>
<td><strong>Full Clock Output (Optional)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Frequency</td>
<td>GHz</td>
<td>$f_{\text{out,clock}}$</td>
<td>51</td>
<td></td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>Output Level</td>
<td>mVpp</td>
<td>$V_{\text{out,clock}}$</td>
<td>500</td>
<td></td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>Output Jitter (RMS)</td>
<td>fs</td>
<td>$J_{\text{RMS}}$</td>
<td>450</td>
<td></td>
<td></td>
<td>with low jitter reference input signal</td>
</tr>
<tr>
<td>Connector Type</td>
<td>Ω</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>1.85 mm (V) female</td>
</tr>
<tr>
<td><strong>General</strong></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>V</td>
<td>$V_{\text{ee}}$</td>
<td>11.5</td>
<td>12</td>
<td>12.5</td>
<td>+12V switching power supply is included</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>W</td>
<td>$P_{\text{tot}}$</td>
<td>7.2</td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Height</td>
<td>mm</td>
<td>$H$</td>
<td>50.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Width</td>
<td>mm</td>
<td>$W$</td>
<td>221.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Depth</td>
<td>mm</td>
<td>$D$</td>
<td>177</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>g</td>
<td>$m$</td>
<td>1500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case Temperature</td>
<td>°C</td>
<td>$T_{\text{case}}$</td>
<td>15</td>
<td>35</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Typical Output Waveforms

Data In @ 51 Gbps
Clock/ Out @ 51 Gbps → 25.5 GHz

Data In @ 52 Gbps
Clock/ Out @ 52 Gbps → 26 GHz

Data In @ 53 Gbps
Clock/ Out @ 53 Gbps → 26.5 GHz
Data In @ 54 Gbps
Clock/Out @ 54 Gbps → 27 GHz

Data In @ 55 Gbps
Clock/Out @ 55 Gbps → 27.5 GHz

Data In @ 56 Gbps
Clock/Out @ 56 Gbps → 28 GHz
SHF reserves the right to change specifications and design without notice – SHF 11126 A - V001 – Sep 6, 2017

Data In @ 57 Gbps

Clock/ Out @ 57 Gbps → 28.5 GHz

Data In @ 58 Gbps

Clock/ Out @ 58 Gbps → 29 GHz

Data In @ 59 Gbps

Clock/ Out @ 59 Gbps → 29.5 GHz
Data In @ 60 Gbps

Clock/Out @ 60 Gbps → 30 GHz

Data In @ 61 Gbps

Clock/Out @ 61 Gbps → 30.5 GHz

Data In @ 62 Gbps

Clock/Out @ 62 Gbps → 31 GHz
Data In @ 63 Gbps

Clock/ Out @ 63 Gbps → 31.5 GHz

Data In @ 64 Gbps

Clock/ Out @ 64 Gbps → 32 GHz

Data In @ 65 Gbps

Clock/ Out @ 65 Gbps → 32.5 GHz
Outline Drawing

all dimensions in mm