

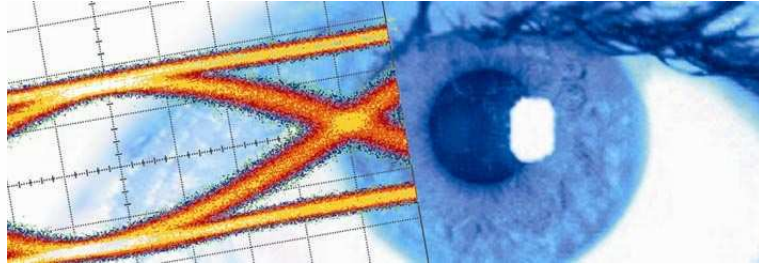


SHF Communication Technologies AG

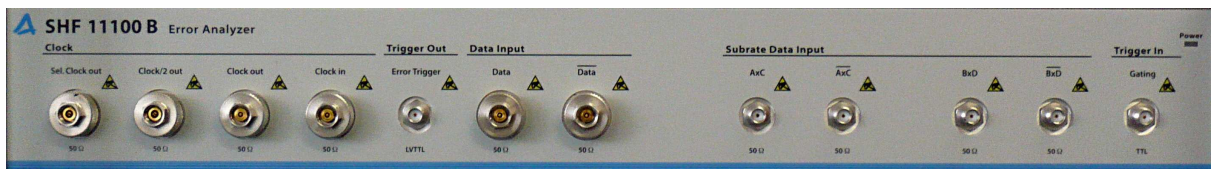
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Datasheet SHF 11100B Error Analyzer





Description

The SHF 11100B is an error analyzer plug-in which can be fitted into any the SHF 10000 Series mainframes.

It has broadband operation from 1.5 to 56 Gbps¹ and features high sensitivity and a wide clock phase margin. It allows the analysis of PRBS signals with pattern lengths of 2^7-1 , 2^9-1 , $2^{11}-1$, $2^{15}-1$, $2^{20}-1$, $2^{23}-1$ and $2^{31}-1$. User patterns can also be analyzed.

In a back-to-back configuration with the SHF 12100 B, the system Q-factor is an impressive 25 (28dB), measured using a $2^{31}-1$ PRBS pattern.

Features

- Scalable and modular system
- Broadband operation up to 56 Gbps¹
- Operation by intuitive software interface
- Q-factor analysis
- Jitter analysis
- Eye contour analysis
- Auto search of optimum sampling point
- Seven built-in PRBS patterns: 2^7-1 , 2^9-1 , $2^{11}-1$, $2^{15}-1$, $2^{20}-1$, $2^{23}-1$, $2^{31}-1$
- Pattern coding and decoding of DQPSK transmission experiments
- Up to 128 MBit user pattern
- Sub-rate clock outputs
- Error Trigger Output

Options

- Option 56 – Guaranteed operation up to 56 Gbps
- Option 010² – Four 12.5 Gbps sub-rate inputs
- Option 020² – Two 25 Gbps (28 Gbps³) sub-rate inputs

¹ Depending on the configuration of the particular system

² Option 020 and 010 cannot be installed at the same time

³ Only if Option 56 is installed



Specifications – SHF 11100B

Parameter	Unit	Min.	Typ.	Max.	Comment
Data input					
Bit rate With Option 56	Gbps	6		50 56	input AC coupled; DC coupled on request (ground referenced CML, 0...-500mV)
S ₁₁	dB			-10	
Sensitivity ⁴	mV		25	50	standard, up to 50 Gbps value corresponds to the measured eye heights on an Agilent 86100 A
Clock phase margin ⁵	°	200			
Threshold adjustment	mV	-300		300	0.5mV steps
Subrate data inputs (optional)	Gbps	1.5		12.5	sensitivity: 100mV
Clock input					
Frequency With option 56	GHz	3 6		25 50 28 56	half clock full clock half clock full clock
Input level	dBm	0		4	
Phase adjustment	ps	0		160	0.1ps resolution
Trigger (gating)					LV TTL
Error trigger output⁶					LV TTL; SMA female

⁴ Value corresponds to the measured eye height on an Agilent 86100 B with 70 GHz sampling heads using 2³¹-1 PRBS at a BER limit of 10⁻⁹

⁵ Note 2: BER limit 10⁻⁹, PRBS 2³¹-1, Eye Height 100 mV_{pp}, Peak-to-Peak-Source-Jitter as displayed on an Agilent 86100 B with 70 GHz sampling heads and precision timebase, calculated using the formula:

$$\text{ClockPhaseMargin[ps]} = 360 \frac{\text{MeasuredClockMargin[ps]} - (\text{Peak-to-Peak-Source-Jitter[ps]})}{\text{EyeLength[ps]}}$$

⁶ Note 3: The Error Trigger will show a logical 1 every time there has been at least one error within 128 bit.



Parameter	Unit	Min.	Typ.	Max.	Comment
Clock outputs					
Frequency	GHz	3		50	clock
	GHz	3		25	clock/2
	MHz	11.7		3125	sel. clock sel: can be switched between bitrate/N (N=16,32,64,128,256,512)
Output level	mV	300	600		clock
		300	450		clock/2
S ₁₁	dB			-10	
System					
Data patterns					2 ⁷ -1, 2 ⁹ -1, 2 ¹¹ -1, 2 ¹⁵ -1, 2 ²⁰ -1, 2 ²³ -1, 2 ³¹ -1
User-programmable pattern	Mbit			128	
Back to back Q factor	linear	25	30		measured with SHF 12100 A @ 40 Gbps, 2 ³¹ -1, 400 mV amplitude
	dB	28	30		

Absolute maximum ratings

Parameter	Unit	Min.	Typ.	Max.	Comment
Data input	V _{pp}			1	
Clock input	V _{pp}			1	
Substrate input	V _{pp}			1	



Typical Sensitivity and Phase Margin

