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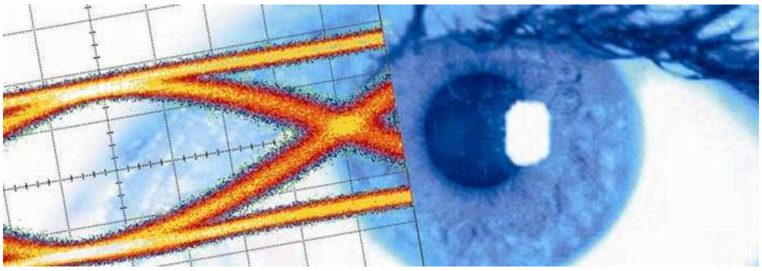
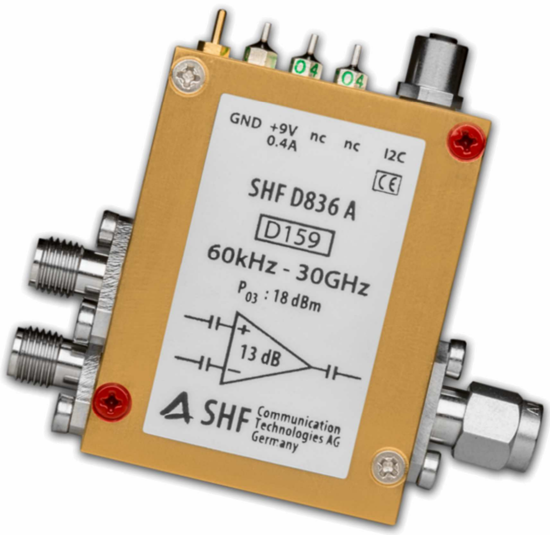


Datasheet

SHF D836 A

Differential to Single-Ended Linear Broadband Amplifier



Description

The SHF D836 A is a differential input, single-ended output linear amplifier designed for PAM4 and 16QAM applications. The single-ended output drive amplitude of up to at least 4 V linear is particularly well suited for state-of-the-art single-drive DP-16QAM modulators. When driven from the differential outputs of a high performance DAC, the common-mode rejection characteristic of this differential input design helps to maintain the linearity and resolution of the DAC.

This amplifier is of a single chip design based on state-of-the-art commercial GaAs process, housed in a special low loss carrier PCB environment to maintain wide bandwidth and low group delay variation, necessary for high performance operation.

Like other amplifiers in the product family, this amplifier enjoys the same benefit of an internal voltage regulation to protect against accidental reverse voltage connection. Similarly, the output amplitude and crossing adjustment using software control via an USB connection. Once adjusted, the connection can be removed until the next time.

Ease of Use

Upon delivery, the amplifier is already pre-set to deliver maximum gain, maximum output amplitude and nominally 50% crossing.

These settings can be modified in an easy to use graphical software interface, as shown below. For connecting the amplifier to the computer, the USB to I2C converter cable, as well as the required software are included with each amplifier with no extra charge.

Once new settings are stored on the device the amplifier will remember the settings until further changes are made. There is no need to connect a computer to the device unless gain, maximum amplitude or crossing adjustments are to be made.

The software is available for download at www.shf.de .

Available Options

01: DC return on output (max. ±1.75 V, max. 35 mA)

02: Built-in bias tee on output (max. ±7 V, max. 220 mA)

Specifications – SHF D836

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Absolute Maximum Ratings						
Maximum RF Input Power in Operation	dBm V	$P_{in\ max}$			4 1	 peak to peak voltage
Maximum RF Input Power without Power Supply	dBm V	$P_{in\ max}$			10 2	 peak to peak voltage
DC Voltage at RF Input	V				±9	AC coupled input
DC Voltage at RF Input	V				±7	AC coupled output
Supply Voltage	V		8		12	0.45 A, reverse voltage protected
Case Temperature[1]	T_{case}	°C	10	40	50	
Electrical Characteristics (At 40°C case temperature, unless otherwise specified)						
High Frequency 3 dB Point	GHz	$f_{HIGH\ InP}$	32			single ended[2], non-inverting input
	GHz	$f_{HIGH\ InN}$	27			single ended[2], inverting input
	GHz	f_{HIGH}	30			Calculated from single ended
Low Frequency 3 dB Point	kHz	f_{LOW}			50	each inputs
Gain	dB	S_{21}	12	13		measured at P_{in}= -27 dBm
Gain Ripple	dB	ΔS_{21}		±0.5	±1	40 MHz…25 GHz, relative to gain-slope
Max. Gain Reduction	dB		-2.5	-3	-4	Control via software interface
Output Power at 1 dB Compression	dBm V	P_{01dB}	15 3.5	16 4		10 MHz…25 GHz peak to peak voltage
Output Power at 2 dB Compression	dBm V	P_{02dB}	17 4.5	18 5		10 MHz…25 GHz peak to peak voltage
Output Power at 3 dB Compression	dBm V	P_{03dB}	19 5,6	19,5 6		10 MHz…25 GHz peak to peak voltage
3rd Order Intercept Point	dBm	IP_3	28			Single ended
Max. RF Input for Linear Operation	dBm V	$P_{in\ lin}$			-4 0.4	I.e. Pout ≤ P01dB peak to peak voltage, single ended
Max. Output Power Reduction	dB			tbd		P_{in} ≥ - 2 dBm Crossing might need to be readjusted by using the crossing control feature. Control via software interface
Crossing Control Range	%			tbd		Control via software interface

[1] If operated with heat sink (part of the delivery) at room temperature there is no need for additional cooling.

[2] Single ended measurement condition with -27dBm input power

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Input Reflection	dB	S_{11}			-15 -10	< 10 GHz, single ended < 20 GHz, single ended
Output Reflection	dB	S_{22}		-10	-9	< 30 GHz
Rise Time/Fall Time	ps	t_r/t_f			8 13.5	20%...80%, 3 V ≤ Vout ≤ 4 V Deconvoluted [3, 4] Full Setup [3]
Jitter	fs	J_{RMS}		500 580	tbd	3 V ≤ Vout ≤ 4 V Deconvoluted [3, 4] Full Setup [3]
Group Delay Ripple	ps				±50	40 MHz…30 GHz, 100 MHz aperture
Power Consumption	W			3.4		9 V supply voltage
Mechanical Characteristics						
Input Connector						2.92mm (K) female[5]
Output Connector						2.92mm (k) male[5]

[2] Single ended measurement condition with -27dBm input power

[3] Measured with: SHF 611 C DAC -> DUT (SHF D836 A) -> Agilent 86100A with 70 GHz sampling head & precision time base.

[4] Calculation based on typical results of setup without DUT :

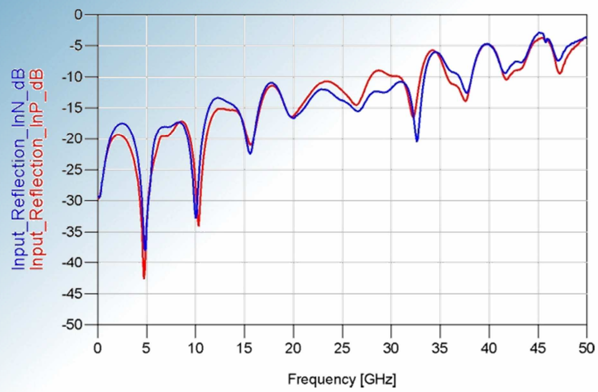
$$t_r/t_{f\ deconvoluted} = \sqrt{(t_r/t_{f\ full\ setup})^2 - (t_r/t_{f\ setup\ w/o\ DUT})^2} = \sqrt{(t_r/t_{f\ full\ setup})^2 - 11\ ps^2}$$

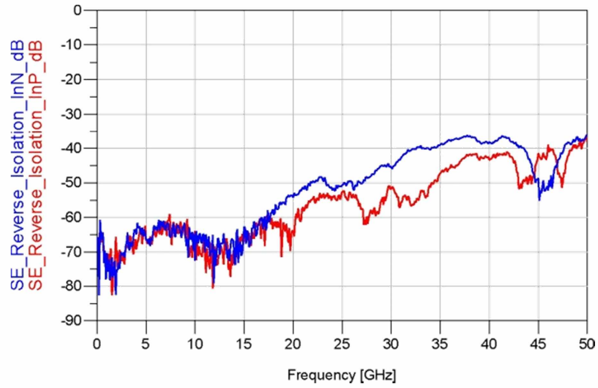
$$J_{RMS\ deconvoluted} = \sqrt{(J_{RMS\ full\ setup})^2 - \left(J_{RMS\ setup\ w/o\ DUT}\right)^2} = \sqrt{(J_{RMS\ full\ setup})^2 - 300\ fs^2}$$

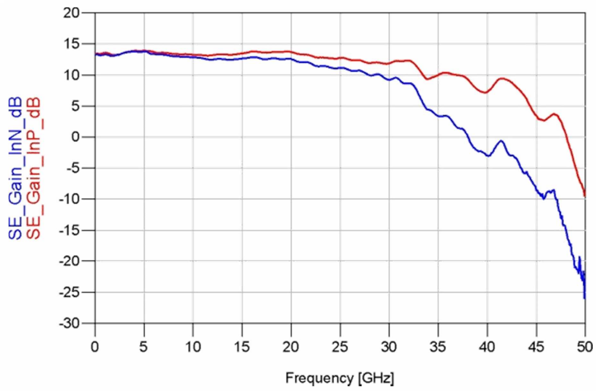
[5] Other gender configurations are available on request. Other connector types are also available but may impact bandwidth & reflection.

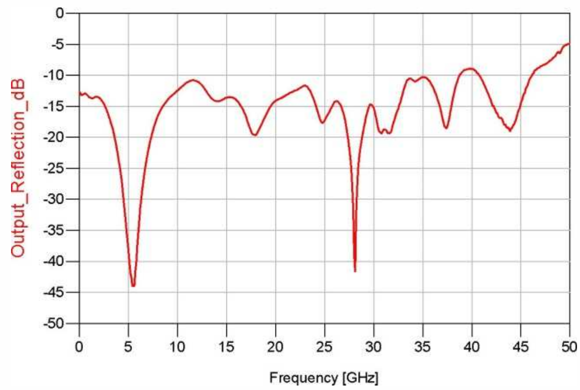
Typical S-Parameters, Group Delay and Phase Response

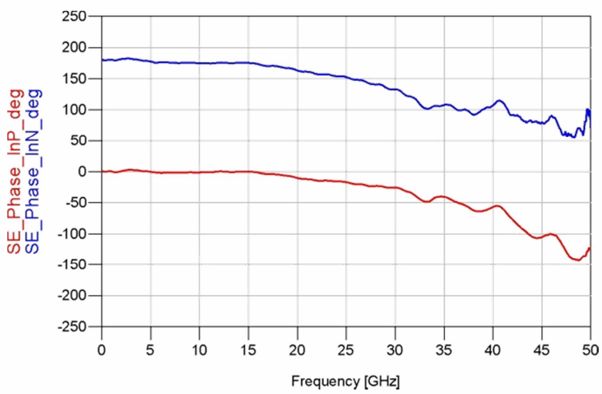
Single-Ended Measurements

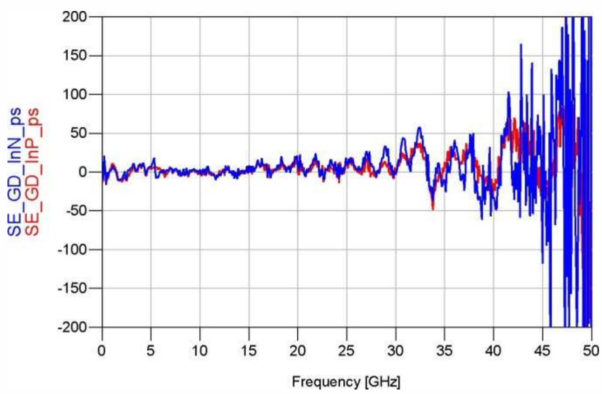






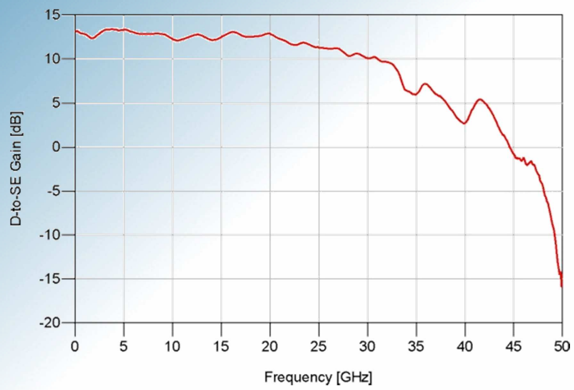


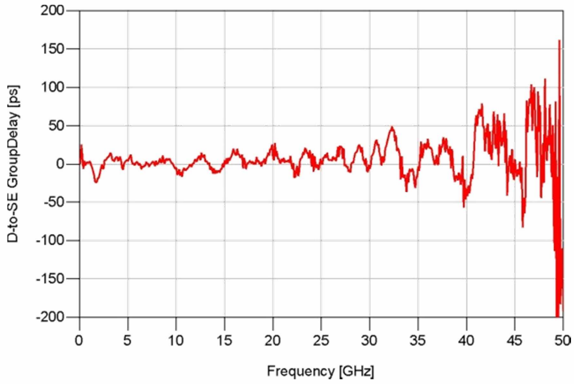


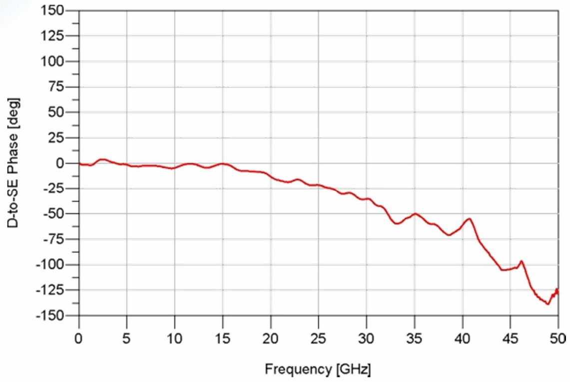


Typical S-Parameters, Group Delay and Phase Response

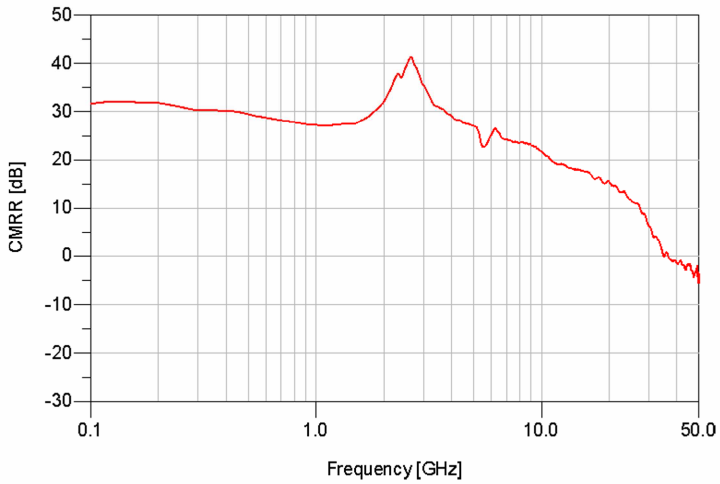
Differential to Single-Ended (calculated from Single-Ended Measurements)





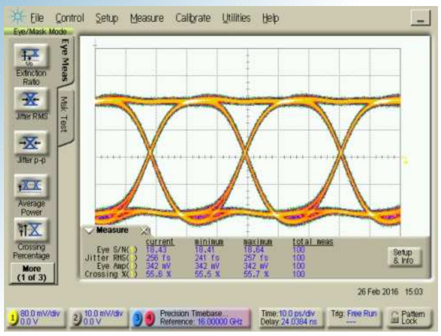


Typical Common-Mode-Rejection-Ratio (CMRR)

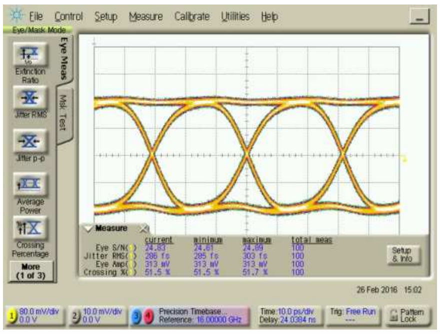


Typical Binary Eye Diagrams

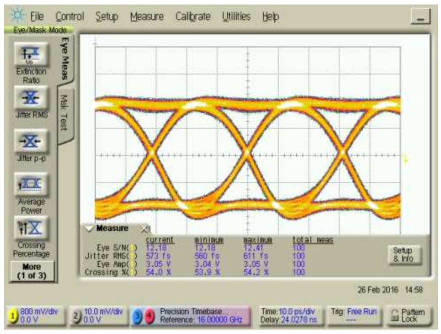
The measurements below had been performed using a SHF 611 C DAC or a SHF 12103 A (for 43 Gbps), respectively and an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A).



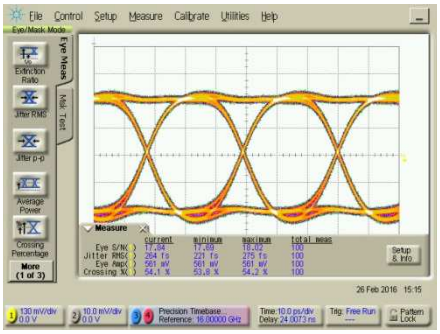
Input Signal InP @ 32 Gbps, Eye amplitude: 342 mV



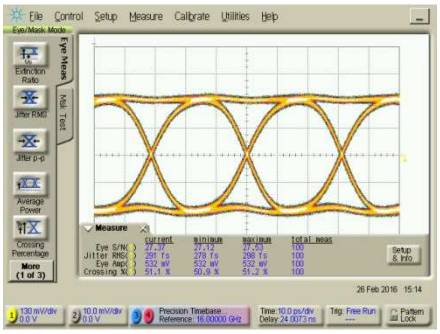
Input Signal InN @ 32 Gbps, Eye amplitude: 313 mV



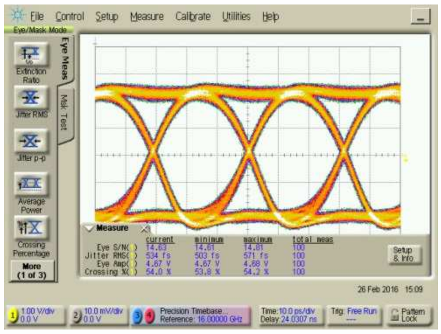
Output Signal @ 32 Gbps, Eye amplitude: 3.05 V



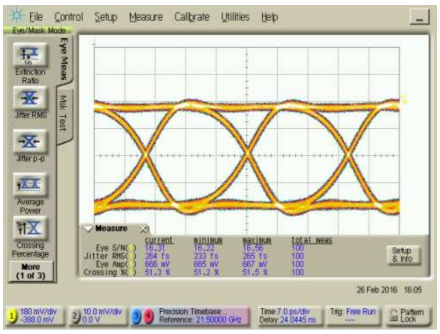
Input Signal InP @ 32 Gbps, Eye amplitude: 561 mV



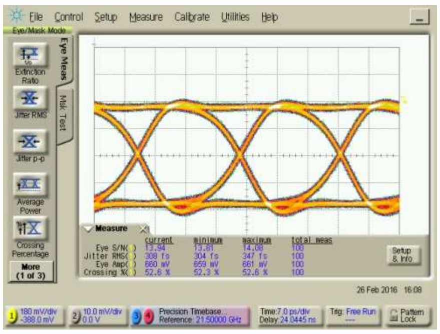
Input Signal InN @ 32 Gbps, Eye amplitude: 532 mV



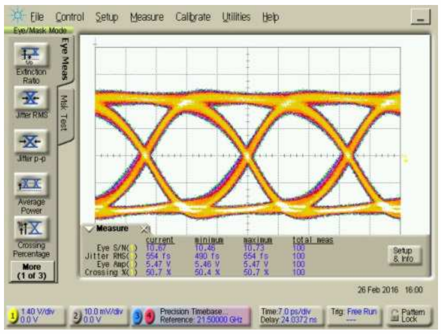
Output Signal @ 32 Gbps, Eye amplitude: 4.67 V



Input Signal InP @ 43 Gbps, Eye amplitude: 666 mV



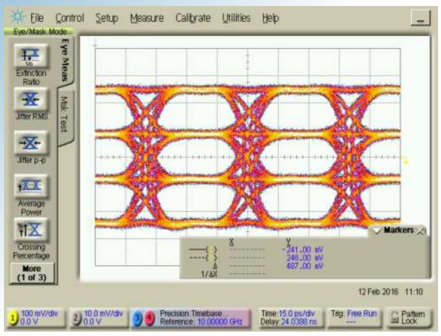
Input Signal InN @ 43 Gbps, Eye amplitude: 660 mV



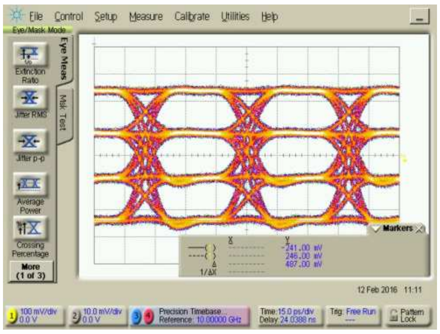
Output Signal @ 43 Gbps, Eye amplitude: 5.47 V

Typical 4-Level Eye diagrams

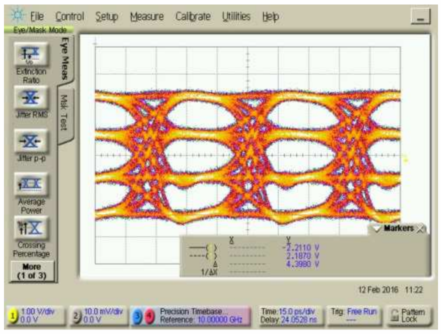
The measurements below had been performed using a SHF 611 C DAC or a SHF 12103 A (for 43 Gbps), respectively and an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A).



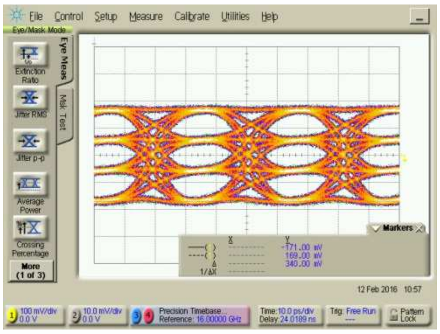
Input Signal InP @ 20 GBaud, Eye amplitude: 487 mV



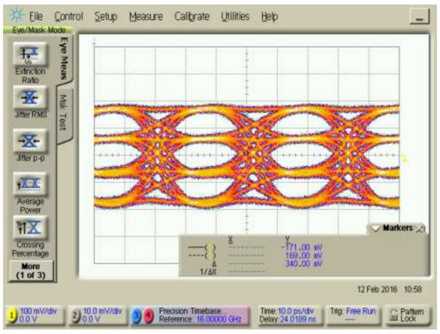
Input Signal InN @ 20 GBaud, Eye amplitude: 487 mV



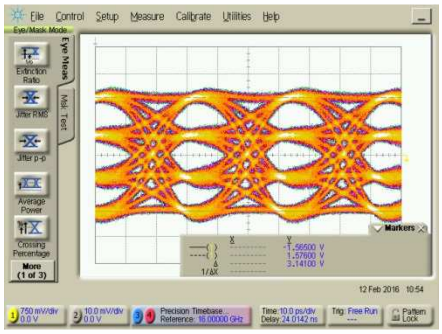
Output Signal @ 20 GBaud, Eye amplitude: 4.39 V



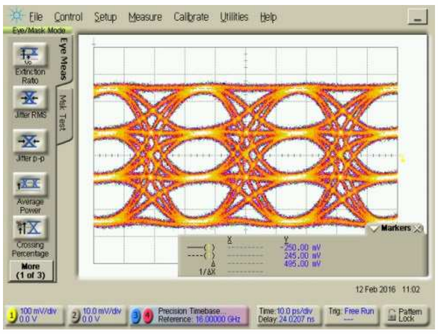
Input Signal InP @ 32 GBaud, Eye amplitude: 340 mV



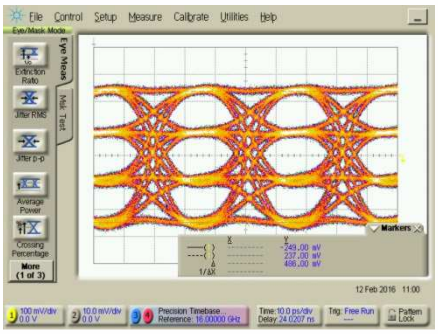
Input Signal InN @ 32 GBaud, Eye amplitude: 340 mV



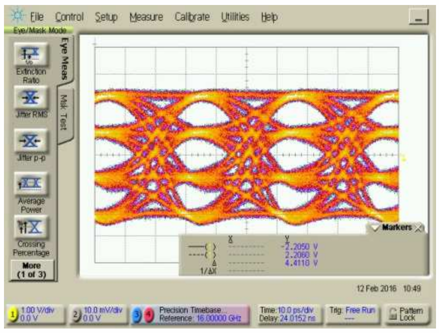
Output Signal @ 32 GBaud, Eye amplitude: 3.14 V



Input Signal InP @ 32 GBaud, Eye amplitude: 495 mV

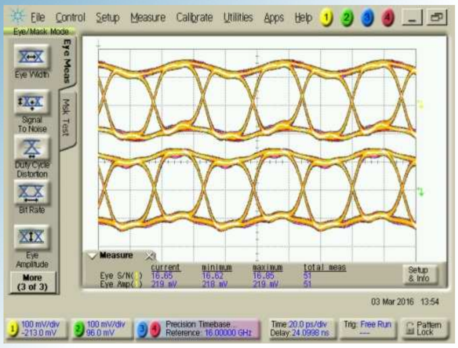


Input Signal InN @ 32 GBaud, Eye amplitude: 486 mV

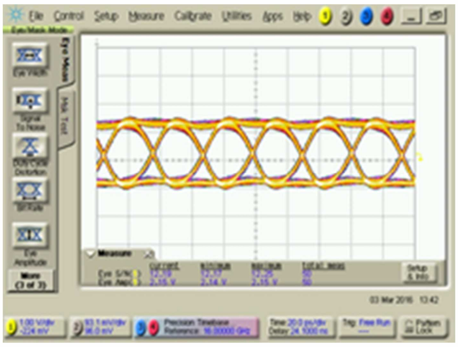


Output Signal @ 32 GBaud, Eye amplitude: 4.41 V

Typical Suppression of common mode interference

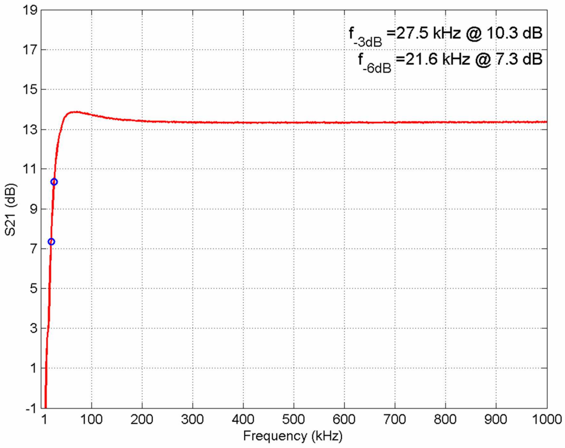


Input Signals 32 GBit/s
100 mV/ 16 GHz interference

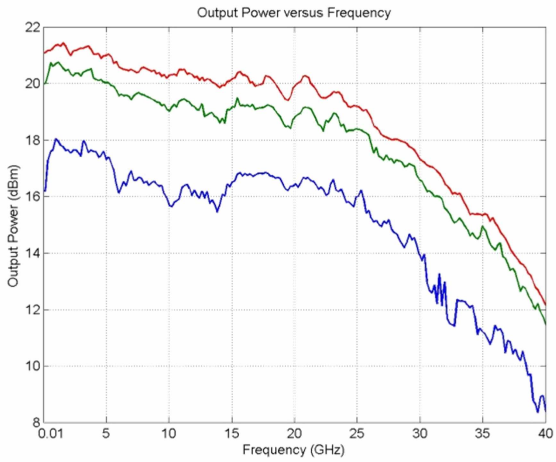


Output Signal 32 GBit/s

Typical Low Frequency Response (<1 MHz)

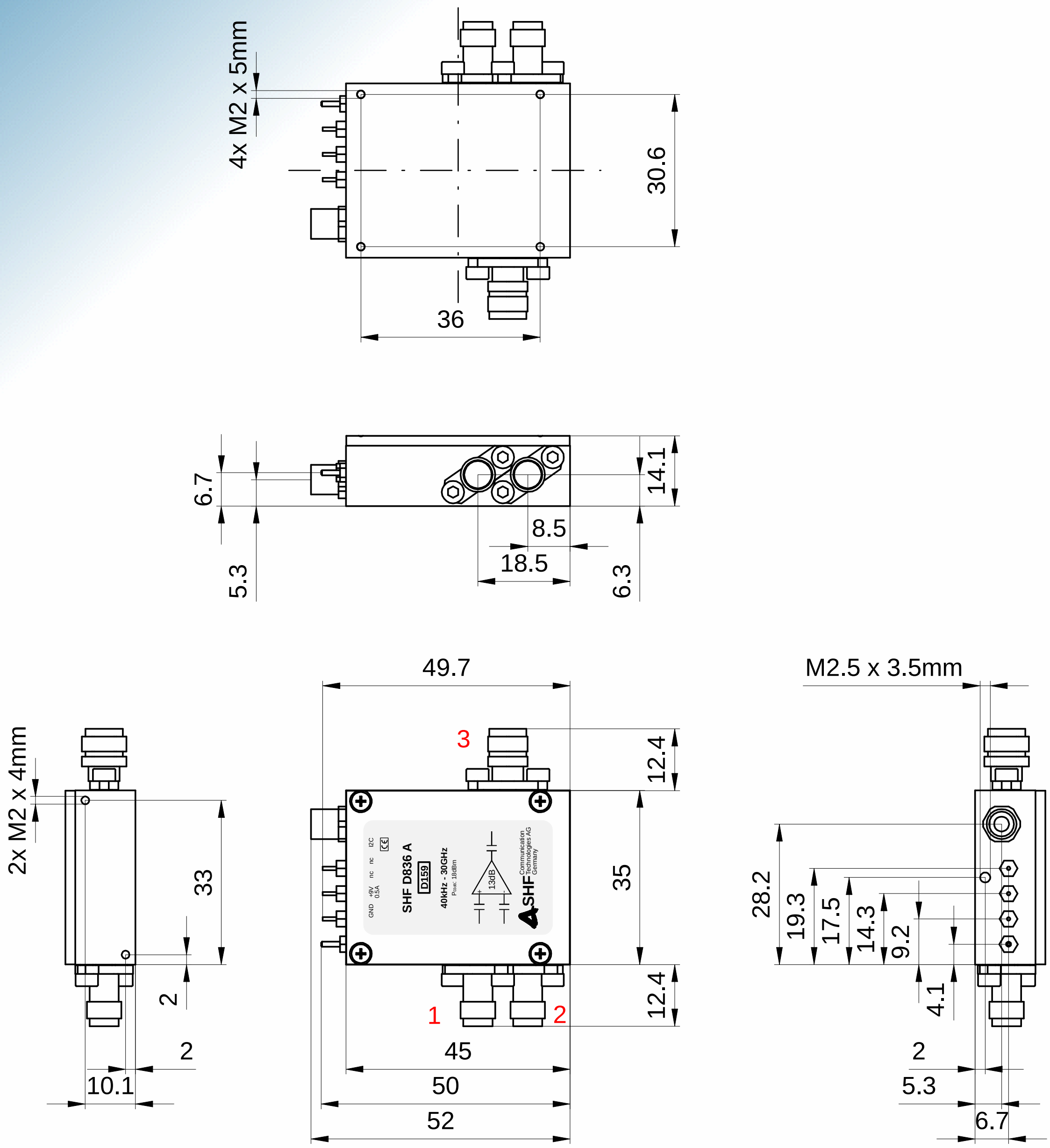


Typical Saturation Power Characteristic (single-ended measurement)

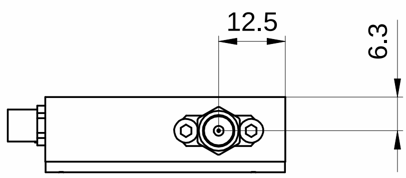


Top (**red**): 3 dB compression;
Middle (**green**): 2 dB compression;
Bottom (**blue**): 1 dB compression

Mechanical Drawing without Heat Sink



Port	Connector
1	non inverting Input
2	inverting Input
3	Output



Pin assignment might change if a bias tee option is chosen.

Thermal resistance of heat sink approx. 6 K/W

For permanent mounting remove the heat sink from the amplifier. In that case please ensure that adequate cooling of the amplifier is guaranteed. It is recommended to use thermal paste or a thermal gap pad for the mounting. In order to separate the heat sink from the amplifier, remove the four screws on the heat sink. Please note, thermal paste is used between the heat sink and the amplifier housing.

User Instructions

ATTENTION!

Electrostatic sensitive GaAs FET amplifier

1. To prevent damage through static charge build up, cables should be always discharged before connecting them to the amplifier!
2. Attach a 50 Ohm output load before supplying DC power to the amplifier!
3. The supply voltage can be taken from any regular 8…12 V, 0.45 A DC power supply and can be connected to the supply feed-through filter via an ON / OFF switch.
4. Using a 3 dB or 6 dB input attenuator will result in a 6 dB or 12 dB increase of the input return loss. For minimal degradation of amplifier rise time, these attenuators should have a bandwidth specification of greater 50 GHz (V/ 1.85mm attenuators)!
5. An input signal of about 0.65 Vpp will produce output swing of about 3 Vpp.
6. Higher input voltages will drive the amplifier’s output stage into saturation, leading to waveform peak clipping.
7. Saturated output voltages can only be used without damage while the amplifier is connected to a 50 Ohm precision load with a VSWR of less than 1.2 or better than 20 dB return loss up to 40 GHz.
8. While using a reflective load the output voltage has to be reduced to a safe operating level according to the magnitudes of the reflections.
9. ATTENTION: At radio frequencies a capacitive load can be transformed to an inductive one through transmission lines! With an output stage driven into saturation this may lead to the immediate destruction of the amplifier (within a few ps)!
10. The input voltage (single ended) should never be greater than 2 Vpp equivalent to 10 dBm input power.