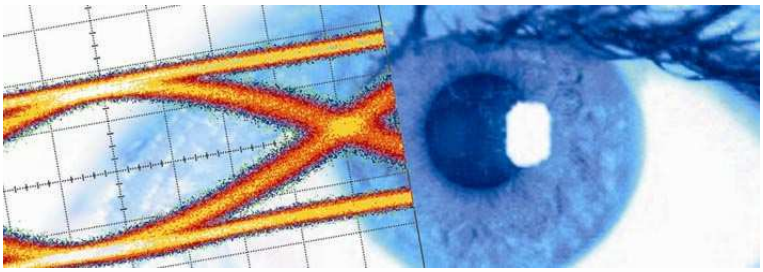
**SHF Communication Technologies AG**

**Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany**

**Phone +49 30 772051-0 • Fax +49 30 7531078**

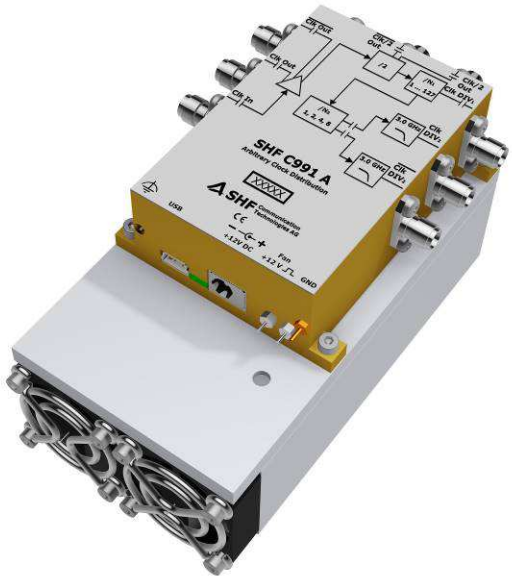
**E-Mail: sales@shf-communication.com • Web: www.shf-communication.com**



# Datasheet

# SHF C991 A

## Arbitrary Clock Distribution






SHF Communication Technologies AG
the bandwidth company

# Description

The SHF C991 A is a versatile broad band clock distribution providing copies of the incoming clock at different divider ratios.

# Features

- Broadband operation from 4 to 64 GHz.
- Multiple clock outputs at different divider ratios.
- Controlled by intuitive graphical user interface BERT Control Center (BCC) via USB
- Controlled by intuitive graphical user interface SHF Control Center (SCC) via USB

# Applications

Test setups are always an interaction of different parts; sophisticated setups may include many different instruments and modules. To operate concurrently a common clock signal is often indispensable. However, frequency requirements of the instruments and modules are very different. A clock distribution is supposed to provide clock signals derived from the master clock (input) at a frequency fraction exactly fitting to the individual requirements.

Some examples for a high-speed (> 40 GHz) clock system are a listed below:

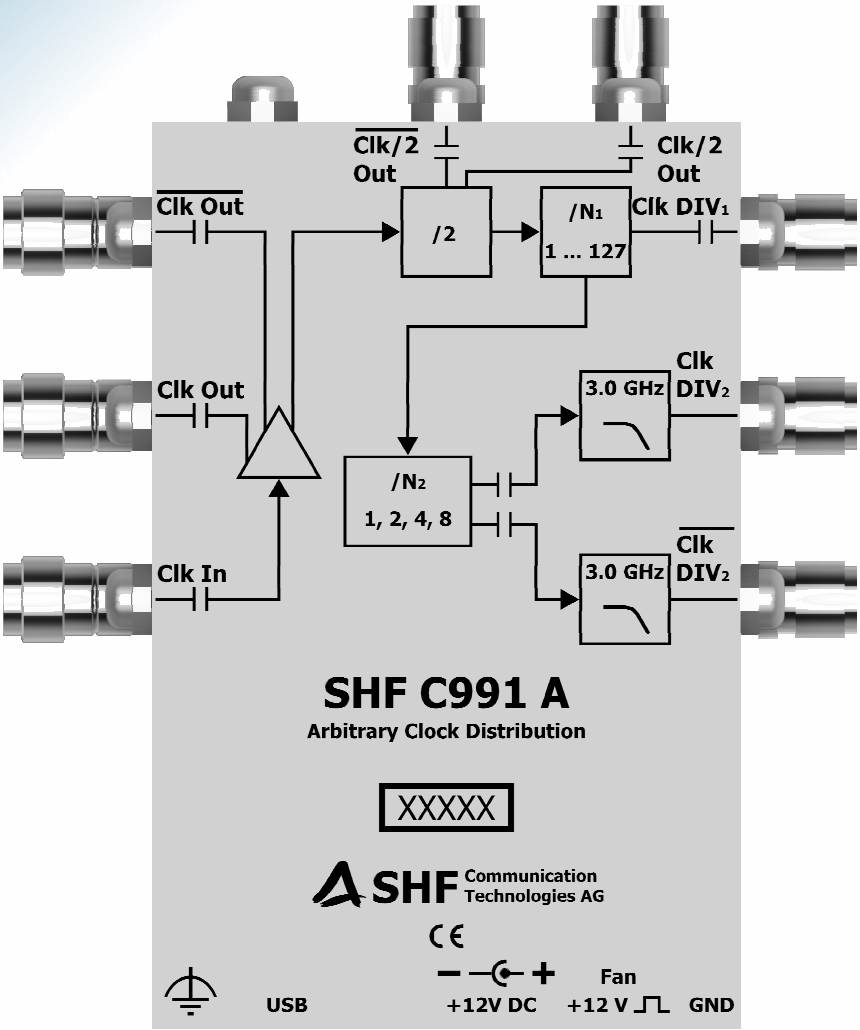
- The clock input is fed with a signal from a signal generator like the SHF 78122 A.
- The full clock outputs can be used to drive remote heads like SHF's DACs, Multiplexers, Demultiplexers or PAM-Multiplexers.
- By selecting the appropriate fraction of the Clock $DIV_1$ output almost all precision time bases, or phase references of commercially available equivalent-time sampling scopes can be driven.
- By setting the LPF Clock output to the appropriate frequency band, the derived signal can be used to synchronize the AWGs with external clock domains and with minimum possible timing jitter, avoiding additional phase-locked-loops which are sometimes used by other vendor's instruments for clock synchronization. Such AWGs are widely deployed in today's optical test laboratories (like e.g. the Keysight® M8196A).

With such a connection of instruments is it possible to enhance the speed and the capabilities of different vendors AWGs[1] with one of SHF's remote head modules. This makes it possible e.g. to generate 120 GBaud PAM4 signals with Keysight's® M8196 A connected to SHF's 616 C PAM-Multiplexer.

® Keysight is a registered trademark of Keysight Technologie Inc.

[1] With SHF's BPGs or AWGs a clock distribution is not required as our instruments provide all required clock signals right away.

# Block Diagram



# Accessories

- +12 V Power Supply Desktop Adapter
- Functional Earth Cable
- Mini-USB cable

# Absolute Maximum Ratings

| Parameter | Unit | Symbol | Min. | Typ. | Max. | Comment |
|---|---|---|---|---|---|---|
| **Input Parameters** | | | | | | |
| Input Amplitude | mV | $V_{Clk\ in}$ | | | 1000 | Peak-to-Peak |
| External DC Voltage on RF Input Port | V | $V_{DC\ in}$ | -6 | | +6 | AC coupled port |
| External DC Voltage on RF Output Ports | V | $V_{DC\ out}$ | -6 | | +6 | AC coupled ports |
| DC Supply Voltage | V | $V_{cc}$ | 0 | | +14 | |

# Specifications – SHF C991 A

| Parameter | Unit | Symbol | Min. | Typ. | Max. | Comment |
|---|---|---|---|---|---|---|
| **Input Frequency** | | | | | | |
| Minimum Input Frequency | GHz | $f_{in\ min}$ | | | 4 | $N_1 \leq 20$ |
| Maximum Input Frequency | GHz | $f_{in\ max}$ | 48<br>64 | | | $N_1 = 1$<br>$N_1 \geq 2$ |
| **Input Amplitude** | | | | | | |
| Input Amplitude | $mV_{pp}$ | $V_{in}$ | 200 | 600 | 900 | AC coupled<br>Single ended |
| **Output Frequency** | | | | | | |
| Clock Out | GHz | $f_{out}$ | 4 | | 64 | $f_{in}$ |
| Clock /2 Out | GHz | $f_{out}$ | 2 | | 32 | $f_{in}$ /2 |
| Clock $DIV_1$ Out | GHz | $f_{out}$ | 0.10 | | 24 | $f_{in}$ /(2×$N_1$)<br>$N_1$ = 1…127 |
| Clock $DIV_2$ Out | GHz | $f_{out}$ | 0.05 | | 3 | $f_{in}$ /(2×$N_1$×$N_2$)<br>$N_2$ = 1,2,4,8 |
| **Output Amplitude** | | | | | | |
| Clock Out | $mV_{pp}$ | $V_{out}$ | 300 | | 700 | AC coupled<br>Single ended |
| Clock /2 Out | $mV_{pp}$ | $V_{out}$ | 600 | | 900 | AC coupled<br>Single ended |
| Clock $DIV_1$ Out | $mV_{pp}$ | $V_{out}$ | 500 | | 900 | AC coupled<br>Single ended |
| Clock $DIV_2$ Out | $mV_{pp}$ | $V_{out}$ | 600 | | 900 | AC coupled<br>Single ended |

# Specifications – SHF C991 A

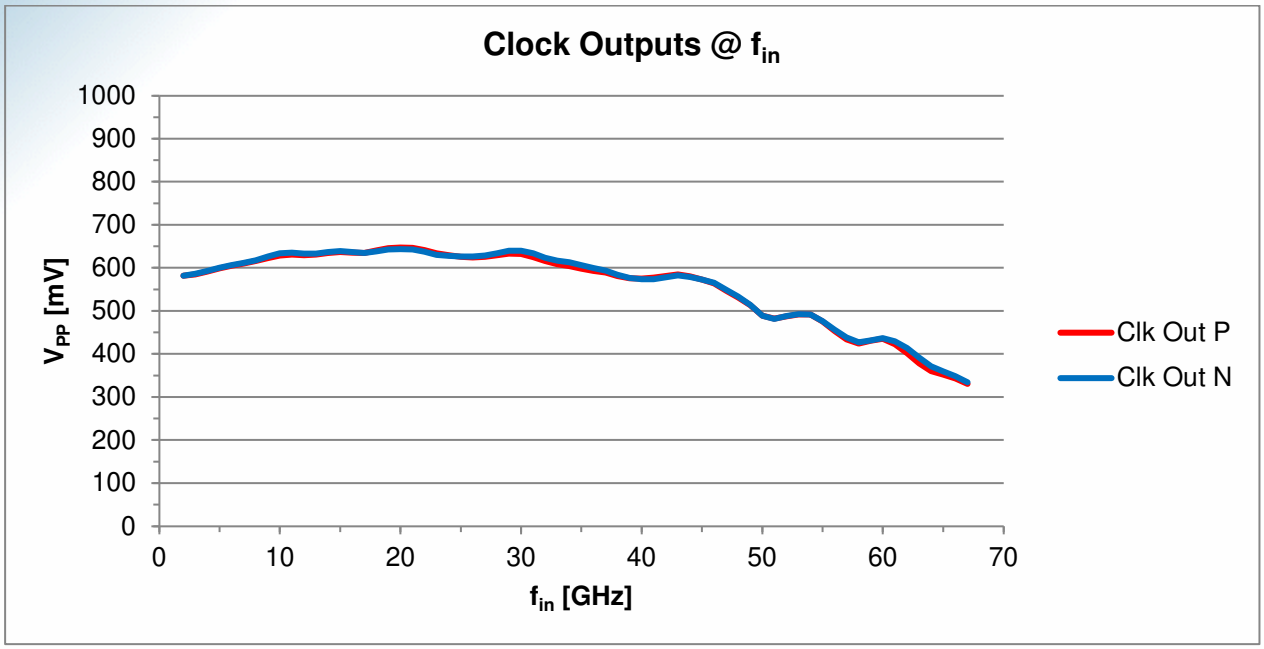
| Parameter | Unit | Symbol | Min. | Typ. | Max. | Comment |
|---|---|---|---|---|---|---|
| **Power Requirement** | | | | | | |
| Supply Voltage | V | $V_{cc}$ | +11.5 | +12.0 | +12.5 | |
| Supply Current | A | $I_{cc}$ | | 0.69<br>0.95 | | Without heat sink<br>With heat sink |
| Power Dissipation | W | $P_d$ | | 8.3<br>11.4 | | Without heat sink<br>With heat sink<br>@ $V_{CC}$ = +12 V |
| **Integrated Fan Control**[2] | | | | | | |
| Output Voltage Fan | V | $V_{Fan+12V}$ | | +12 | | |
| Output Current Fan | A | $I_{Fan+12V}$ | | 0.26 | | |
| Output Frequency Fan | Hz | $f_{Fan+12V}$ | | 30 | | |
| Input Tacho Fan | V | $V_{Fan\ Tacho}$ | | 3.3 | | |
| **Mechanical Characteristics** | | | | | | |
| Clock In | Ω | | | 50 | | 1.85 mm (V) female |
| Clock Out | Ω | | | 50 | | 1.85 mm (V) female |
| Clock /2 Out | Ω | | | 50 | | 2.92 mm (K) female |
| Clock $DIV_1$ Out | Ω | | | 50 | | 2.92 mm (K) female |
| Clock $DIV_2$ Out | Ω | | | 50 | | 2.92 mm (K) female |
| Dimensions | mm | | | | | See Outline Drawing<br>pages 17 / 18 |
| Weight | g | | | 190<br>480 | | Without heat sink<br>With heat sink |
| **Conditions** | | | | | | |
| Operating Temperature | °C | $T_{ambient}$ | 15 | | 35 | |

[2] Use only with the supplied heat sink and fan!

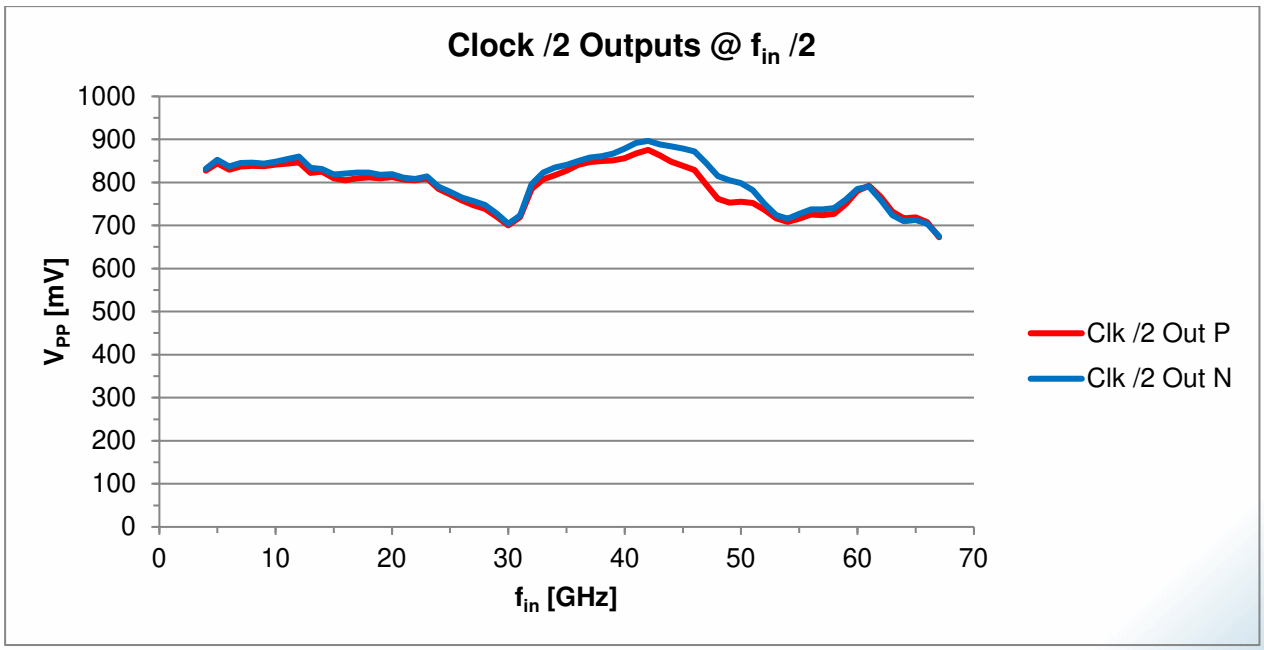
# Typical Output Amplitudes @ 2.0 GHz ≤ Clk DIV$_2$ ≤ 3.0 GHz

The measurements below have been performed using an Anritsu® signal generator (MG3697C) and a Tektronix® Digital Serial Analyzer (DSA8300) with a Phase Reference Module (82A04B-60G) and a 70 GHz Sampling Module (80E11). The outputs of the Clock distribution module had been connected directly to the DSA input. Input power of the clock signal is 0 dBm (630 mV$_{pp}$).

## Clock Outputs




## Clock /2 Outputs

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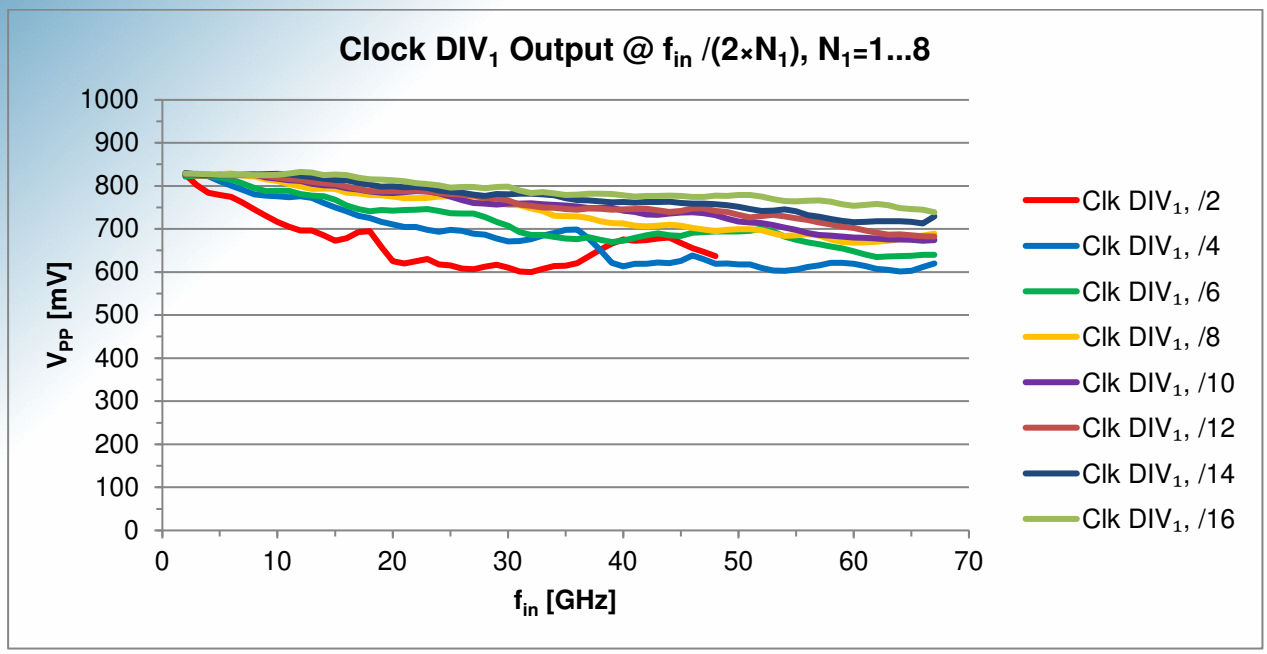
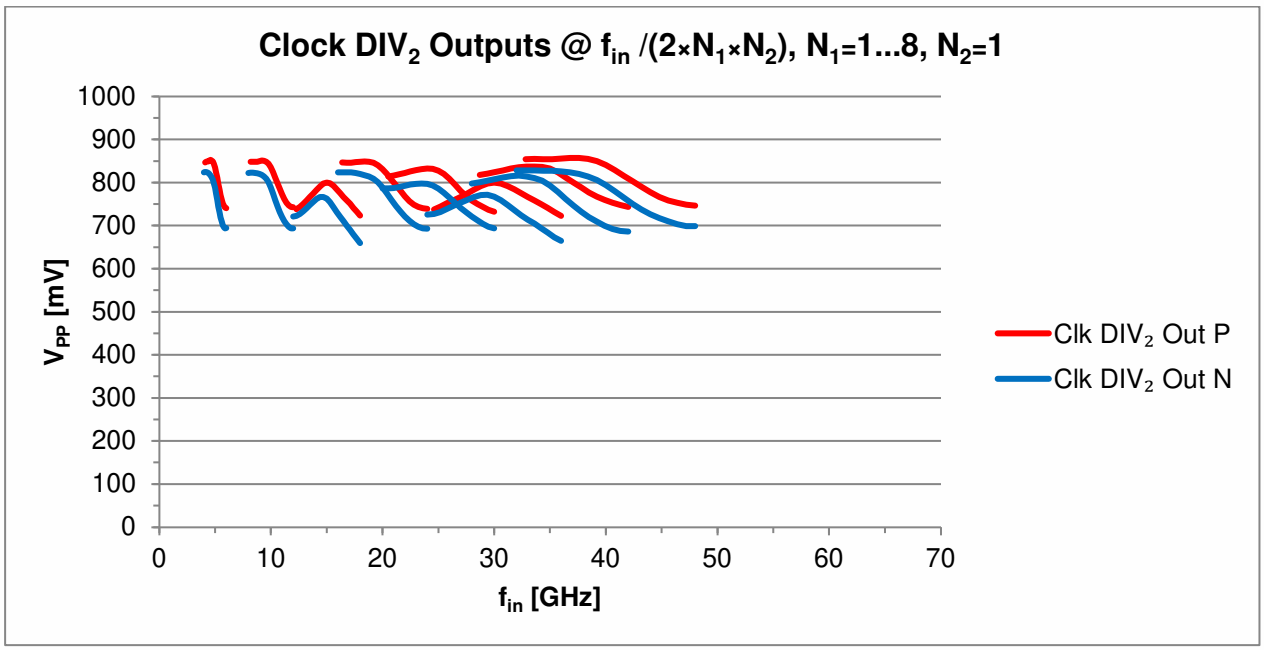
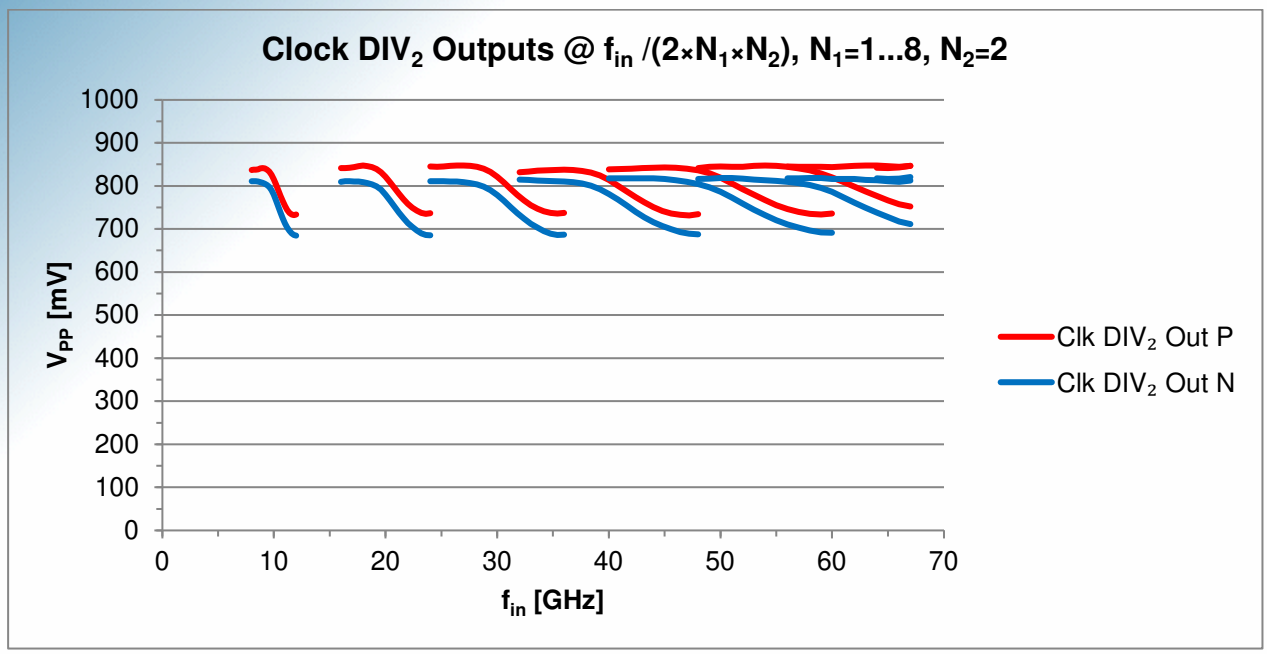
## Clock DIV$_1$ Output, N$_1$=1…8



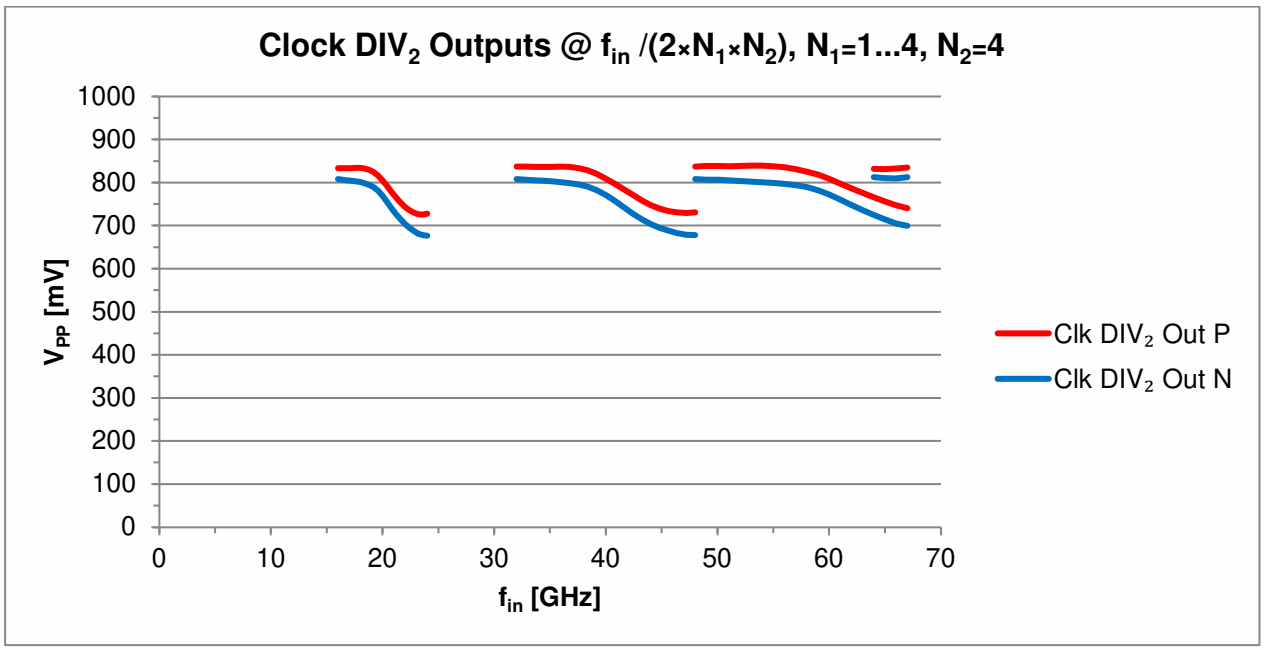

## Clock DIV$_2$ Outputs, N$_2$=1



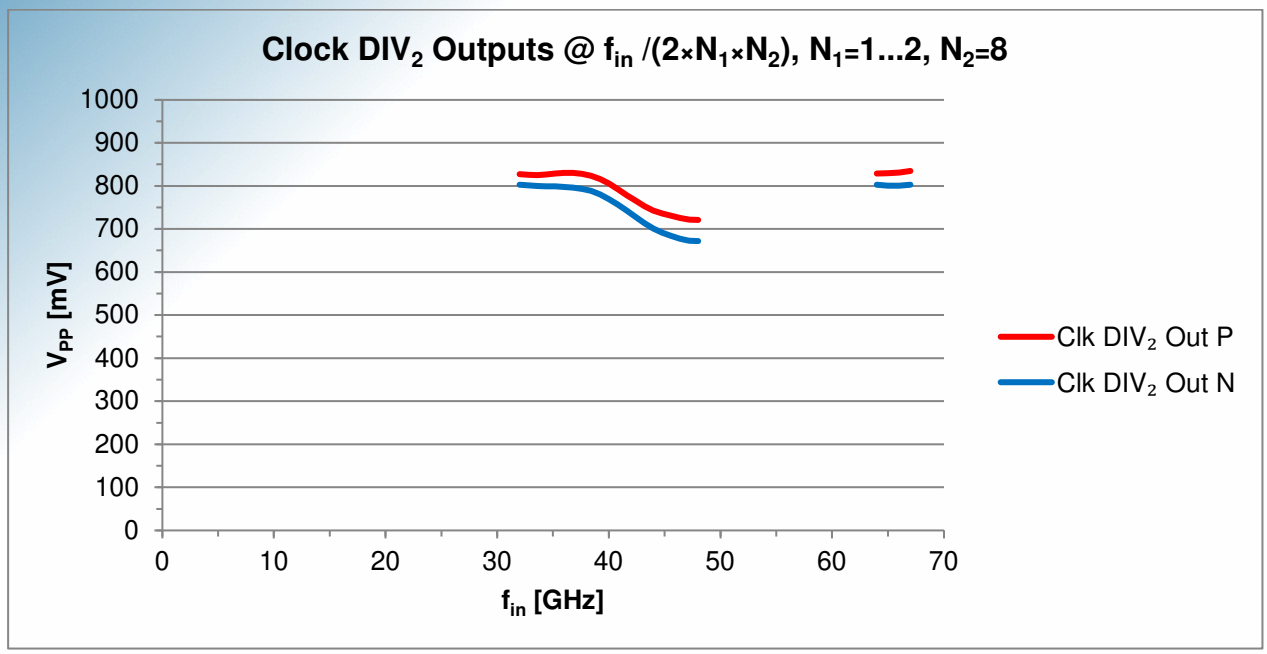
## Clock DIV2 Outputs, N2=2




## Clock DIV2 Outputs, N2=4



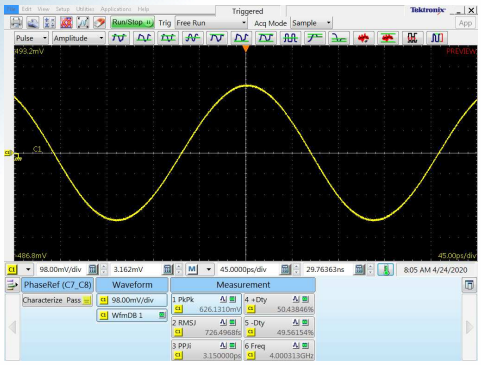
## Clock DIV$_2$ Outputs, N$_2$=8



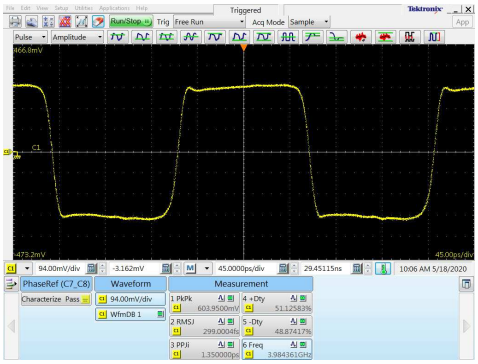
# Typical Output Waveforms @ 2.0 GHz ≤ Clk DIV$_2$ ≤ 3.0 GHz

The measurements below have been performed using an Anritsu® signal generator (MG3697C) and a Tektronix® Digital Serial Analyzer (DSA8300) with a Phase Reference Module (82A04B-60G) and a 70 GHz Sampling Module (80E11). The outputs of the Clock distribution module had been connected directly to the DSA input. Input power of the clock signal is 0 dBm (630 mV$_{pp}$).

## Clock Outputs @ 4.0 GHz Clock Input



**4.0 GHz input signal**



**4.0 GHz output signal @ Clk Out**

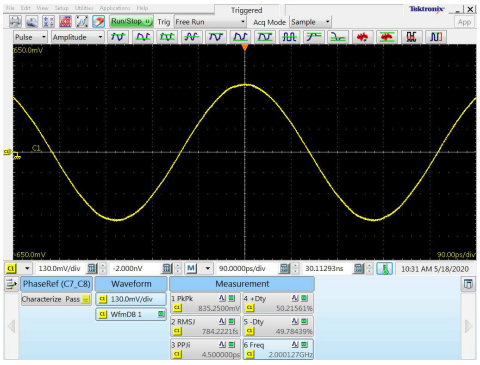
$f_{out} = f_{in}$

**2.0 GHz output signal @ Clk /2 Out**

$f_{out} = f_{in} /2$

**2.00 GHz output signal @ Clk DIV$_1$ Out**

$f_{out} = f_{in} /(2 \times N_1)$, $N_1=1$



**2.00 GHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1=1$, $N_2=1$

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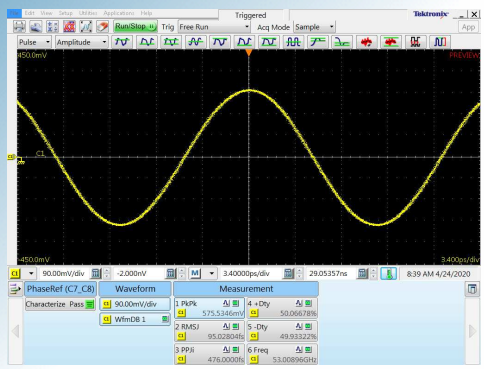
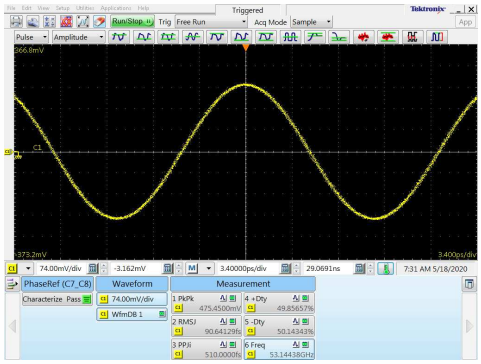
## Clock Outputs @ 53.0 GHz Clock Input

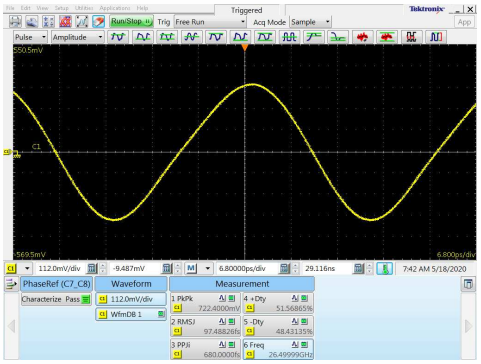


**53.0 GHz input signal**



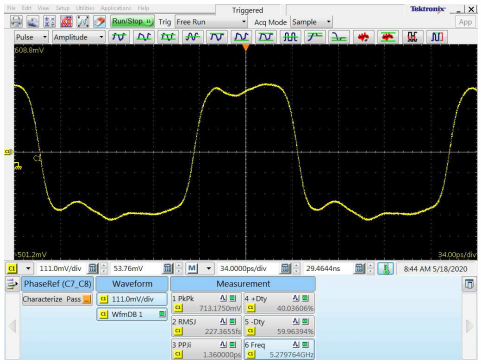
**53.0 GHz output signal @ Clk Out**

$f_{out} = f_{in}$



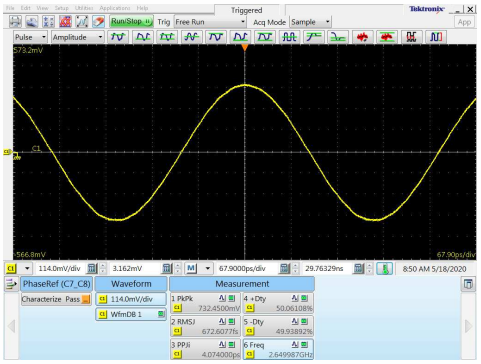
**26.5 GHz output signal @ Clk /2 Out**

$f_{out} = f_{in} / 2$



**5.30 GHz output signal @ Clk DIV$_1$ Out**

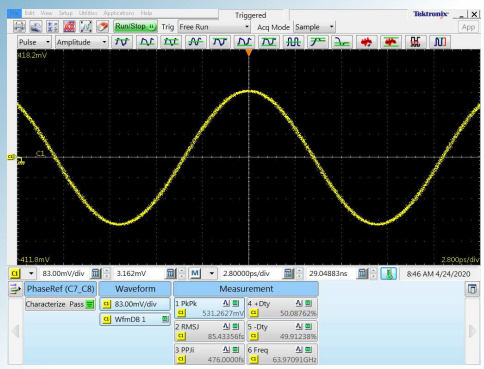
$f_{out} = f_{in} / (2 \times N_1)$, $N_1=5$



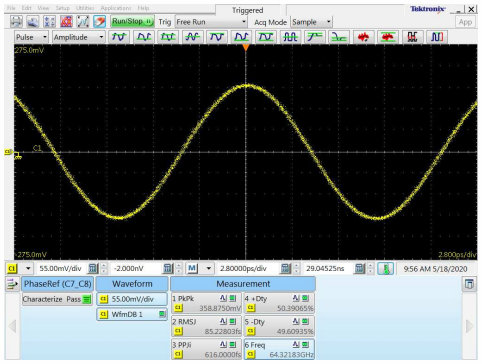
**2.65 GHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} / (2 \times N_1 \times N_2)$, $N_1=5$, $N_2=2$

## Clock Outputs @ 64.0 GHz Clock Input

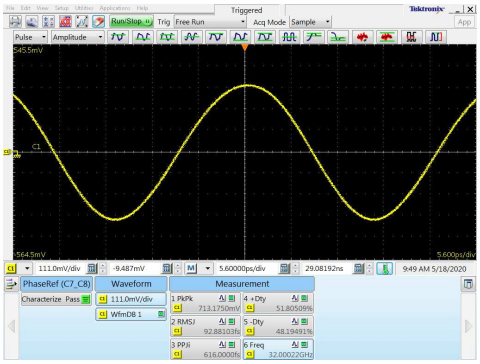


**64.0 GHz input signal**



**64.0 GHz output signal @ Clk Out**

$f_{out} = f_{in}$

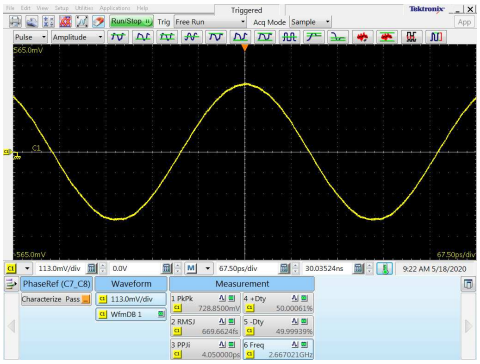


**32.0 GHz output signal @ Clk /2 Out**

$f_{out} = f_{in} /2$

**5.33 GHz output signal @ Clk DIV$_1$ Out**

$f_{out} = f_{in} /(2 \times N_1)$, $N_1=6$



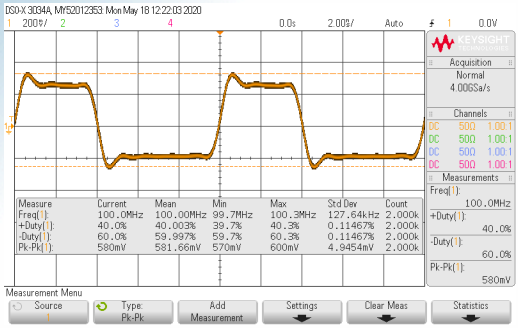
**2.67 GHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1=6$, $N_2=2$

# Typical Output Waveforms @ Clk DIV$_2$ < 2.0 GHz

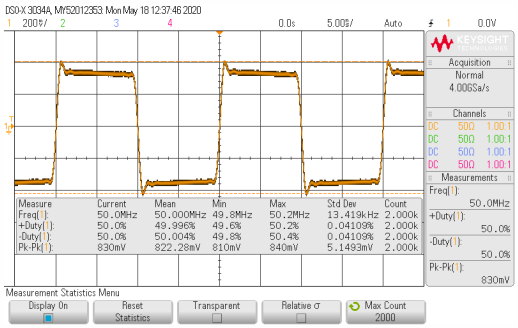
The measurements below have been performed using an Anritsu® signal generator (MG3697C) and a Keysight® Digital Storage Oscilloscope (DSO-X 3034A). The outputs of the Clock distribution module had been connected directly to the DSO input. Input power of the clock signal is 0 dBm (630 mV$_{pp}$).

## Clock Outputs @ 4.0 GHz Clock Input, N$_1$=20




**100 MHz output signal @ Clk DIV$_1$ Out**

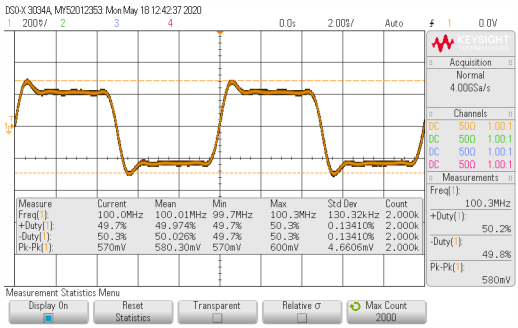
$f_{out} = f_{in} /(2 \times N_1)$, $N_1$=20




**50 MHz output signal @ Clk DIV$_2$ Out**

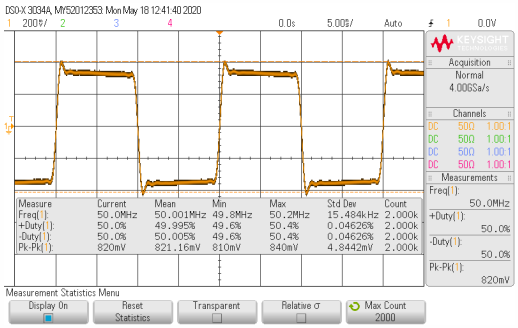
$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=20, $N_2$=2

## Clock Outputs @ 6.4 GHz Clock Input, N$_1$=32




**100 MHz output signal @ Clk DIV$_1$ Out**

$f_{out} = f_{in} /(2 \times N_1)$, $N_1$=32




**50 MHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=32, $N_2$=2

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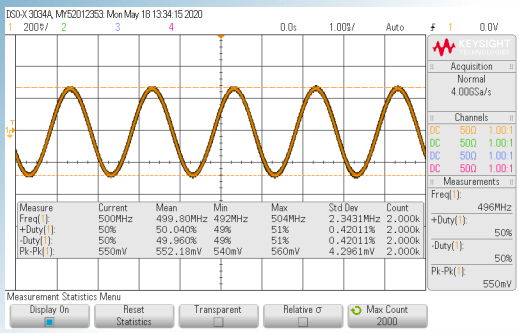
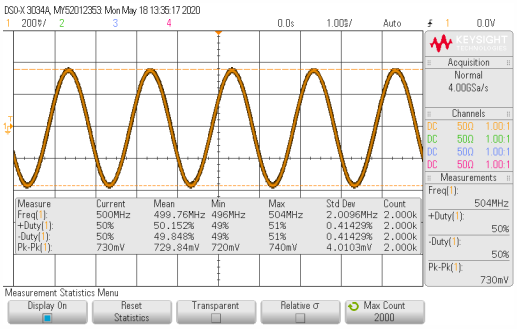
## Clock Outputs @ 64.0 GHz Clock Input, $N_1$=64



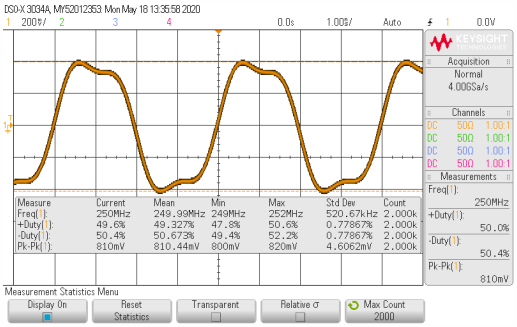

**500 MHz output signal @ Clk DIV$_1$ Out**

$f_{out} = f_{in} /(2 \times N_1)$, $N_1$=64



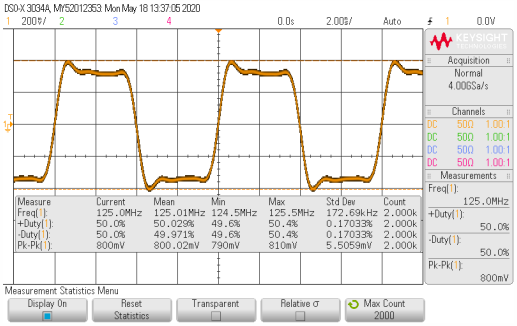

**500 MHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=64, $N_2$=1



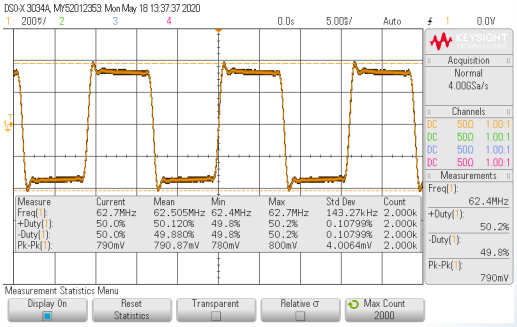

**250 MHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=64, $N_2$=2




**2.67 MHz output signal @ Clk DIV$_2$ Out**

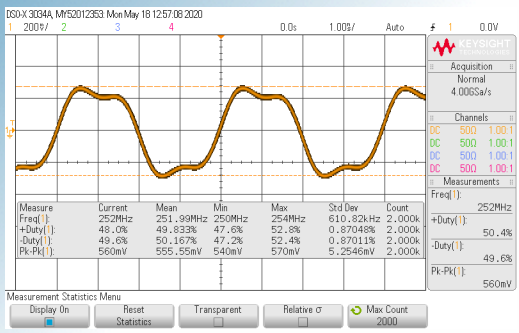
$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=64, $N_2$=4




**62.5 MHz output signal @ Clk DIV$_2$ Out**

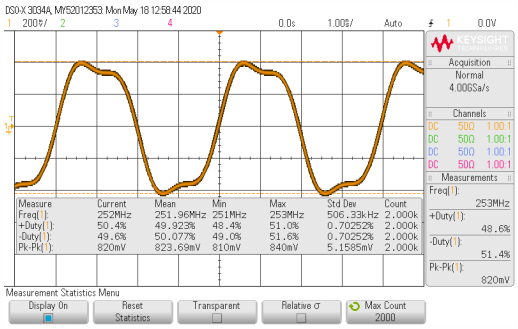
$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=64, $N_2$=8

## Clock Outputs @ 64.0 GHz Clock Input, $N_1$=127



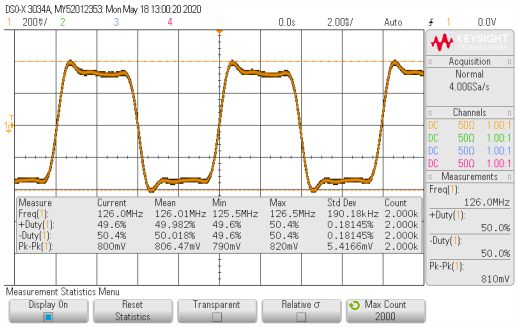

**251.97 MHz output signal @ Clk DIV$_1$ Out**

$f_{out} = f_{in} /(2 \times N_1)$, $N_1$=127



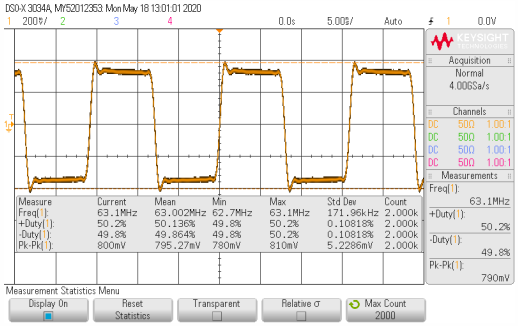

**251.97 MHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=127, $N_2$=1




**125.98 MHz output signal @ Clk DIV$_2$ Out**

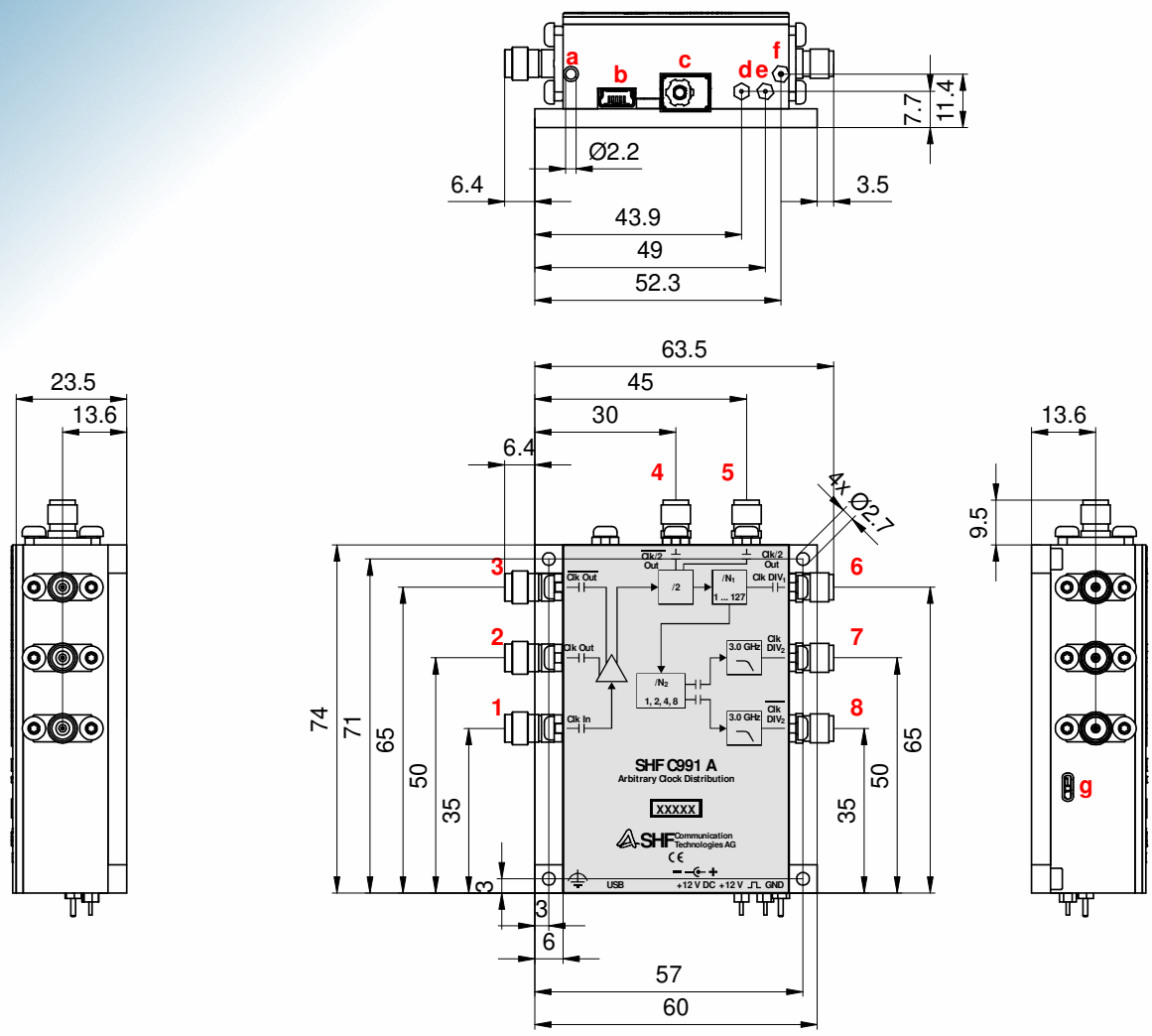
$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=127, $N_2$=2




**62.99 MHz output signal @ Clk DIV$_2$ Out**

$f_{out} = f_{in} /(2 \times N_1 \times N_2)$, $N_1$=127, $N_2$=4

# Mechanical Drawing

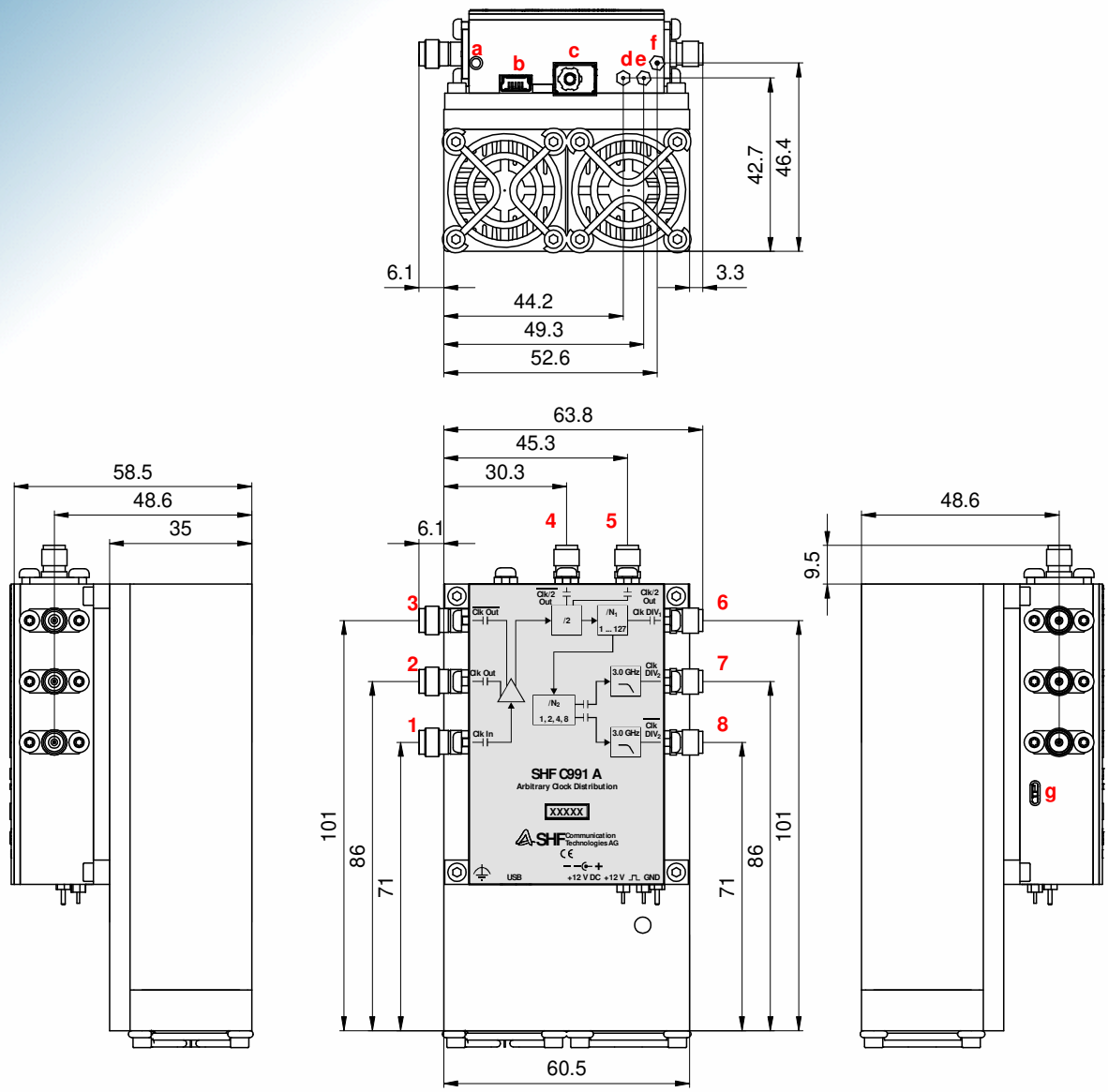



| Pos | Port | Connector |
|---|---|---|
| 1 | Clock In | 1.85mm (V) female |
| 2 | Clock Out | 1.85mm (V) female |
| 3 | $\overline{\text{Clock Out}}$ | 1.85mm (V) female |
| 4 | $\overline{\text{Clock/2 Out}}$ | 2.92mm (K) female |
| 5 | Clock/2 Out | 2.92mm (K) female |
| 6 | Clock $DIV_1$ | 2.92mm (K) female |
| 7 | Clock $DIV_2$ | 2.92mm (K) female |
| 8 | $\overline{\text{Clock DIV}_2}$ | 2.92mm (K) female |

| Port | Connector |
|---|---|
| a | Functional earth (FE) |
| b | Mini-USB |
| c | Power |
| d | Fan+12V |
| e | Fan Tacho |
| f | GND |
| g | Service |

all dimensions in mm

# Mechanical Drawing




| Pos | Port | Connector |
|---|---|---|
| 1 | Clock In | 1.85mm (V) female |
| 2 | Clock Out | 1.85mm (V) female |
| 3 | $\overline{\text{Clock Out}}$ | 1.85mm (V) female |
| 4 | $\overline{\text{Clock/2 Out}}$ | 2.92mm (K) female |
| 5 | Clock/2 Out | 2.92mm (K) female |
| 6 | Clock $DIV_1$ | 2.92mm (K) female |
| 7 | Clock $DIV_2$ | 2.92mm (K) female |
| 8 | $\overline{\text{Clock DIV}_2}$ | 2.92mm (K) female |

| Port | Connector |
|---|---|
| a | Functional earth (FE) |
| b | Mini-USB |
| c | Power |
| d | Fan+12V |
| e | Fan Tacho |
| f | GND |
| g | Service |

all dimensions in mm