SHF Communication Technologies AG

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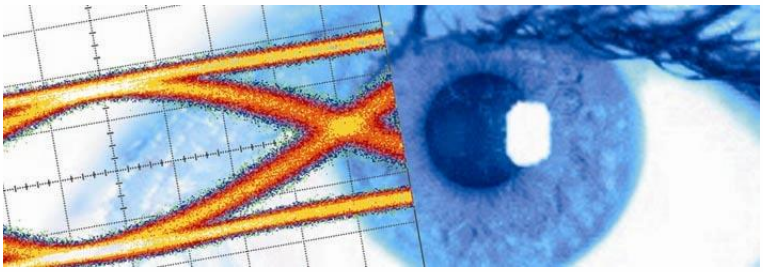
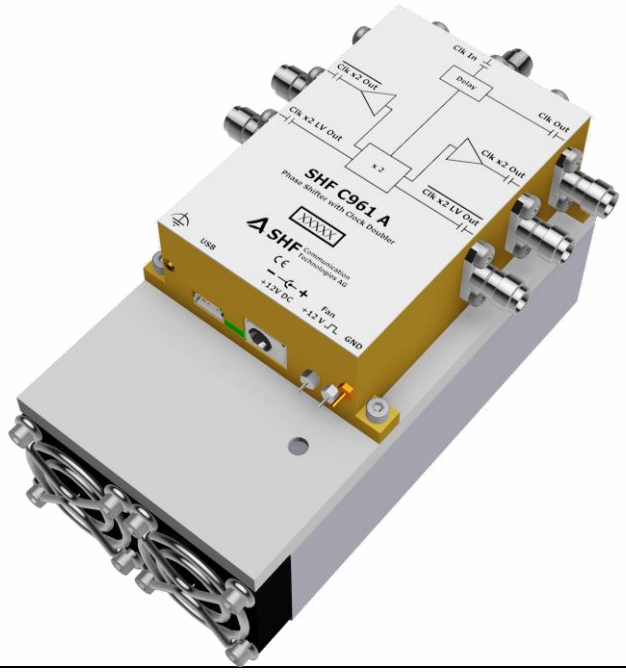


Datasheet

SHF C961 A

Phase Shifter with Clock-Doubler



Description

The SHF C961 A is a broadband digital controlled delay line plus a broad band clock distribution.

The delay line features a maximum delay of 70 ps with 100 fs resolution. This phase-controlled signal is provided at five outputs:

- One output at the input frequency
- Two outputs at double the input frequency
- Two amplified outputs at double the input frequency (level-controlled)

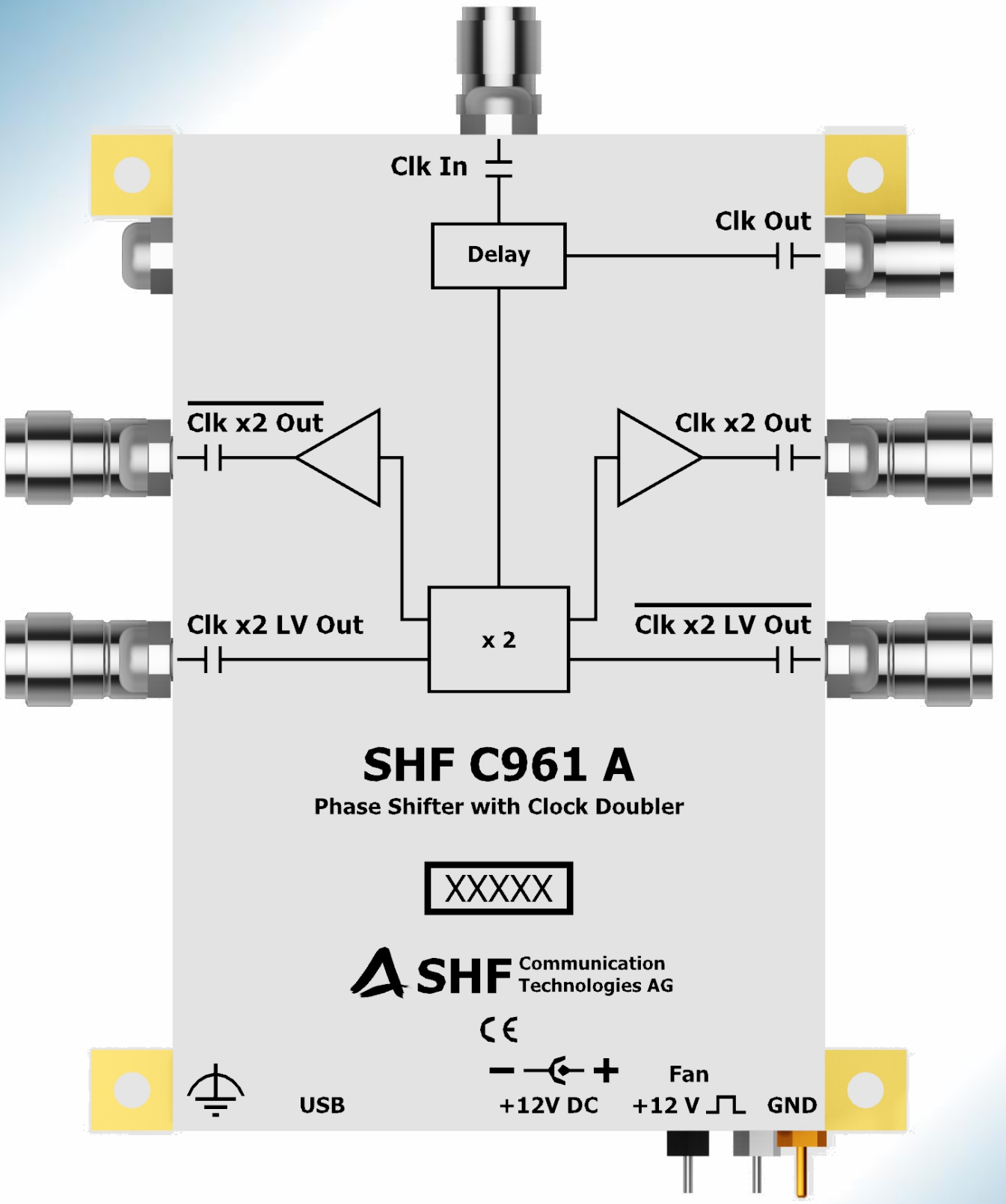
Features

- Broadband 70ps Delay Line with a 100 fs step size operating from 2 GHz up to 67 GHz
- Several outputs with different functionality
- Controlled by intuitive graphical user interface SHF Control Center (SCC) via USB
- Controlled by intuitive graphical user interface BERT Control Center (BCC) via USB

Applications

- Computer controlled phase adjustments of clock signals up to 67 GHz
- Clock signal distribution in high-speed telecom setups
- Precise delay control for automated measurements

Block Diagram



Accessories

- +12 V Power Supply Desktop Adapter
- Functional Earth Cable
- Mini-USB cable

Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Input Amplitude	mV	$V_{Clk\ in}$			1000	Peak-to-Peak
External DC Voltage on RF Input Port	V	$V_{DC\ in}$	-6		+6	AC coupled port
External DC Voltage on RF Output Ports	V	$V_{DC\ out}$	-6		+6	AC coupled ports
DC Supply Voltage	V	V_{cc}	0		+14	

Specifications – SHF C961 A

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Delay						
Adjustable Delay	ps		0		70	
Step Size	fs			100		
Input Frequency						
CLK In	GHz	f_{in}	2		35	
Input Amplitude						
Input Amplitude	mV_{pp}	V_{in}	200	450	900	AC coupled Single ended
Output Frequency						
CLK Out	GHz	f_{out}	2		35	f_{in}
CLK x2 Out	GHz	f_{out}	30		60	f_{in} x2
CLK x2 LV Out	GHz	f_{out}	30		67	f_{in} x2
Output Amplitude						
CLK Out	mV_{pp}	V_{out}	500		850	AC coupled Single ended
CLK x2 Out	mV_{pp}	V_{out}	680		1100	AC coupled Single ended
CLK x2 LV Out	mV_{pp}	V_{out}	250		650	AC coupled Single ended

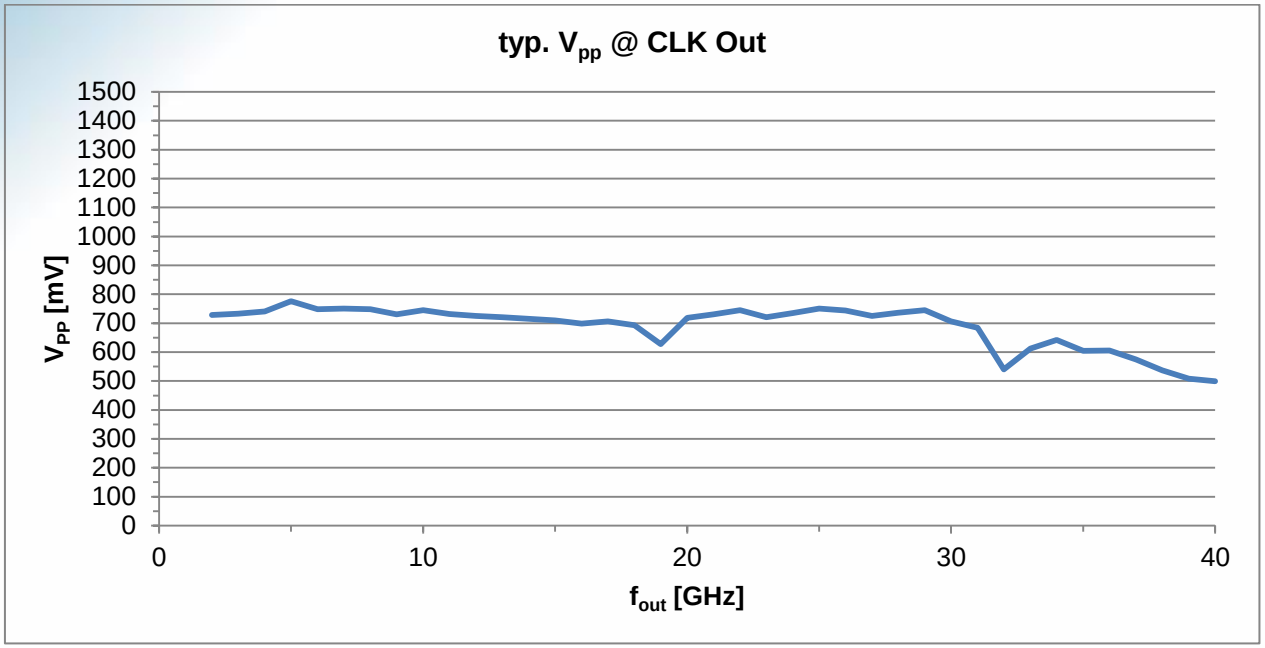
Specifications – SHF C991 A

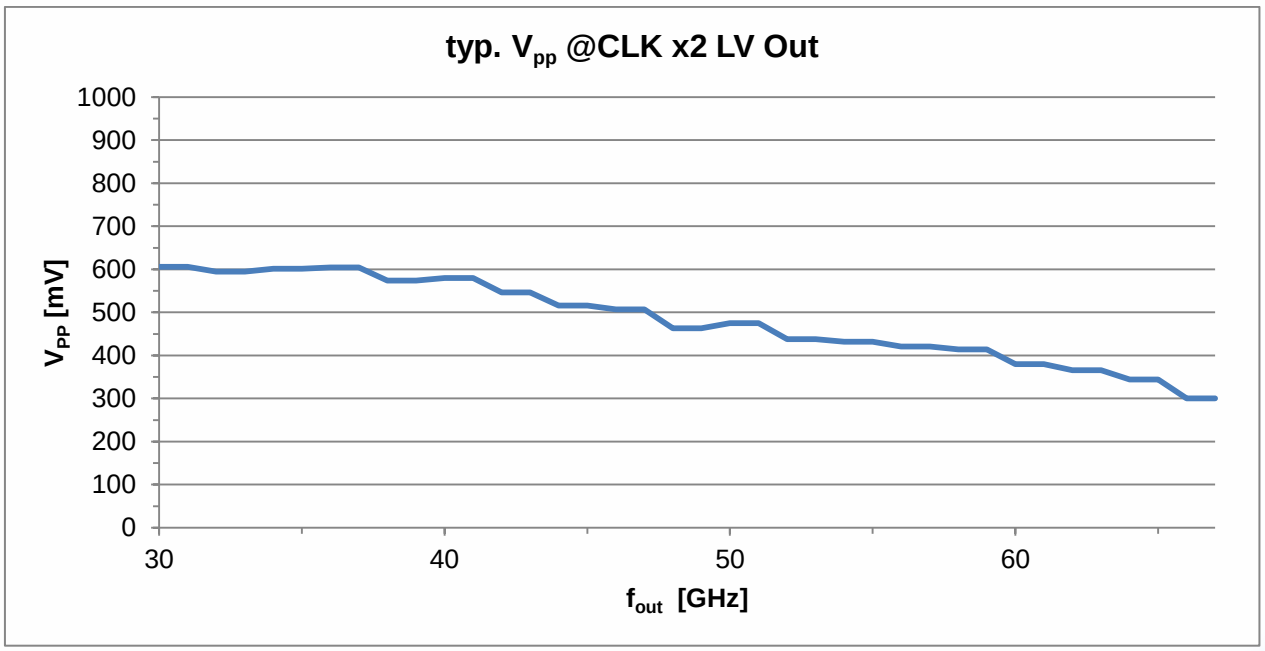
Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Power Requirement						
Supply Voltage	V	V_{cc}	+11.5	+12.0	+12.5	
Supply Current	A	I_{cc}		1.2 1.5		Without heat sink With heat sink+fan
Power Dissipation	W	P_d		14.4 18		Without heat sink With heat sink+fan @ V_{CC} = +12 V
Integrated Fan Control[1]						
Output Voltage Fan	V	$V_{Fan+12V}$		+12		
Output Current Fan	A	$I_{Fan+12V}$		0.26		
Output Frequency Fan	Hz	$f_{Fan+12V}$		30		
Input Tacho Fan	V	$V_{Fan\ Tacho}$		3.3		
Mechanical Characteristics						
Clock In	Ω			50		2.92 mm (K) female
CLK Out	Ω			50		2.92 mm (K) female
CLK x2 Out	Ω			50		1.85 mm (V) female
CLK x2 LV Out	Ω			50		1.85 mm (V) female
Dimensions	mm					See Outline Drawing pages 12 / 13
Weight	g			162 480		Without heat sink With heat sink+fan
Conditions						
Operating Temperature	°C	$T_{ambient}$	15		35	

[1] Use only with the supplied heat sink and fan!

Typical Output Amplitudes

The measurements below have been performed using an Anritsu® signal generator (MG3697C) and an Agilent® Digital Communication Analyzer (86100A) with a 70 GHz Sampling Module (86118A) and a Time Base (86107A). The outputs of the module had been connected directly to the DCA input. Input power of the clock signal is 0 dBm (630 mV_{pp}) .





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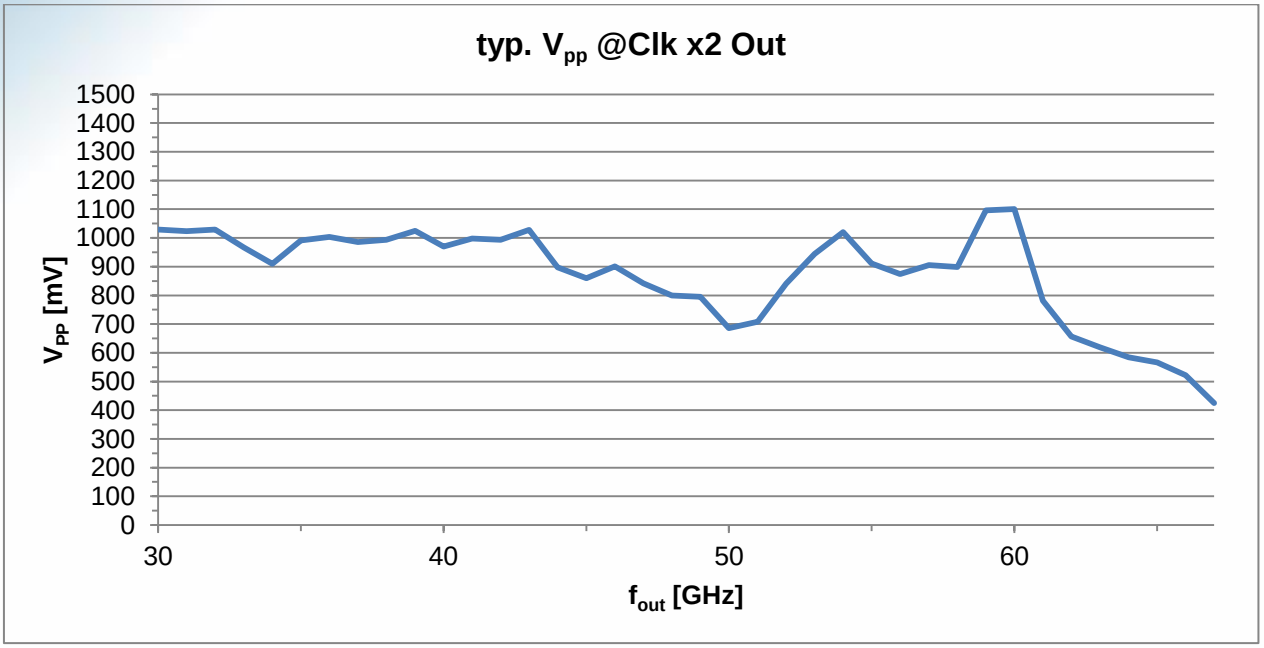

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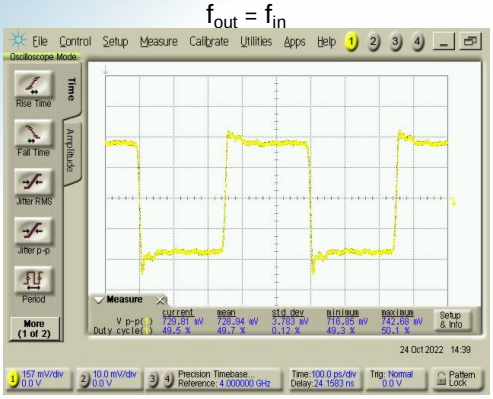
Typical Output Waveforms @ CLK Out

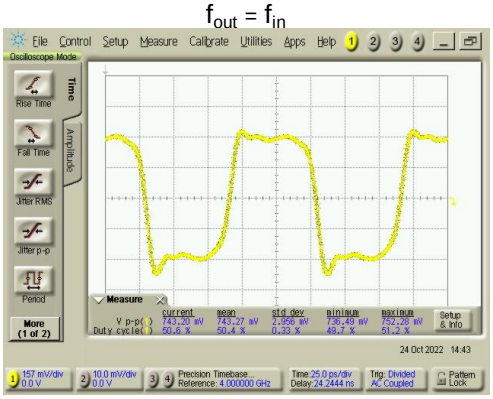
The measurements below have been performed using an Anritsu® signal generator (MG3697C) and an Agilent® Digital Communication Analyzer (86100A) with a 70 GHz Sampling Module (86118A) and a Time Base (86107A). The outputs of the module had been connected directly to the DCA input. Input power of the clock signal is 0 dBm (630 mV_{pp}).

$f_{out} = f_{in}$



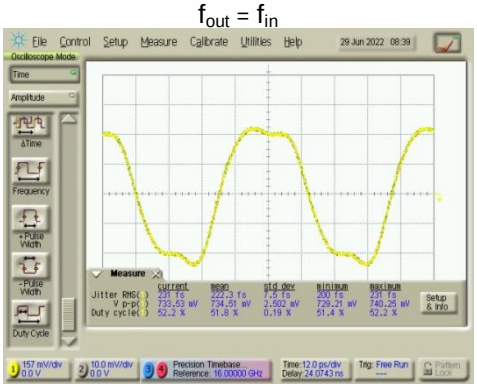
2 GHz Output signal

$f_{out} = f_{in}$



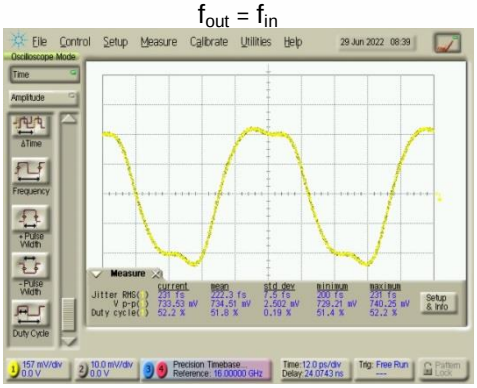
8 GHz output signal

$f_{out} = f_{in}$



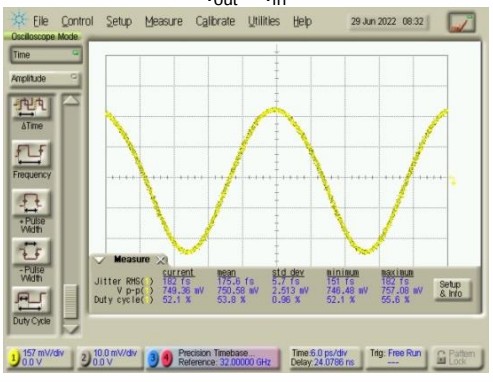
16 GHz output signal

$f_{out} = f_{in}$



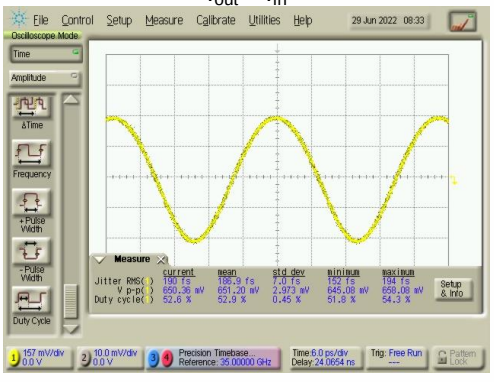
24 GHz output signal

$f_{out} = f_{in}$



32 GHz output signal

$f_{out} = f_{in}$



35 GHz output signal

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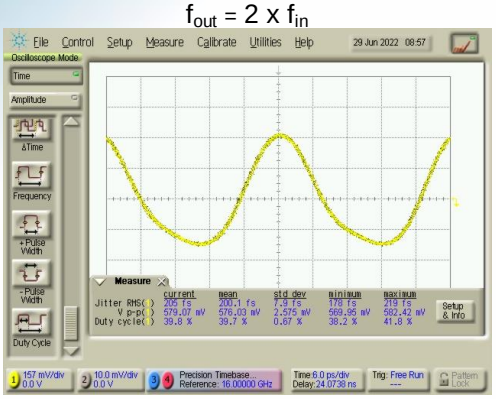
Typical Output Waveforms @ CLK x2 LV Out

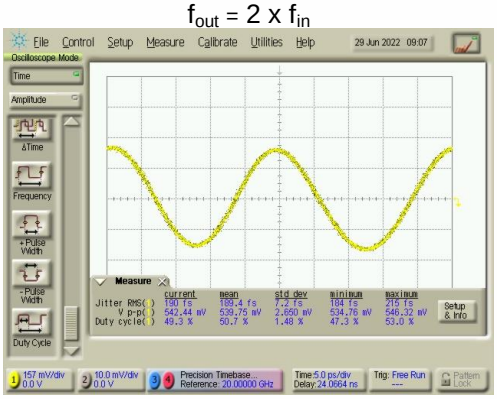
The measurements below have been performed using an Anritsu® signal generator (MG3697C) and a Agilent® Digital Communication Analyzer (86100A) with a 70 GHz Sampling Module (86118A) and a Time Base (86107A). The outputs of the module had been connected directly to the DCA input. Input power of the clock signal is 0 dBm (630 mV_{pp}).

$f_{out} = 2 \times f_{in}$



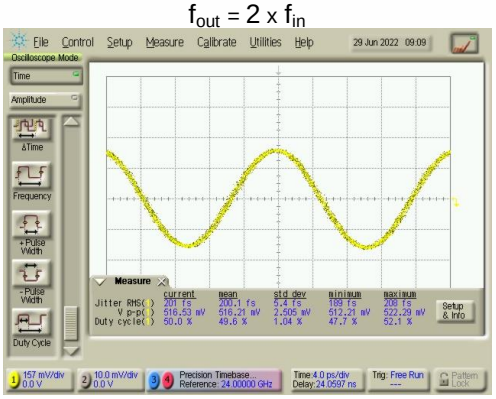
32 GHz Output signal

$f_{out} = 2 \times f_{in}$



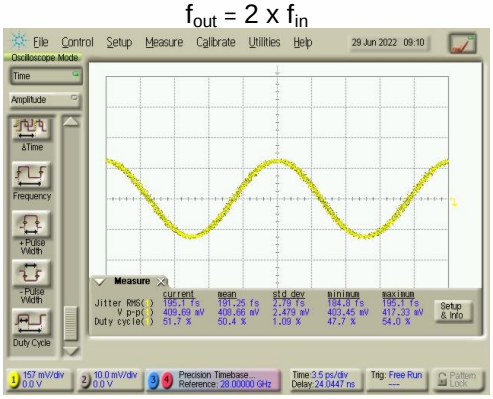
40 GHz output signal

$f_{out} = 2 \times f_{in}$



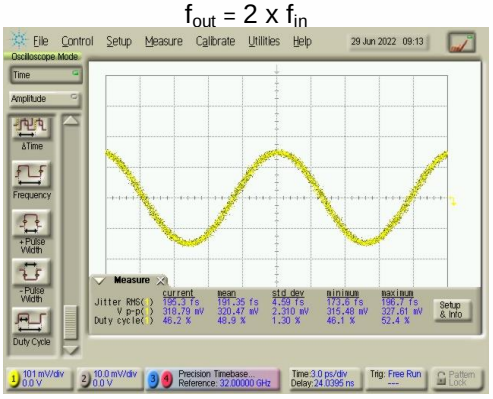
48 GHz output signal

$f_{out} = 2 \times f_{in}$



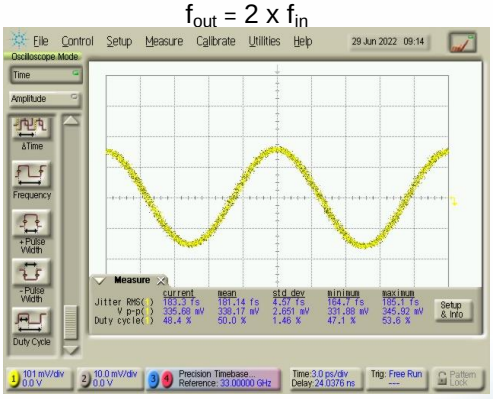
56 GHz output signal

$f_{out} = 2 \times f_{in}$



64 GHz output signal

$f_{out} = 2 \times f_{in}$



66 GHz output signal

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Typical Output Waveforms @ CLK x2 Out

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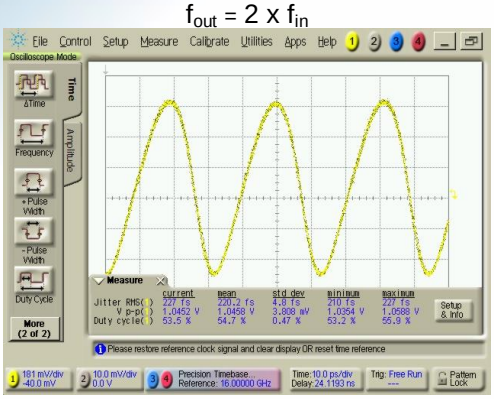
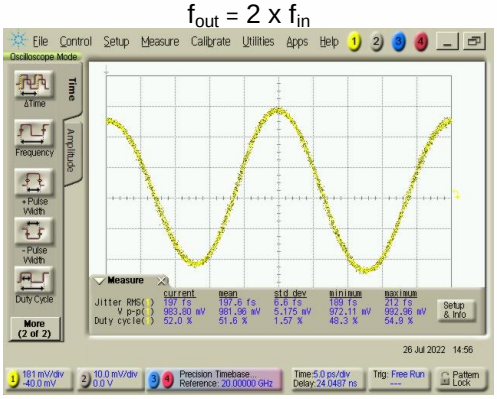
$f_{out} = 2 \times f_{in}$



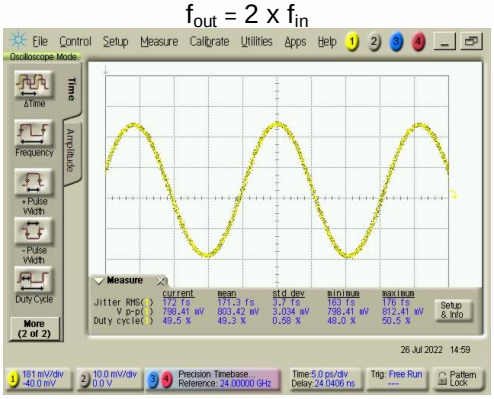
32 GHz Output signal

$f_{out} = 2 \times f_{in}$



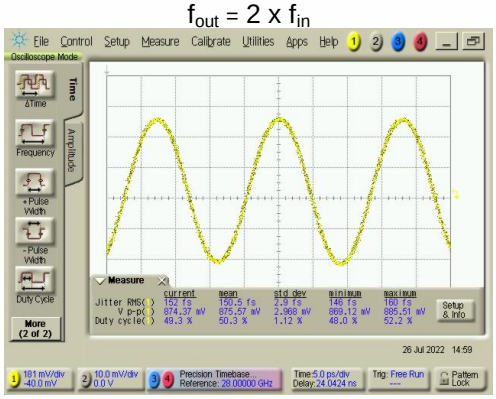
40 GHz output signal

$f_{out} = 2 \times f_{in}$



48 GHz output signal

$f_{out} = 2 \times f_{in}$



56 GHz output signal

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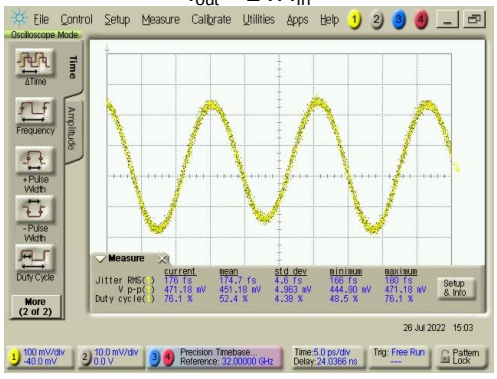

64 GHz output signal

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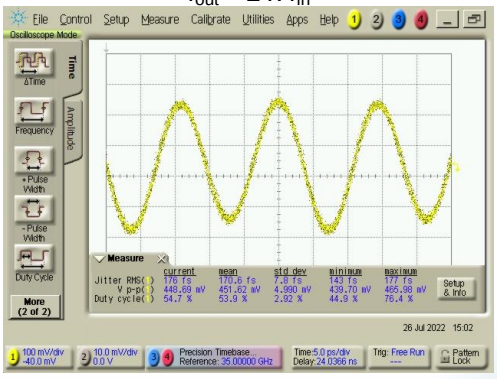

66 GHz output signal

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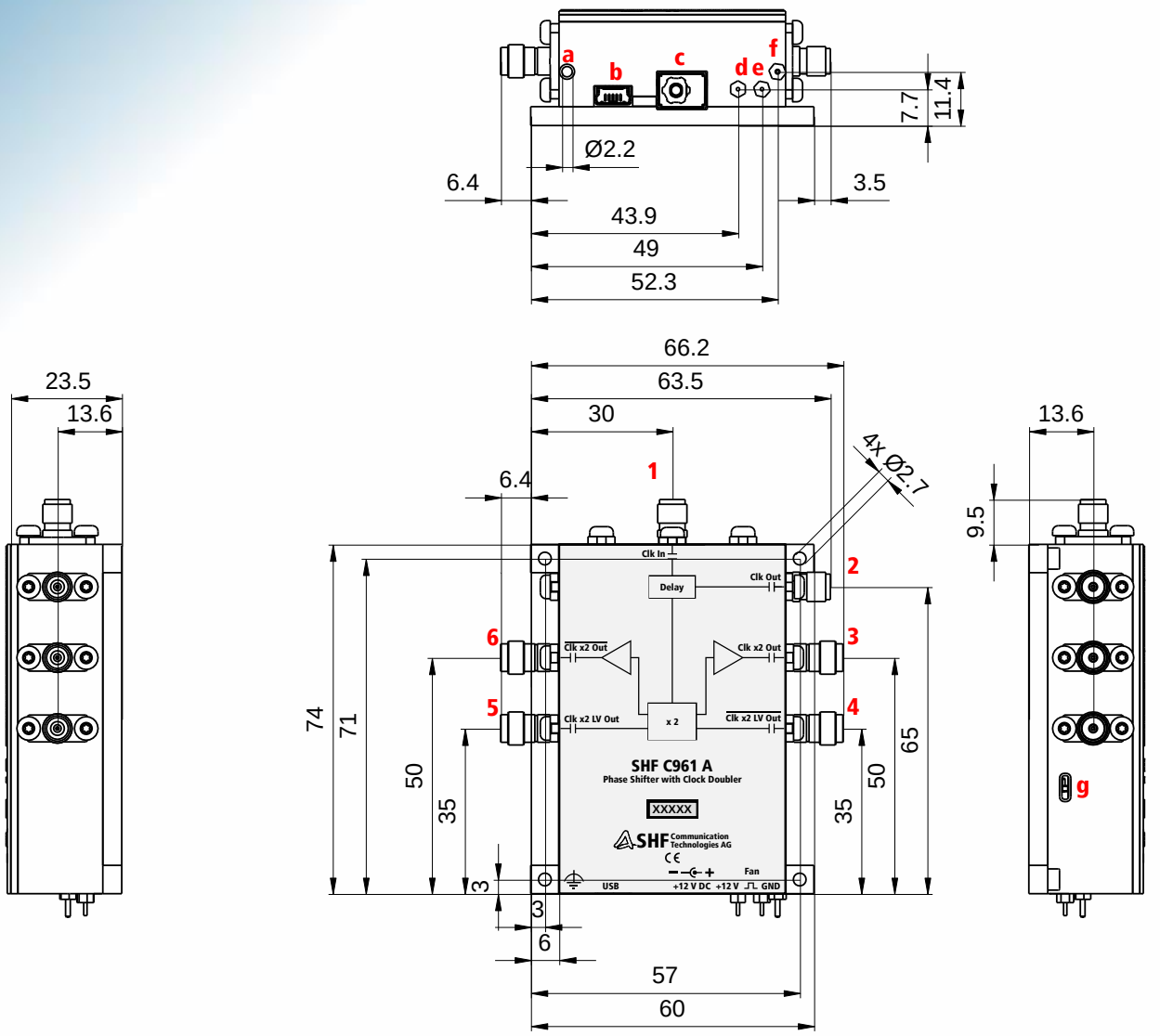
Mechanical Drawing

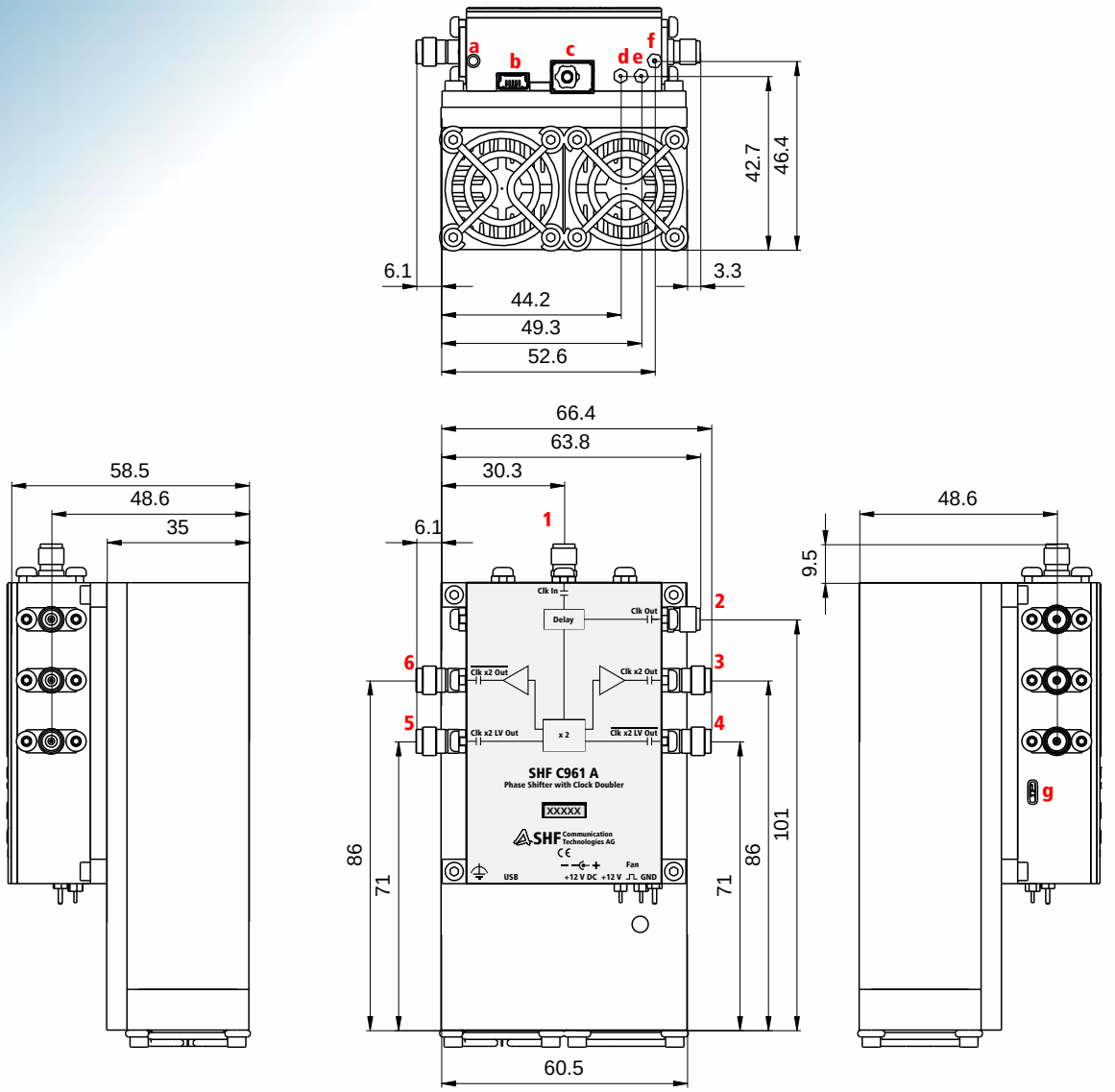


Pos	Port	Connector
1	Clk In	2.92mm (K) female
2	Clk Out	2.92mm (K) female
3	Clk x2 Out	1.85mm (V) female
4	$\overline{\text{Clk x2 LV Out}}$	1.85mm (V) female
5	Clk x2 LV Out	1.85mm (V) female
6	$\overline{\text{Clk x2 Out}}$	1.85mm (V) female

Port	Connector
a	Functional earth (FE)
b	Mini-USB
c	Power
d	Fan+12V
e	Fan Tacho
f	GND
g	Service

all dimensions in mm

Mechanical Drawing with Heat Sink



Pos	Port	Connector
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6	$\overline{\text{Clk x2 Out}}$	1.85mm (V) female

Port	Connector
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