

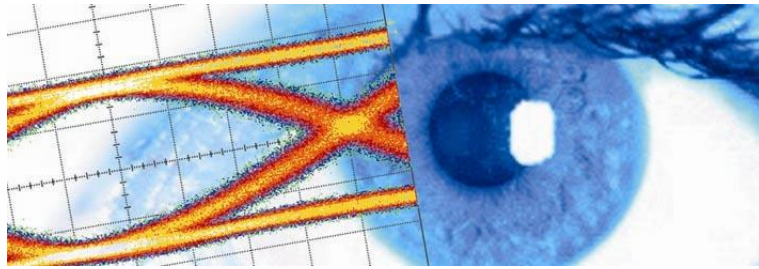


## SHF Communication Technologies AG

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# Datasheet

## SHF C623 A

### 120 Gbps

### 1:2 Demultiplexer



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## Description

The SHF C623 A is a ROHS compliant 1:2 demultiplexer (DEMUX) operating at data rates up to 120 Gbps for use in broadband test setups and telecom transmission systems. It is the ideal counterpart to the SHF C603 A (MUX).

One single ended or differential serial data stream is accepted by the demultiplexer and converted into two single ended data signals at a output data rate of 60 Gbps. A single-ended clock signal with a frequency half of the input data rate drives the SHF C623 A. All RF in- and output ports are AC-coupled and internally terminated with 50 Ohm to GND. Unused in- or output ports should be terminated with 50 Ohm.

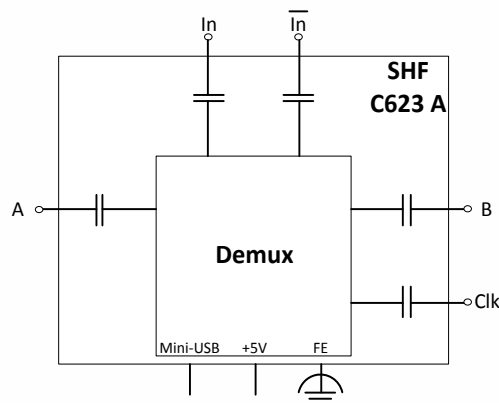
## Features

- Broadband operation up to 120 Gbps
- Differential data input
- Data Input Sensitivity <100 mV (single ended)
- Single ended data outputs

## Applications

- 100G, 200G, 400G and 1T system evaluation & development
- Telecom transmission
- Broadband test and measurement equipment

## Block Diagram



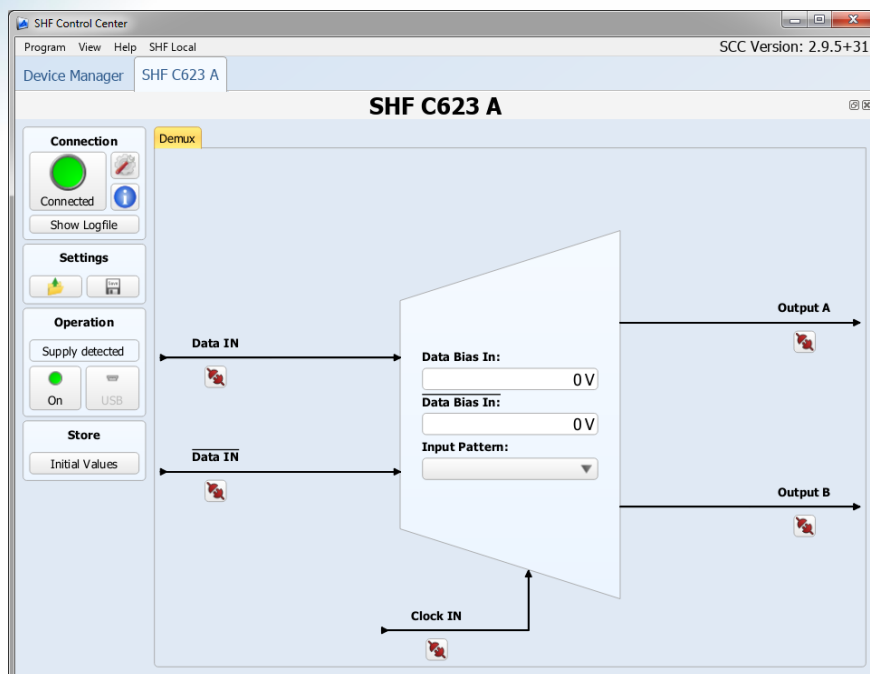
## Accessories

- +5V Power Supply Desktop Adapter
- Functional earth cable
- Mini-USB cable



## Remote Interface & Software

The DEMUX is controlled by the easy to use software package SHF Control Center (SCC). The DC input threshold voltages (Data / Inverted Data Bias) can be set and are displayed in the graphical user interface (GUI).



SHF Control Center (SCC)

## Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
<b>Input Parameters</b>						
Data Input Voltage	mV	$V_{data\ in}$			900	Peak-to-Peak
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on Data Input Ports	V	$V_{DCin}$	-3		+3	AC coupled input
External DC Voltage on Clock Input Port	V	$V_{DCin}$	-6		+6	AC coupled input
External DC Voltage on RF Output Ports	V	$V_{DCout}$	-6		+6	AC coupled output
DC Supply Voltage	V	$V_{cc}$	0		+6.0	



## Specifications

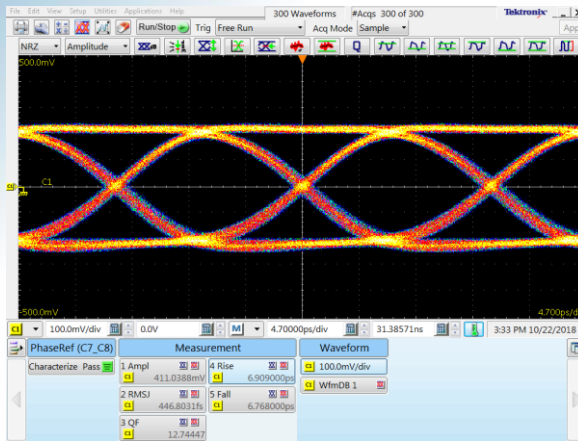
Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
<b>Input Parameters</b>						
Minimum Input Data Rate	Gbps	$R_{in,min}$			10	
Maximum Input Data Rate	Gbps	$R_{in,max}$	120			
Data Input Voltage	mV	$V_{data\ in}$		400	800	Eye Amplitude; Single-ended
Data Input Sensitivity	mV	$V_{data\ in}$	100 50			> 80 Gbps $\leq$ 80 Gbps Eye height; Single-ended; On scope display
Min. Clock Input Frequency	GHz	$f_{in,min}$			5	
Max. Clock Input Frequency	GHz	$f_{in,max}$	60			
Clock Input Voltage	mV	$V_{clk\ in}$	550 400		800 800	> 100 Gbps $\leq$ 100 Gbps Peak-to-Peak
<b>Output Parameters</b>						
Output Amplitude	mV	$V_{out}$	350	400		Eye Amplitude; Single-ended
Rise / Fall time	ps	$t_r/t_f$		7	9	20 % / 80 %; On scope display
Output Jitter, RMS value <sup>1</sup>	fs	$J_{rms}$		400	650	
<b>Power Requirements</b>						
Supply Voltage	V	$V_{cc}$	+5	5.2	+5.5	2.5 x 0.7 mm DC Power Jack
Supply Current	mA	$I_{ee}$		830	950	
Power Dissipation	mW	$P_d$		4150		@ $V_{cc} = +5V$
<b>Conditions</b>						
Operating Temperature	°C	$T_{ambient}$	15		35	

<sup>1</sup> Test condition: Input Signal Jitter<sub>RMS</sub> = 230 fs

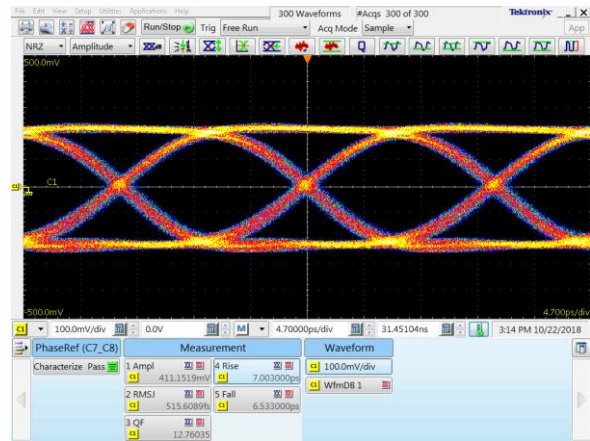


## Typical Output Eye Diagrams

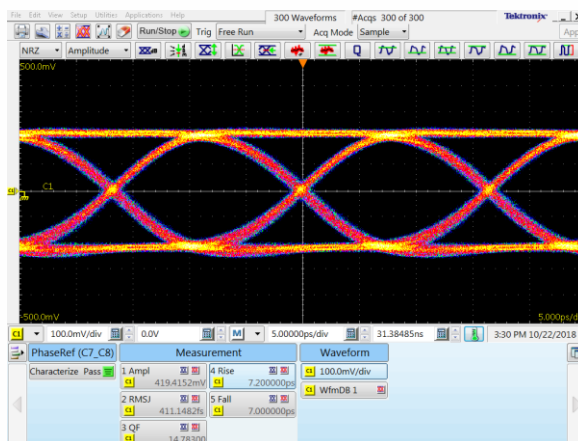
The measurements below had been performed using a SHF 603 A MUX (PRBS  $2^{31}-1$ ) and a Tektronix DSA8300 with Phase Reference Module (82A04B) and 70 GHz Sampling Head (80N01). The outputs of the demultiplexer module had been connected by 10 dB attenuators to the DSA input.



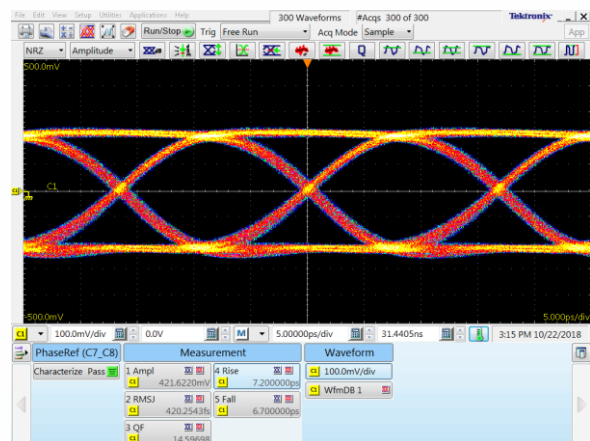
Out A @ 64 Gbps Output Bitrate



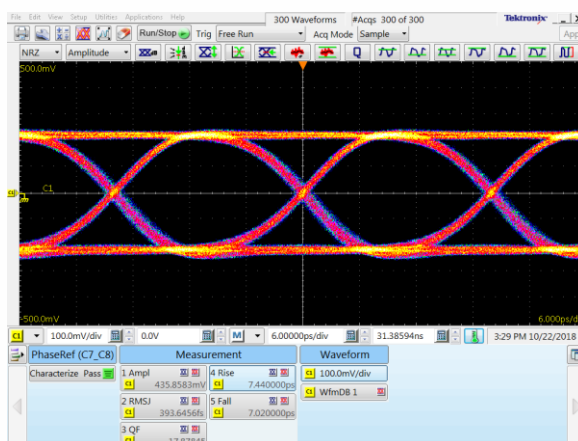
Out B @ 64 Gbps Output Bitrate



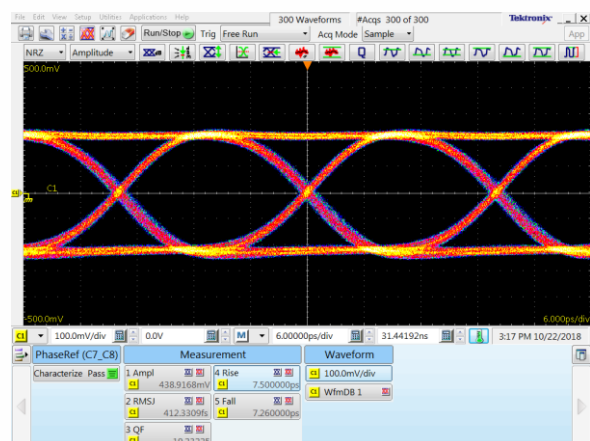
Out A @ 60 Gbps Output Bitrate



Out B @ 60 Gbps Output Bitrate



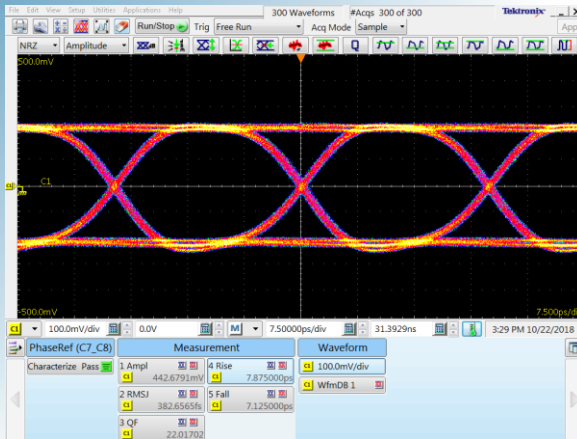
Out A @ 50 Gbps Output Bitrate



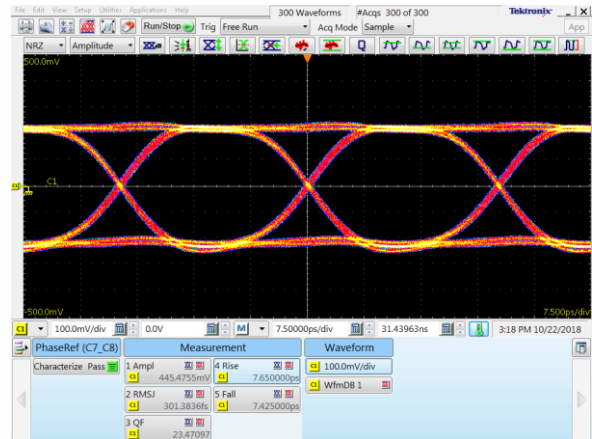
Out B @ 50 Gbps Output Bitrate

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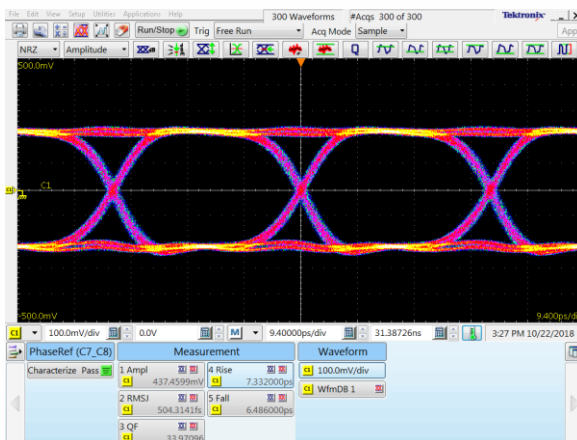




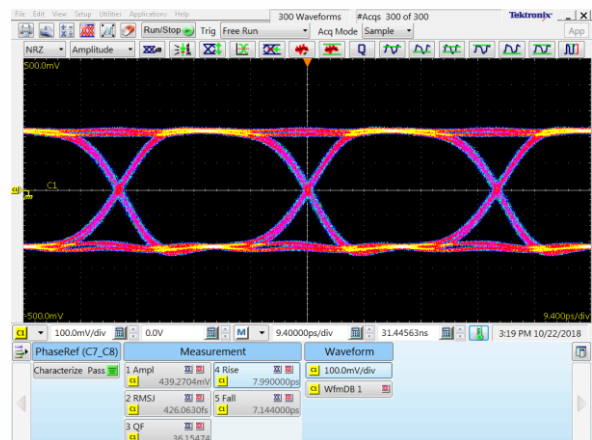
**Out A @ 40 Gbps Output Bitrate**



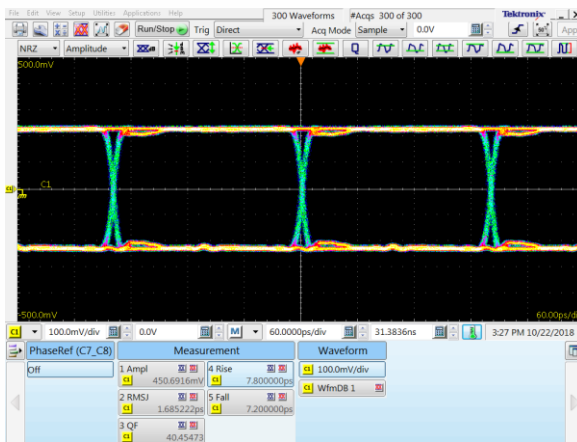
**Out B @ 40 Gbps Output Bitrate**



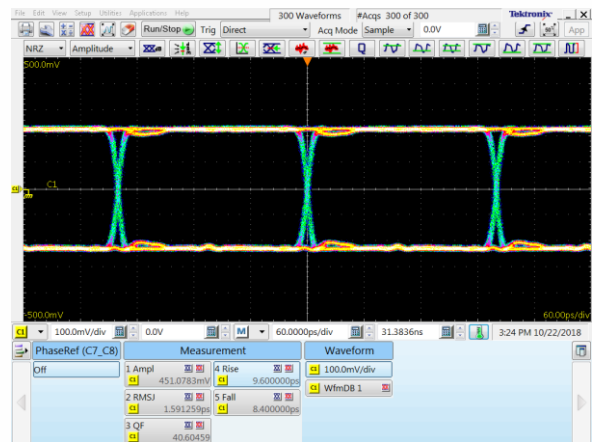
**Out A @ 32 Gbps Output Bitrate**



**Out B @ 32 Gbps Output Bitrate**



**Out A @ 5 Gbps Output Bitrate**



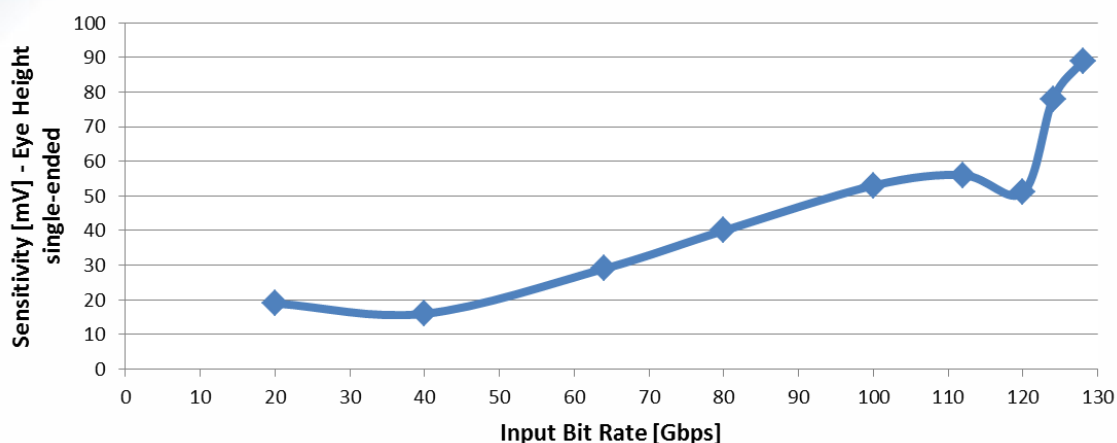
**Out B @ 5 Gbps Output Bitrate**



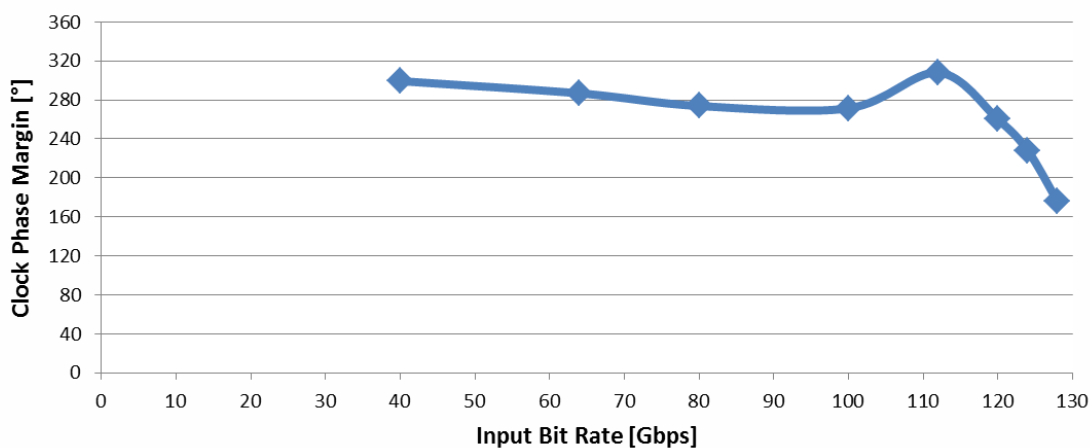
## Typical Performance

The measurements shown below had been performed using a SHF 603 A MUX (PRBS  $2^{31}-1$ ), a SHF 11104 A Error Analyzer, a Tektronix DSA8300 with Phase Reference Module (82A04B) and 70 GHz Sampling Head (80N01) to determine the eye height and jitter contribution of the input signal. In case of the sensitivity measurement the input signal had been reduced until a BER limit of  $<10^{-9}$  was achieved. For the clock phase margin measurement, an input signal with an eye height of 100 mV has been applied and the phase of the clock signal was varied until the BER reached the  $10^{-9}$  limit.

### Data Input Sensitivity

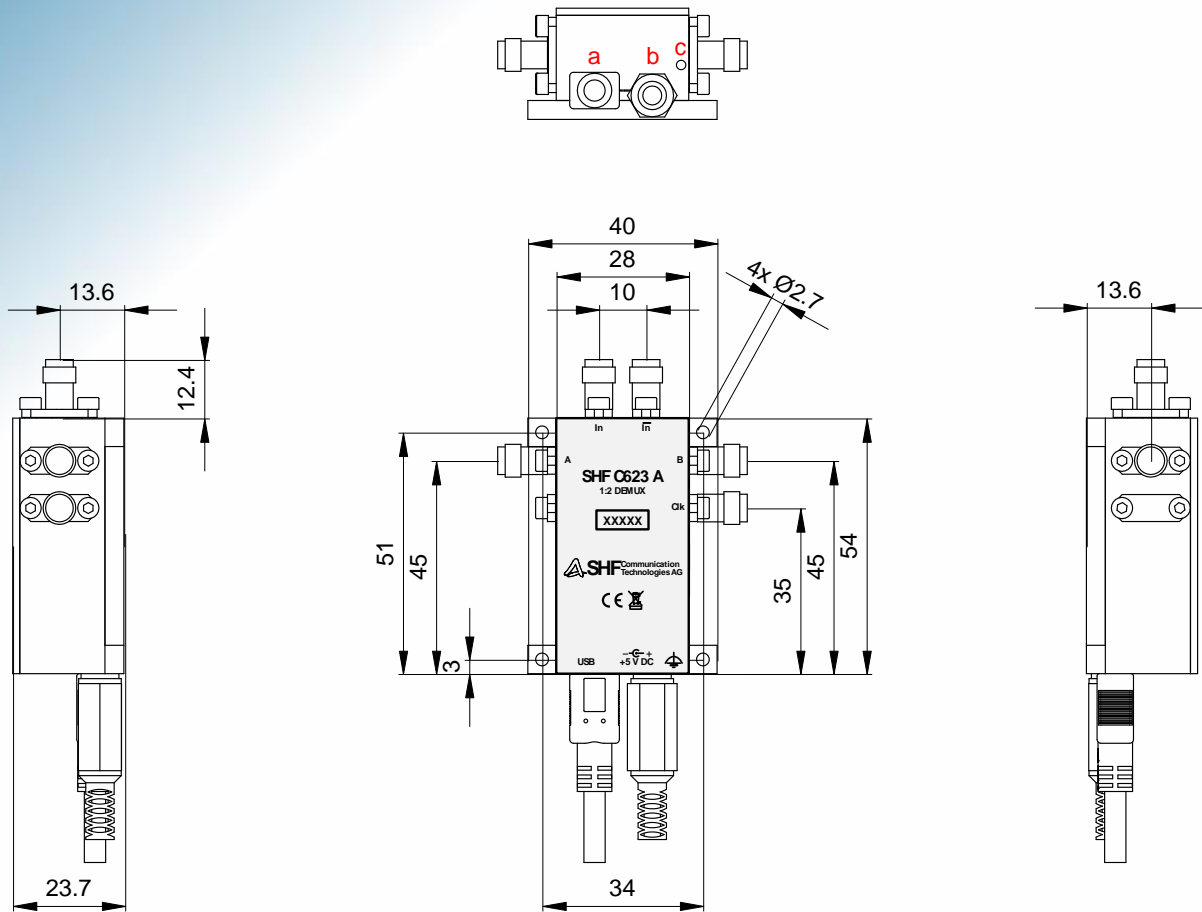


### Clock Phase Margin

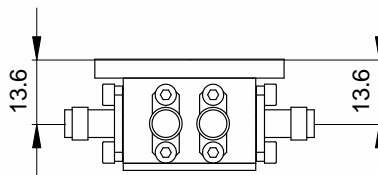




## Outline Drawing – Module



Port	Connector
In	1.85mm (V) female
In-	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female



Port	Connector
a	Mini-USB
b	Power
c	Functional earth (FE)





## Outline Drawing – Module with Heat Sink

