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Datasheet SHF C603 A 120 Gbps 2:1 Multiplexer







Description

The SHF C603 A is a 2:1 Multiplexer operating at data rates up to 120 Gbps for use in broadband test setups and telecom transmission systems. Two single ended serial data streams of up to 60 Gbps are accepted by the multiplexer and converted into one differential data signal of up to 120 Gbps. A single ended clock signal with a frequency half of the output data rate drives the SHF C603 A. All RF in- and output ports are AC-coupled and internally terminated with 50 Ohm to GND. Unused in- or output ports should be terminated with 50 Ohm.

Features

- Broadband operation up to 120 Gbps
- Differential data output, 400mV single ended output swing
- Single ended clock and data inputs
- Output Level Control
- USB interface

Applications

- 100G, 200G and 400G system evaluation & development
- Telecom transmission
- Broadband test and measurement equipment

Block Diagram







Remote Interface & Software

The MUX is controlled by the easy to use software package SHF Control Center (SCC). The amplitude, the duty cycle and the RF output state (on/off) can be set and is displayed in the graphical user interface (GUI).



SHF Control Center (SCC)

Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	V _{data in}			900	Peak-to-Peak
Clock Input Voltage	mV	$V_{\text{clk in}}$			900	Peak-to-Peak
External DC Voltage on RF Input Ports	V	V _{DCin}	-6		+6	AC coupled input
External DC Voltage on RF Output Ports	V	V _{DCout}	-6		+6	AC coupled output
DC Supply Voltage	V	V _{cc}	0		+6	

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Specifications

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	V _{data in}	300		800	
Minimum Clock Input Frequency	GHz	f _{in, min}		1	2	
Maximum Clock Input Frequency	GHz	f _{in, max}	60			
Clock Input Voltage	${\sf mV}_{\sf pp}$	$V_{\text{clk in}}$	400		800	
Output Parameters						
Minimum Output Data Rate	Gbps	R _{out,min}		2	4	@ 500mV _{pp} clock input
Maximum Output Data Rate	Gbps	R _{out,max}	120			@ 500mV _{pp} clock input
Maximum Output Amplitude	mV	V _{out}	350	400	550	single ended, adjustable up to -3dB
Rise / Fall time	ps	t _r /t _f		5	6	20% / 80%
Output Jitter, RMS value ¹	fs	J _{rms}		350 550	550 650	≤ 100Gbps > 100Gbps
Power Requirement						
Supply Voltage	V	V _{cc}	+5	5.2	+5.5	2.5 x 0.7 mm DC Power Jack
Supply Current	mA	Icc		960		
Power Dissipation	W	Pd		4.8		@ V _{CC} = +5V
Conditions						
Case Temperature ²	°C	T _{case}	10		45	

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¹ Test condition: Clock Input Signal Jitter_{RMS} <150 fs

 $^{^2}$ Tr / Tf of the output data signal can be slightly decreased by applying additional cooling measures like heat sinks or cooling fans.



Typical Output Eye Diagrams

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2³¹-1) and an Agilent Digital Communication Analyzer (DCA) with a Precision Timebase Module (86107A) and a 70 GHz Sampling Module (86118A). The outputs of the MUX module had been connected directly to the DCA input.



Out @ 120 Gbps

Out inv. @ 120 Gbps



Out @ 112 Gbps





Out @ 100 Gbps

Out inv. @ 100 Gbps

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Out @ 60 Gbps

Out inv. @ 60 Gbps



Out @ 100 Gbps, Level = -3dB

Out! @ 100 Gbps, Level = -3dB

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Port	Connector		
Out	1.85mm (V) female		
Out	1.85mm (V) female		
А	1.85mm (V) female		
В	1.85mm (V) female		
Clk	1.85mm (V) female		



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