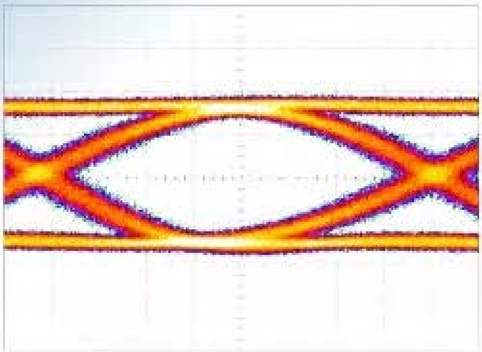
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23 • Aufgang D • 12277 Berlin – Marienfelde • Germany

Phone ++49 30 / 772 05 10 • Fax ++49 30 / 753 10 78

E-Mail: sales@shf.biz • Web: http://www.shf.biz



Datasheet

SHF 804 EA

Broadband Amplifier

SHF Communication Technologies AG

the bandwidth company

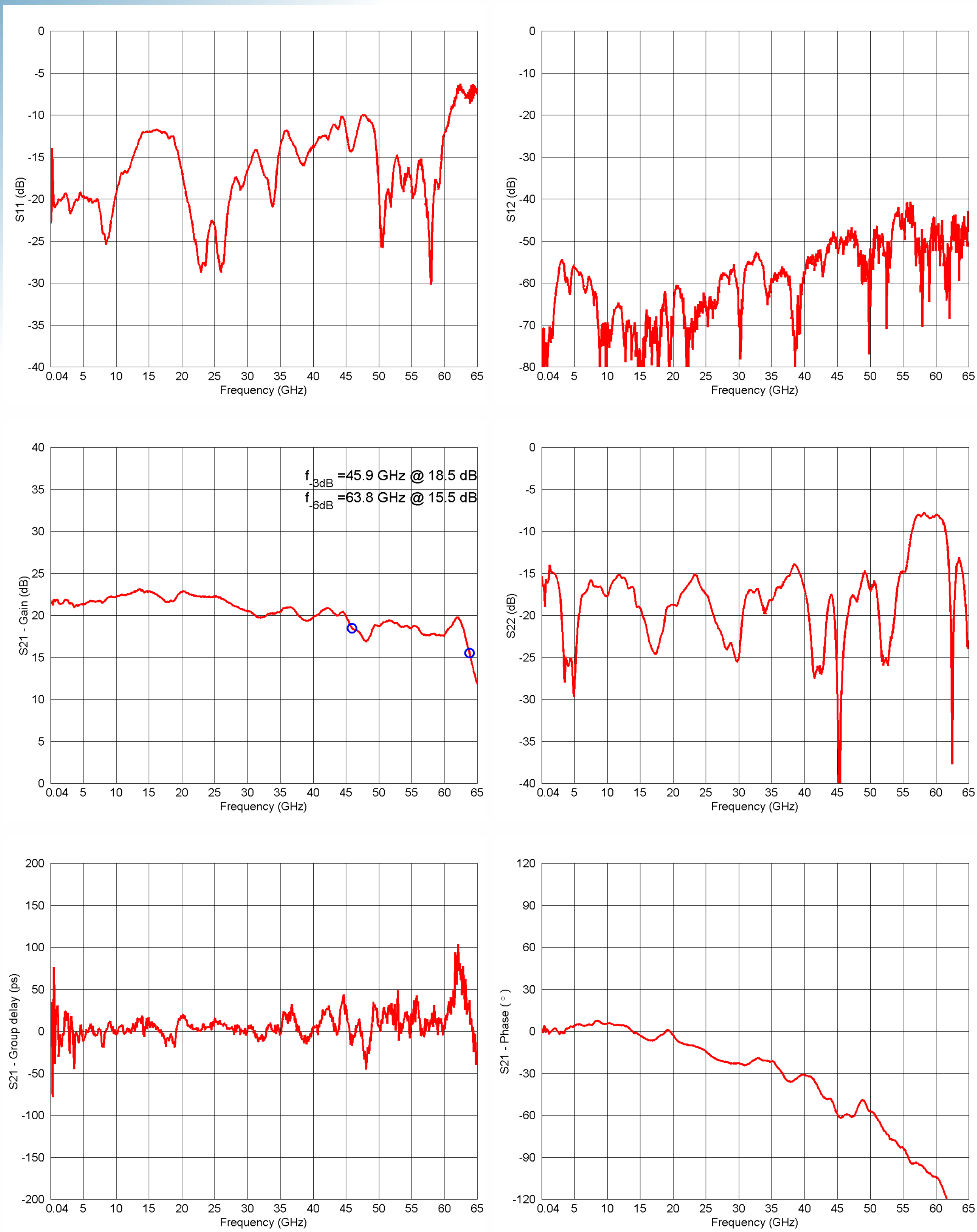
Specifications – SHF 804 EA

Parameter	Symbol	Unit	Min	Typ	Max	Conditions
High frequency 3 dB point	f_{HIGH}	GHz	45			
Low frequency 3 dB point	f_{LOW}	kHz			30	
Gain	G_p	dB	19	20	21	non-inverting
Gain control voltage current	U_{gc} I_{gc}	V mA	0 0		-5 -10	reduces gain by up to 3 dB
Gain ripple	ΔG_p	dB		±1	±1.5	
Temperature coefficient	T_c	dB/°C		-0.05		
Noise figure	N_F	dB		6		at 5 GHz
Group delay		ps		±50		>5GHz, <45GHz with 100 MHz aperture
Output power at 1 dB compression	P_{01dB}	dBm V	12.5 2.5			<35 GHz
Output power at 2 dB compression	P_{02dB}	dBm V	14.5 3.3			<35 GHz
Output power at 3 dB compression	P_{03dB}	dBm V	15.5 3.7			<35 GHz
Jitter		fs		 650	800 700	see page 6 deconvoluted in the output range between 2 and 3 V
Input return loss	S_{11}	dB		-15	-12 -10	<10 GHz <35 GHz
Output return loss	S_{22}	dB			-10	<45 GHz
Maximum input power		dBm			4 10	in operation without power supply
Rise time/fall time	t_r/t_f	ps		6	8	20%...80%
Supply voltage		V	6		15	0.25 A, reverse voltage protected
Power consumption		W	1.5			using 6 V supply voltage
Input connector						1.85mm V female
Output connector						1.85mm V female
Dimensions		mm				51x35x13.5 excluding connectors

The SHF 804 EA is a modulator driver suitable for driving electro-absorption modulators. In addition to high performance, the amplifier is extremely easy to use: a single power supply is all that is needed for operation.

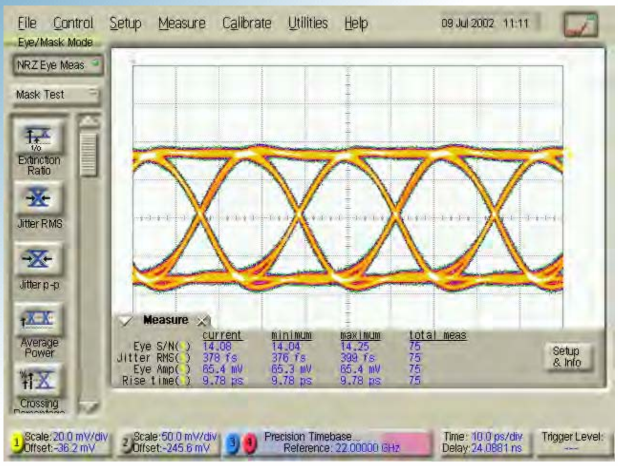
A two stage amplifier design is employed using special monolithic microwave integrated circuits (MMICs) inside special carriers to achieve ultra wide bandwidth and low noise performance. The custom made MMIC carrier is optimized for good input return loss between its interior and the 50 Ohm outside hybrid technology. The computer optimized broadband circuit is specially tuned for minimum passband ripple. A voltage regulator IC makes the amplifier insensitive to reverse voltage and line ripple.

S-Parameters, group delay and phase response at maximum gain

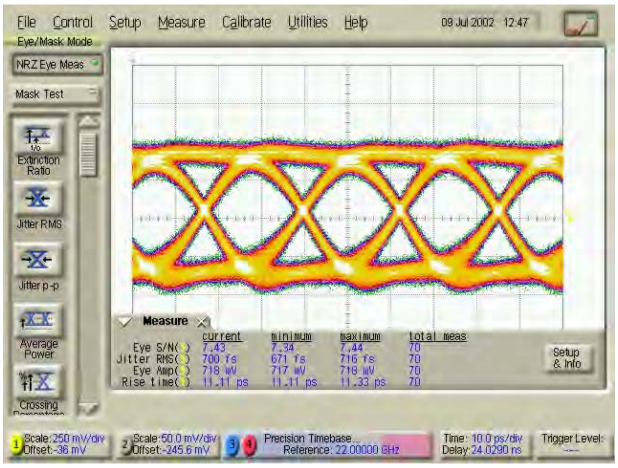


Aperture of group delay measurement: 100 MHz

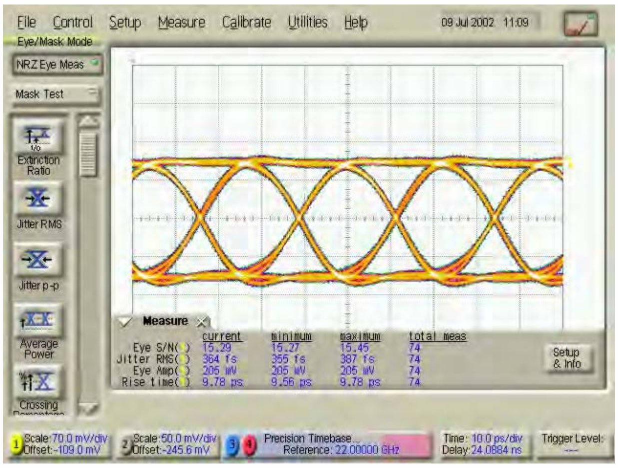
Eye diagrams at 44 Gbps



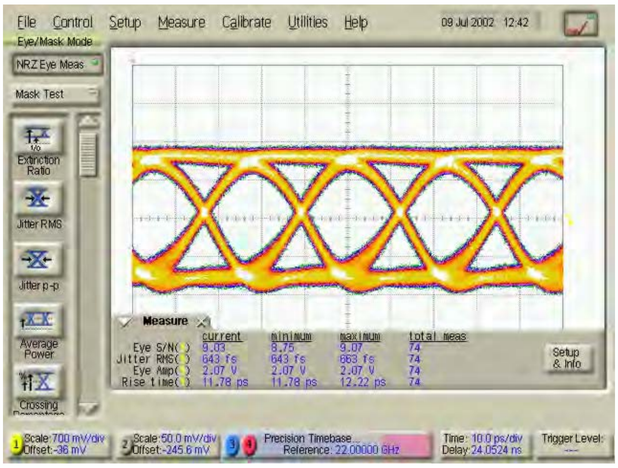
Input signal amplitude: 65 mV



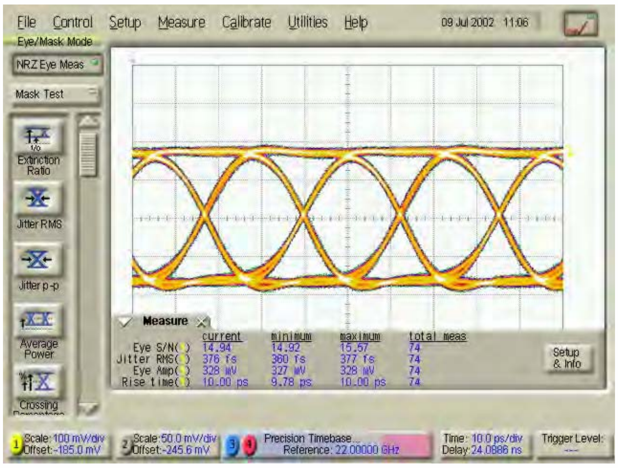
Output signal amplitude: 720 mV



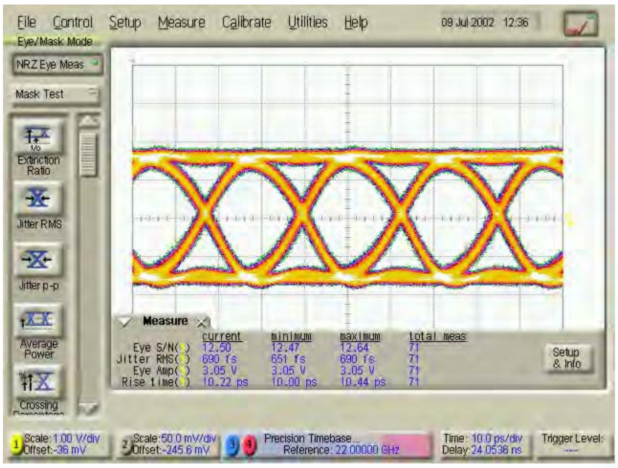
Input signal amplitude: 200 mV



Output signal amplitude: 2.0 V

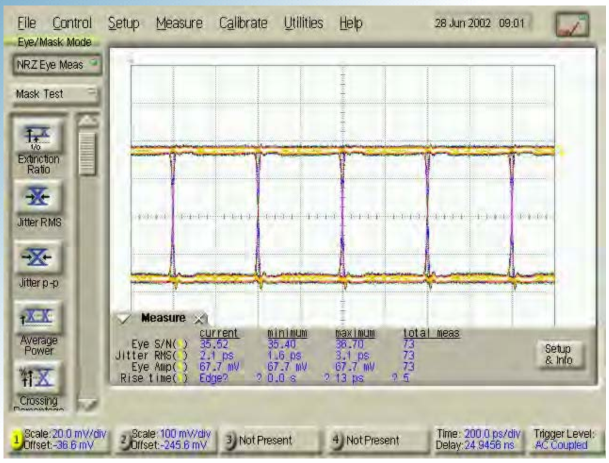


Input signal amplitude: 330 mV

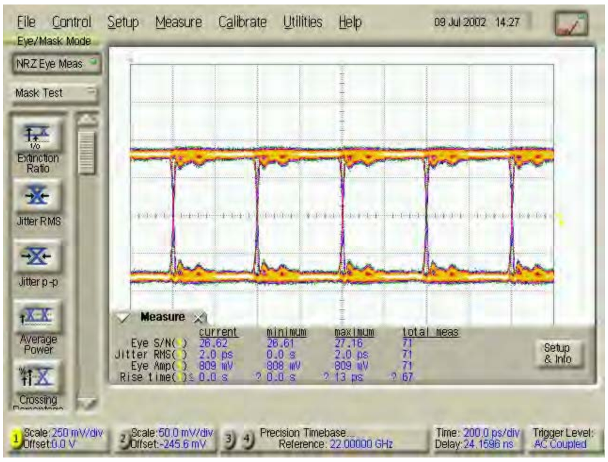


Output signal amplitude: 3.0 V

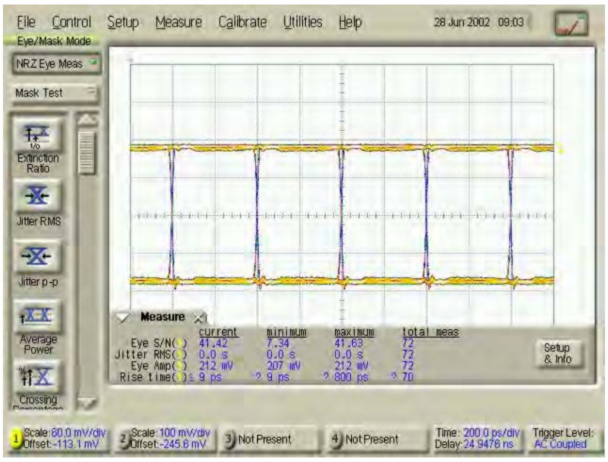
Eye diagrams at 2.5 Gbps



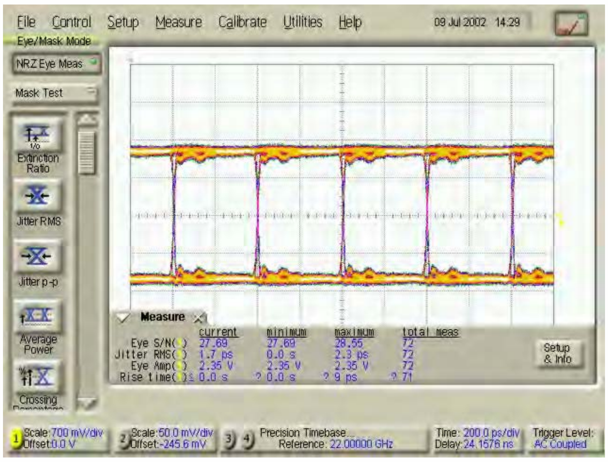
Input signal amplitude: 68 mV



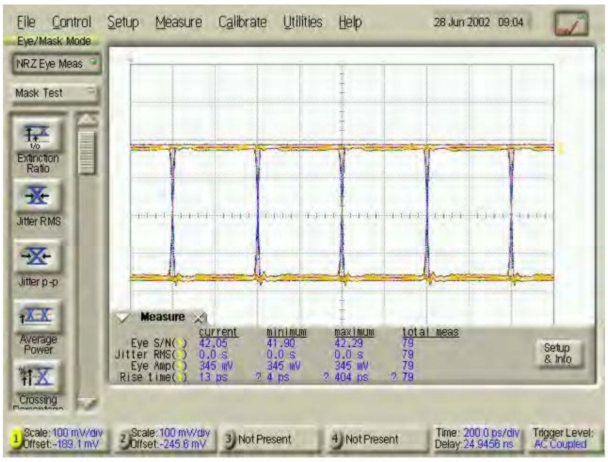
Output signal amplitude: 809 mV



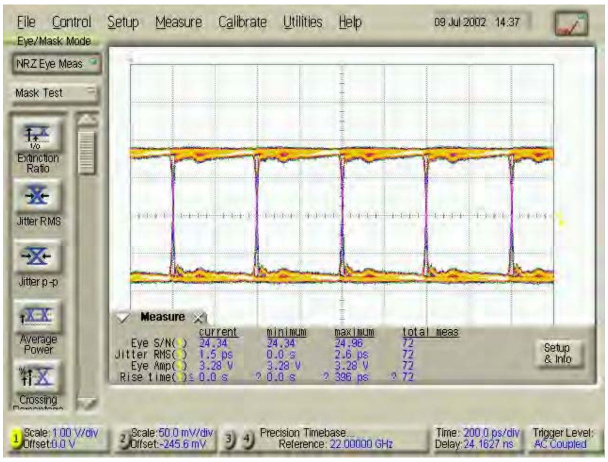
Input signal amplitude: 210 mV



Output signal amplitude: 2.35 V



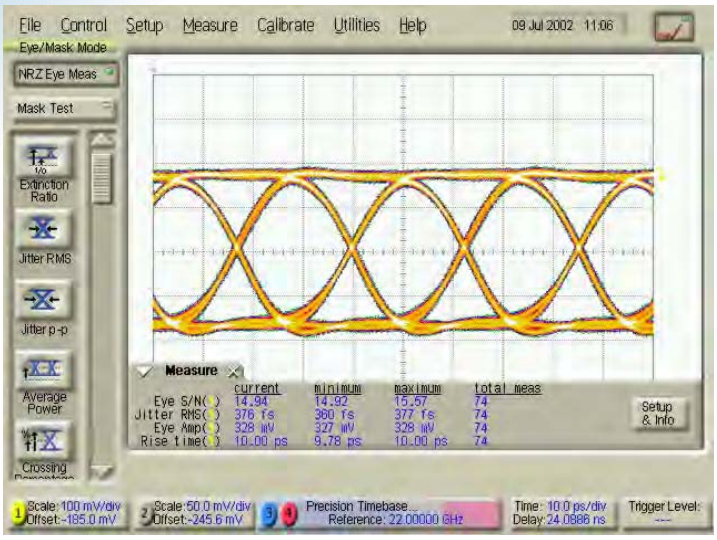
Input signal amplitude: 345 mV



Output signal amplitude: 3.3 V

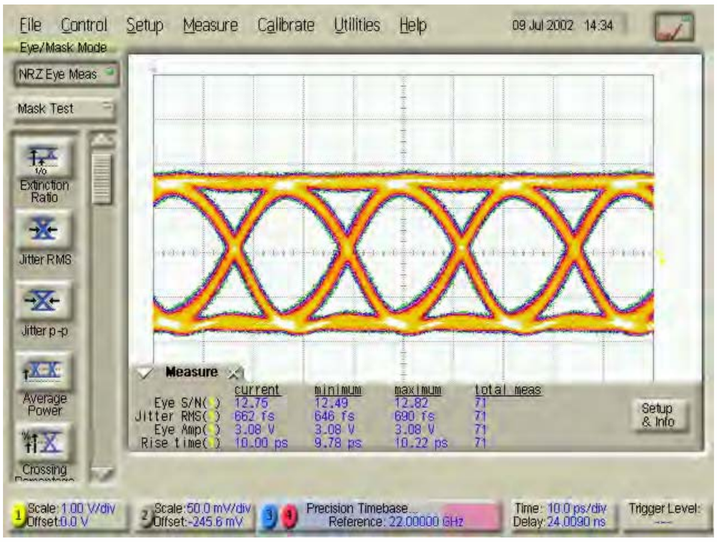
Jitter and rise time measurements at 44 Gbps

Input signal



Input jitter: 376 fs
Input rise time: 10.0 ps

Output signal



Output jitter: 660 fs
Output rise time: 10.0 ps

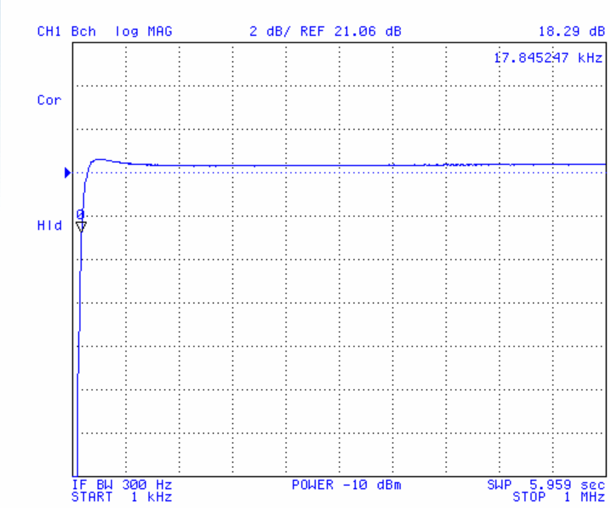
The specification for jitter is based on the measurement using a 63 GHz sampling module and precision time base. The figure of <800 fs specified on page 2 is **not** deconvoluted from the total system jitter; it is the figure displayed on the oscilloscope for the whole system (multiplexer, amplifier, sampling head and oscilloscope).

To deconvolute the jitter, we use the following formula:

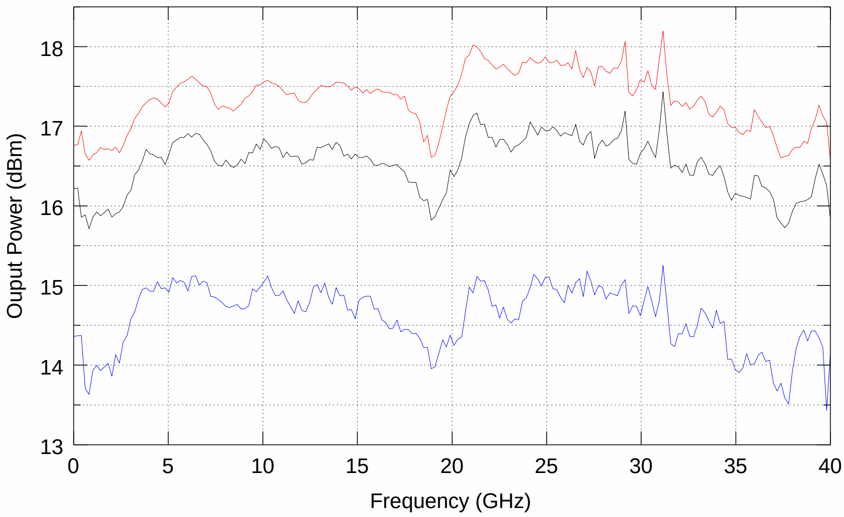
amplifier jitter = $[(\text{total jitter})^2 - (\text{input signal jitter})^2]^{½}$

This yields a jitter value of <700 fs.

Low frequency response (<1 MHz)

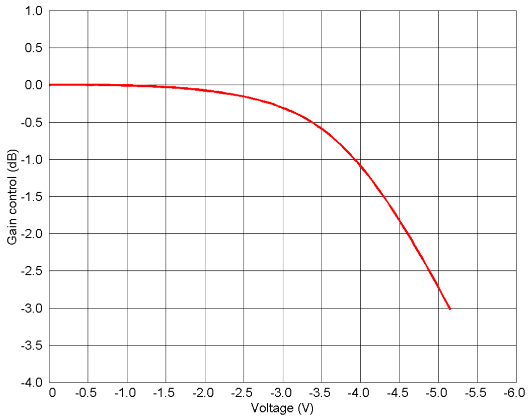


Saturation power



Top (red): 3 dB compression; Middle (black): 2 dB compression; Bottom (blue): 1 dB compression

Gain reduction function



All SHF amplifiers have a feature which allows the output gain to be reduced by up to approximately 3dB by applying a negative voltage to the gain reduction pin.

- **Available Options**

01: DC return on input (max. ±1.75 V, max. 35 mA)

02: Built-in bias tee on input (max. ±12 V, max. 220 mA)

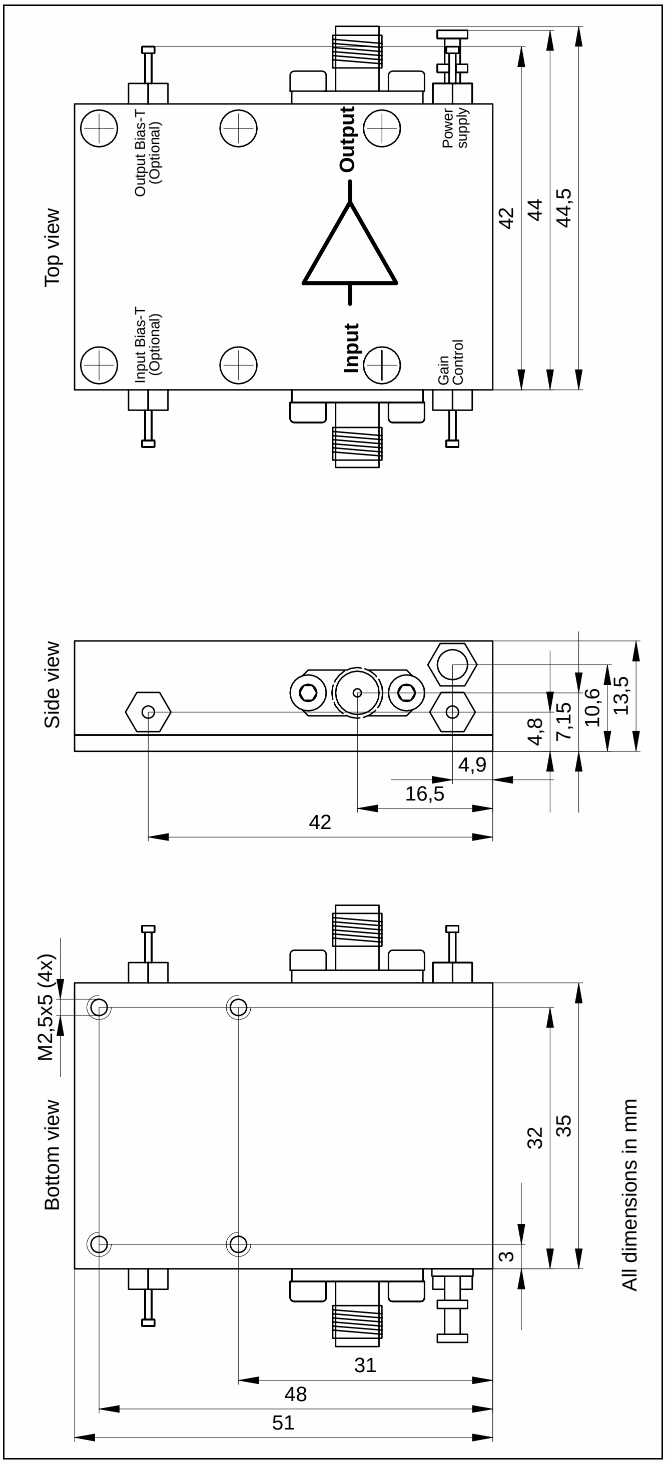
03: DC return on output (max. ±1.75 V, max. 35 mA)

04: Built-in bias tee on output (max. ±12 V, max. 220 mA)

MT: Special tuning available to optimize performance with E/O modulators
Positive gain slope of up to +3 dB possible

MP: Matches the phase of two amplifiers

The following options cannot be combined:
01 and 02
03 and 04
02 and 04



User Instructions

ATTENTION !

Electrostatic sensitive GaAs FET amplifier

1. To prevent damage through static charge build up, cables should be always discharged before connecting them to the amplifier!
2. Attach a 50 Ohm output load **before** supplying DC power to the amplifier!
3. The supply voltage can be taken from any regular 6…15 V, 0.5 A DC power supply and can be connected to the supply feed-through filter via an ON / OFF switch.
4. The minimum supply voltage is 6 V. A higher one increases the power dissipation of the internal voltage stabilizer.
5. Using a 3 dB or 6 dB input attenuator will result in a 6 dB or 12 dB increase of the input return loss. For minimal degradation of amplifier rise time, these attenuators should have a bandwidth specification of greater 50 GHz (V/ 1.85mm attenuators)!
6. An input signal of about 0.5 V_{pp} equivalent to -2 dBm will produce saturated output swing of 3.5V_{pp}.
7. Higher input voltages will drive the amplifier's output stage into saturation, leading to waveform peak clipping.
8. Saturated output voltages can only be used between 10 MHz and 40 GHz without damage while the amplifier is connected to a 50 Ohm precision load with a VSWR of less than 1.2 or better than 20 dB return loss up to 26 GHz.
9. While using a reflective load the output voltage has to be reduced to a safe operating level according to the magnitudes of the reflections.

   ATTENTION: At frequencies up to 20 GHz a capacitive load can be transformed to an inductive one through transmission lines! With an output stage driven into saturation this may lead to the immediate destruction of the amplifier (within a few ps)!
10. The input voltage should never be greater than 1 V_{pp} equivalent to 4 dBm input power.

    The input voltage without DC power supplied to the amplifier should never be greater than 2 V_{pp} equivalent to 10 dBm input power.
11. Hint: Pulse shape tuning of the amplifier has been performed after warm up at about 35°C case temperature. Slightly more over and undershoot will be present at low temperature!