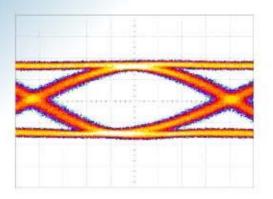


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Datasheet SHF 803 P

Broadband Amplifier









Specifications - SHF 803 P

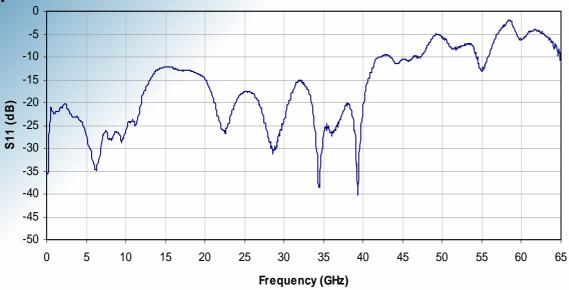
Parameter	Symbol	Unit	Min	Тур	Max	Conditions
High frequency 3 dB point High frequency 6 dB point	f _{HIGH}	GHz	40 50	45 53		
Low frequency 3 dB point	f _{LOW}	kHz			35	non-inverting
Gain		dB	16	17	18	
Output voltage adjust Voltage Current		V mA	0	10	-5	reduces gain by up to 3 dB
Gain ripple		dB		±1	±1.5	
Temperature coefficient	T _c	dB/°C		-0.05		
Noise figure	N _F	dB		6		at 5 GHz
Output power at 1 dB compression	P _{01dB}	dBm (V)	20 (6.3) 17 (4.5)			<10 GHz <40 GHz
Output power at 2 dB compression	P _{02dB}	dBm (V)	21 (7.0) 18 (5.1)			<10 GHz <40 GHz
Output power at 3 dB compression	P _{03dB}	dBm (V)	22 (7.8) 19 (5.6)			<10 GHz <40 GHz
Jitter		fs		550	700 600	on scope display deconvoluted output voltage ~4V
Input return loss	S ₁₁	dB		-20	-15 -10	>40 MHz <10 GHz >10 GHz <40 GHz
Output return loss	S ₂₂	dB			-10	>40 MHz <40 GHz
Maximum input power		dBm			9 10	in operation without power supply
Rise time/fall time	t _r /t _f	ps			9	20%80%
Supply voltage		V	9		12	0.55 A, reverse voltage protected
Power consumption		W	5			using 9 V supply voltage
Input connector						V (1.85 mm) female
Output connector						V (1.85mm) male
Dimensions		mm				51x35x13.5 excluding connectors

The SHF 803 P is a modulator driver suitable for OC-768 applications. Together with high performance, the amplifier is extremely easy to use: a single power supply is all that is needed for operation.

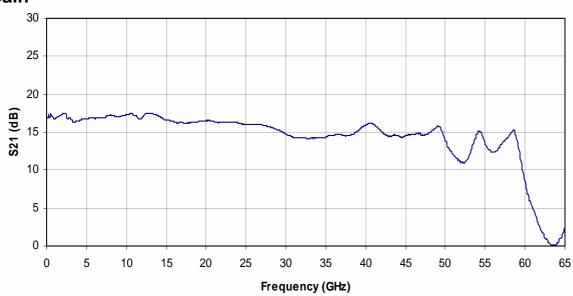
A two stage amplifier design is employed using special monolithic microwave integrated circuits (MMICs) inside special carriers to achieve ultra wide bandwidth and low noise performance. The custom made MMIC carrier is optimized for good input return loss between its interior and the 50 Ohm outside hybrid technology. The computer optimized broadband circuit is individually tuned for minimum pass band ripple. A voltage regulator IC makes the amplifier insensitive to reverse voltage and line ripple.

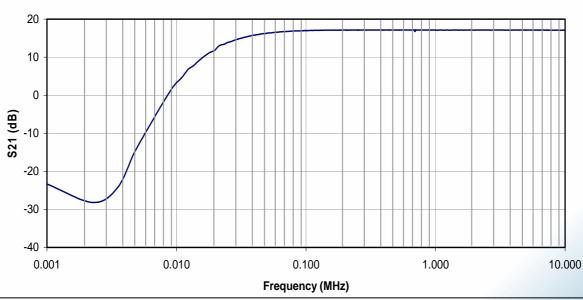






Gain



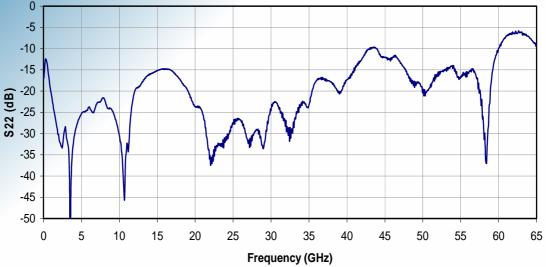


SHF reserves the right to change specifications and design without notice – SHF 803 P – Rev. 3.0 – 7/DEC/2004

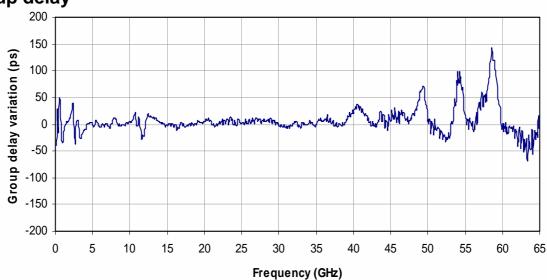




Output return loss

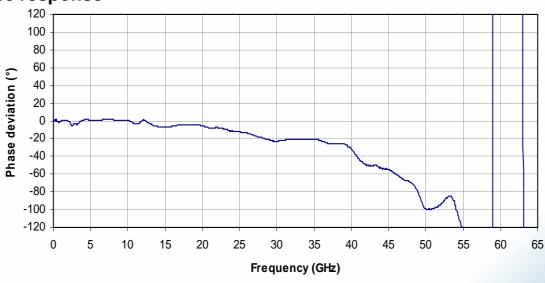


Group delay



Aperture of group delay measurement: 100MHz

Phase response

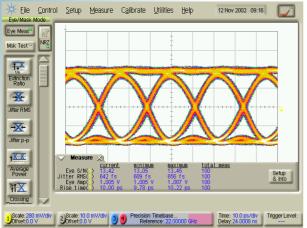






Eye diagrams at 44 Gbps

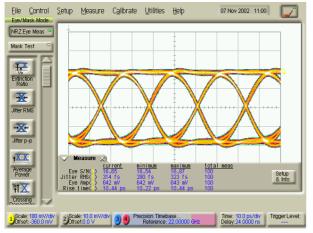
Measured with 50 GHz sampling module and precision timebase.

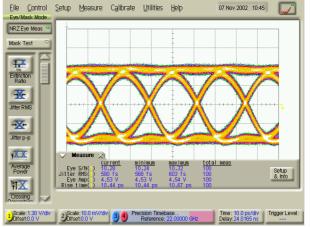


| Scale: 180 V/div | 2 | Scale: 100 m//div | 3 | Precision Timebase. | Time: 100 ps/div | Tingger Level: | Scale: 180 V/div | 2 | Scale: 100 m//div | 3 | Precision Timebase. | Time: 100 ps/div | Tingger Level: | Tingger Level:

Input signal amplitude: 1.005 V

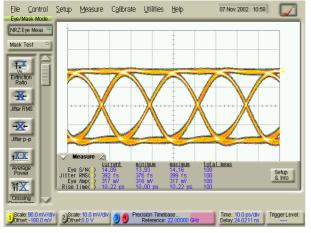
Output signal amplitude: 6.45 V

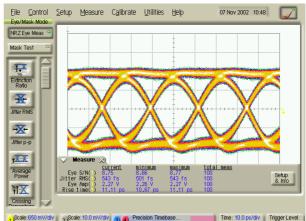




Input signal amplitude: 642 mV

Output signal amplitude: 4.53 V





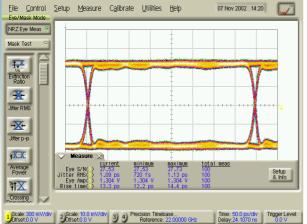
Input signal amplitude: 317 mV

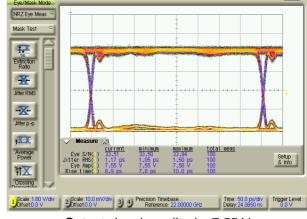
Output signal amplitude: 2.27V





Eye diagrams at 2.5 Gbps



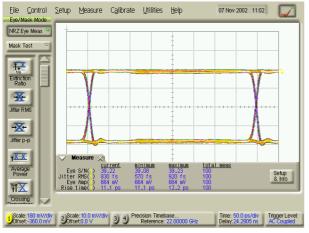


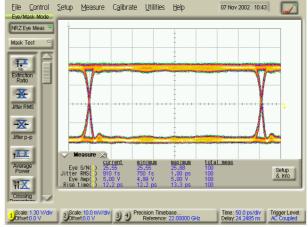
07 Nov 2002 14:08

Eile Control Setup Measure Calibrate Utilities Help

Input signal amplitude: 1.304 V

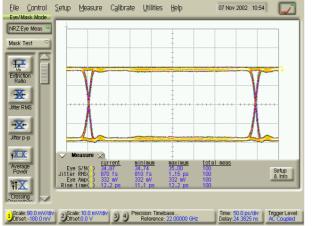
Output signal amplitude: 7.55 V

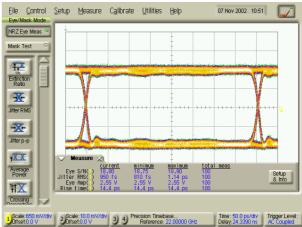




Input signal amplitude: 664 mV

Output signal amplitude: 5.00 V





Input signal amplitude: 332 mV

Output signal amplitude: 2.55 V



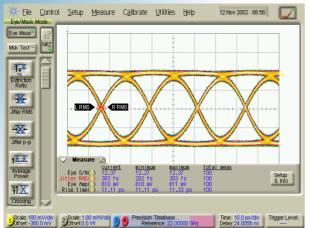


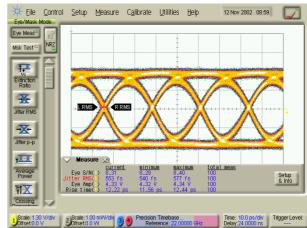
Jitter and rise time measurements at 44 Gbps

Measured with 63 GHz sampling module and precision timebase.

Input signal

4.3 V output from SHF 803 P



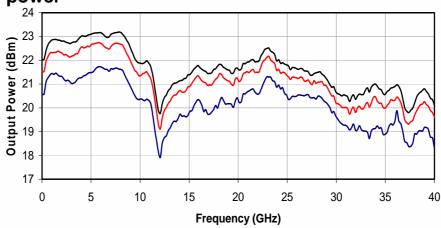


Jitter: 303 fs; Rise time: 11.11 ps

Jitter: 553 fs; Rise time: 12.22 ps

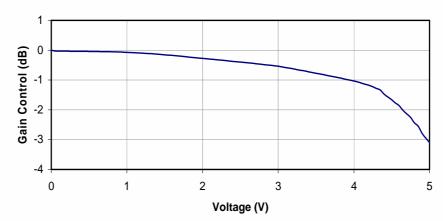
To deconvolute the jitter, we use the following fomula: **amplifier jitter = [(total jitter)**² - (input signal jitter)²]^{$\frac{1}{2}$} This yields a jitter value of <600 fs.

Saturation power



Top (blue): 3 dB compression; Middle (red): 2 dB compression; Bottom (black): 1 dB compression

Gain reduction function



All SHF amplifiers have a feature which allows the output gain to be reduced by up to approximately 3 dB by applying a negative voltage to the gain reduction pin.





Available Options

01: DC return on input (max. ±1.75 V, max. 35 mA)

02: Built-in bias tee on input (max. ± 12 V, max. 220 mA)

03: DC return on output (max. ± 1.75 V, max. 35 mA)

04: Built-in bias tee on output (max. ±12 V, max. 220 mA)

MT: Special tuning available to optimize performance with E/O modulators Positive gain slope of up to +3 dB possible

MP: Matches the phase of two amplifiers

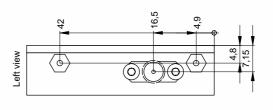
The following options cannot be combined:

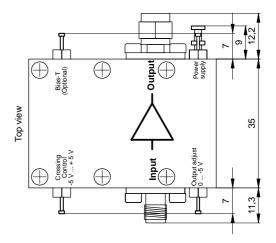
01 and 02

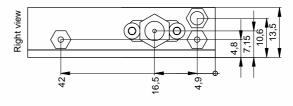
03 and 04

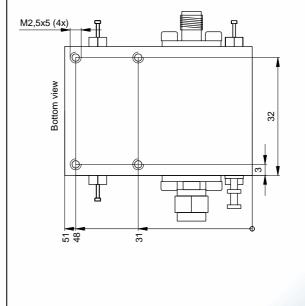
02 and 04

For other configurations please contact us.













User Instructions

ATTENTION!

Electrostatic sensitive GaAs FET amplifier

- 1. To prevent damage through static charge build up, cables should be always discharged before connecting them to the amplifier!
- 2. Attach a 50 Ohm output load **before** supplying DC power to the amplifier!
- 3. The supply voltage can be taken from any regular 9...12 V, 1 A DC power supply and can be connected to the supply feed-through filter via an ON / OFF switch.
- 4. The minimum supply voltage is 9 V. A higher one increases the power dissipation of the internal voltage stabilizer.
- 5. Using a 3 dB or 6 dB input attenuator will result in a 6 dB or 12 dB increase of the input return loss. For minimal degradation of amplifier rise time, these attenuators should have a bandwidth specification of greater than 50 GHz (V/ 1.85mm attenuators)!
- 6. An input signal of about 1.6 V_{pp} equivalent to 8 dBm will produce saturated output swing of 7.8 V_{pp} .
- 7. Higher input voltages will drive the amplifier's output stage into saturation, leading to waveform peak clipping.
- 8. Saturated output voltages can only be used between 10 MHz and 40 GHz without damage while the amplifier is connected to a 50 Ohm precision load with a VSWR of less than 1.2 or better than 20 dB return loss up to 26 GHz.
- 9. While using a reflective load the output voltage has to be reduced to a safe operating level below $8V_{pp}$ according to the magnitudes of the reflections.
 - **ATTENTION**: At frequencies up to 20 GHz a capacitive load can be trans-formed to an inductive one through transmission lines! With an output stage driven into saturation this may lead to the immediate destruction of the amplifier (within a few ps)!
- 10. The input voltage should never be greater than 1.8 V_{pp} equivalent to 9 dBm input power.
 - The input voltage without DC power supplied to the amplifier should never be greater than 2 V_{pp} equivalent to 10 dBm input power.
- 11. Hint: Pulse shape tuning of the amplifier has been performed after warm up at about 35°C case temperature. Slightly more over and undershoot will be present at low temperature!

