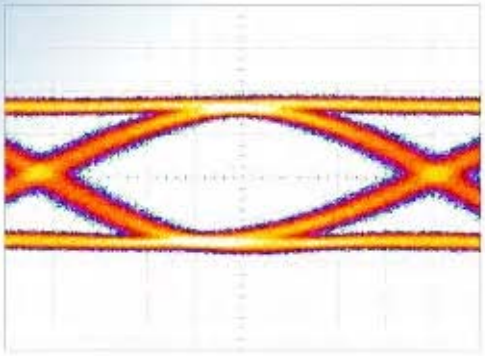
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23 • Aufgang D • 12277 Berlin – Marienfelde • Germany

Phone ++49 30 / 772 05 10 • Fax ++49 30 / 753 10 78

E-Mail: sales@shf.biz • Web: http://www.shf.biz



Datasheet

SHF 801 P

Broadband Amplifier

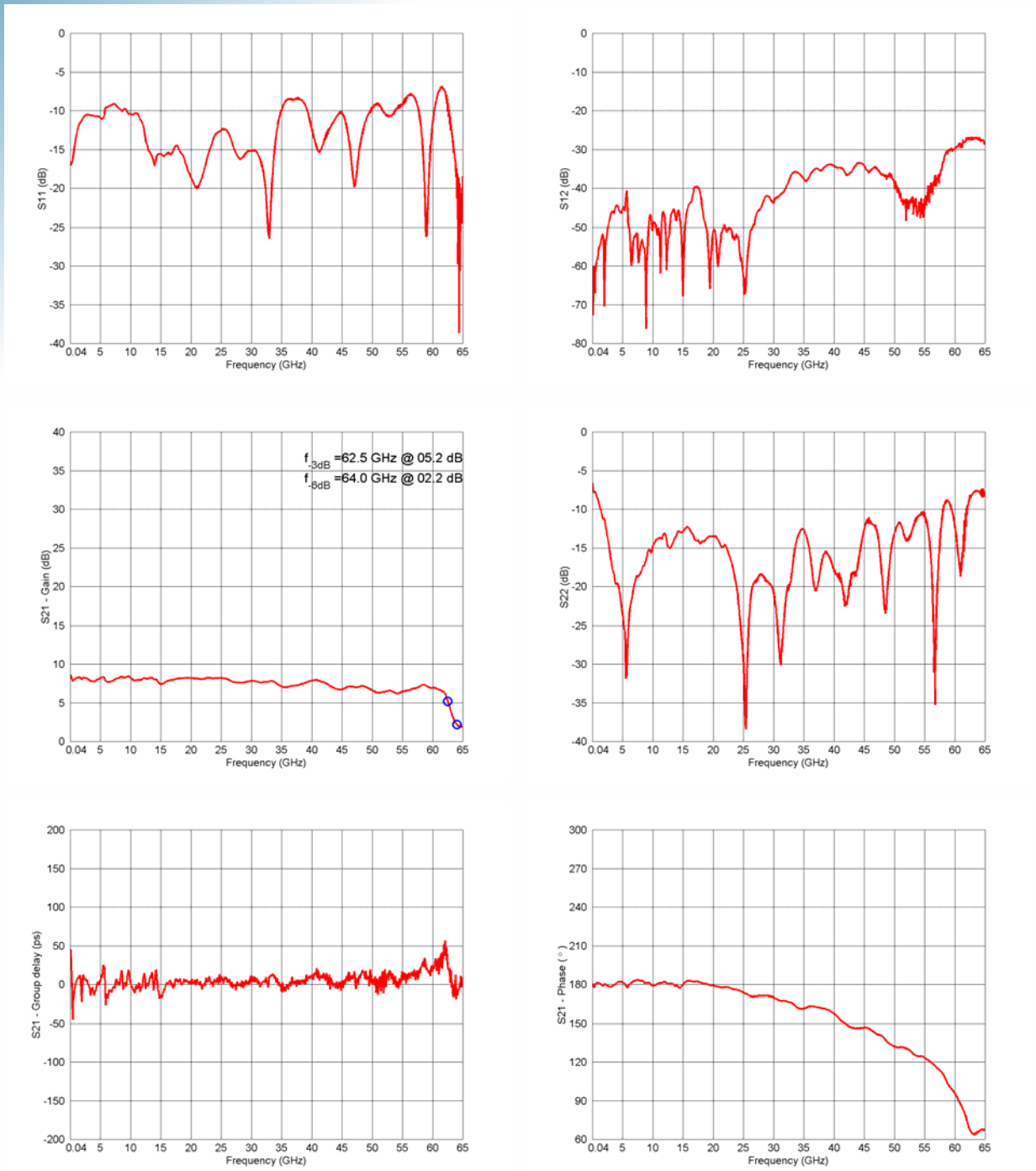
Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Conditions
High frequency 3 dB point High frequency 6 dB point	f_{HIGH}	GHz	58 62	62 64		
Low frequency 3 dB point	f_{LOW}	kHz			15	inverting
Gain		dB	7	8	9	
Gain control voltage		V	0		-5	reduces by up to 3 dB
Gain ripple		dB		±1	±1.5	
Output power at 1 dB compression	P_{01dB}	dBm (V)	9 (1.8) 11 (2.2)			<5 GHz <40 GHz
Output power at 2 dB compression	P_{02dB}	dBm (V)	10 (2) 12 (2.5)			<5 GHz <40 GHz
Output power at 3 dB compression	P_{03dB}	dBm (V)	11 (2.2) 13 (2.8)			<5 GHz <40 GHz
Jitter		fs		450	600 500	on scope display deconvoluted in the output range between 1…2 V
Input return loss	S_{11}	dB		8 7	7 6	<50 GHz <65 GHz
Output return loss	S_{22}	dB			5 10 6	<3 GHz <50 GHz <65 GHz
Maximum input power		dBm			8 13	in operation without power supply
Rise time/fall time	t_r/t_f	ps		6	8	20%...80%
Supply voltage		V	5.2		9	0.13 A, reverse voltage protected
Power consumption		W	0.68			using 5.2 V supply voltage
Input connector						V female
Output connector						V female
Dimensions		mm				51x35x13.5 excluding connectors

The SHF 801 P is ideal for use as a preamplifier for extremely high bandwidth devices, e.g. photodiodes, spectrum analyzers, network anlyzers, test equipment, etc.

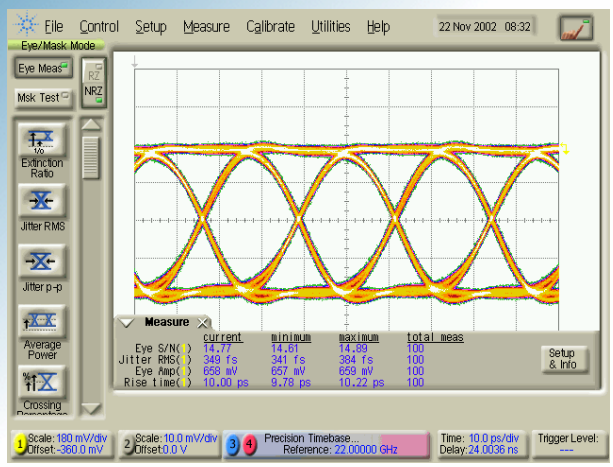
A single stage amplifier design is employed using special monolithic microwave integrated circuits (MMICs) inside special carriers to achieve ultra wide bandwidth and low noise performance. The custom made MMIC carrier is optimized for good input return loss between its interior and the 50Ω outside hybrid technology. The computer optimized broadband circuit is designed for minimum pass band ripple. A voltage regulator IC makes the amplifier insensitive to reverse voltage and line ripple.

S-Parameters, group delay and phase response at maximum gain

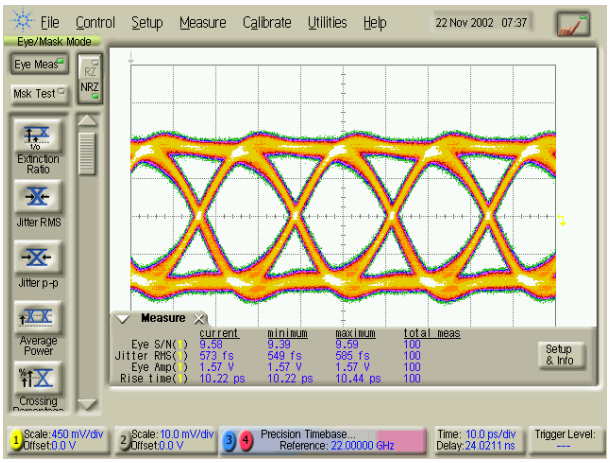


Aperture of Group Delay measurement: 100 MHz

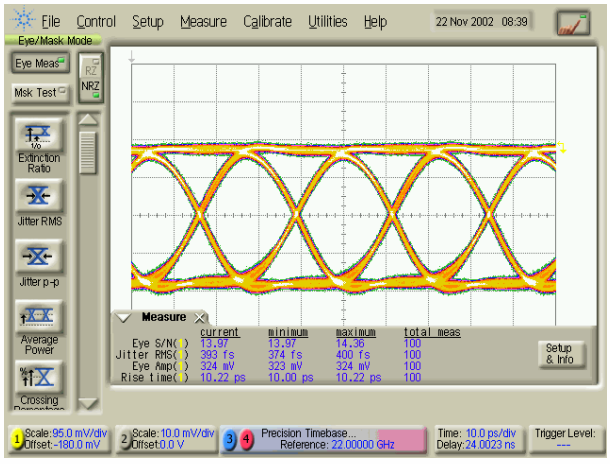
Eye diagrams at 44 GBit/s



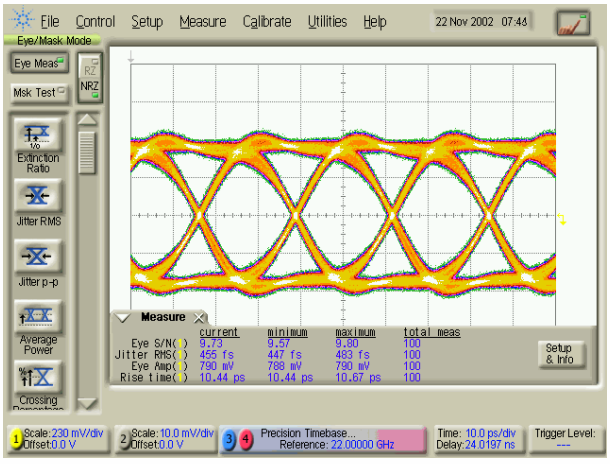
Input signal amplitude: 658 mV



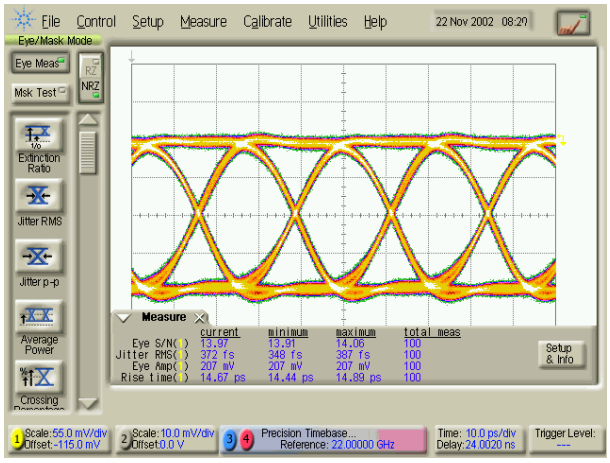
Output signal amplitude: 1.57 V



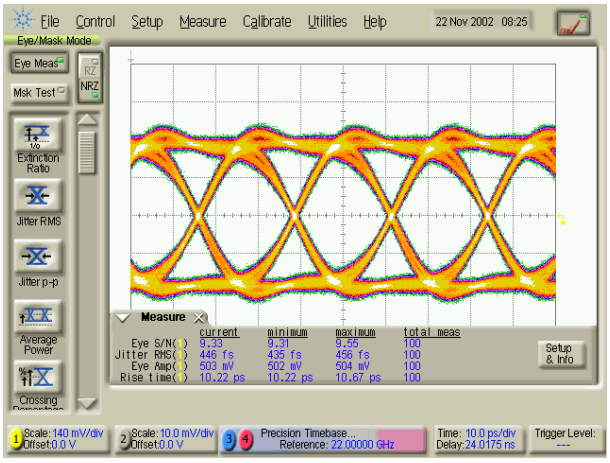
Input signal amplitude: 324 mV



Output signal amplitude: 790 mV

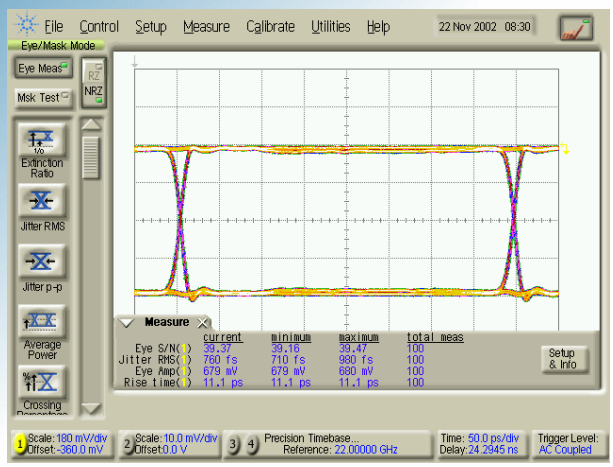


Input signal amplitude: 207 mV

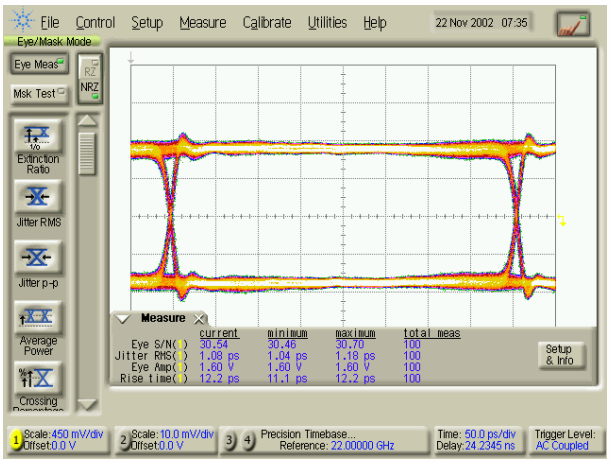


Output signal amplitude: 503 mV

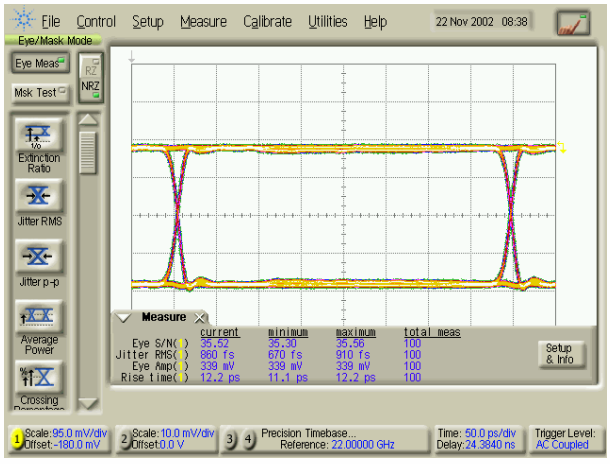
Eye diagrams at 2.5 GBit/s



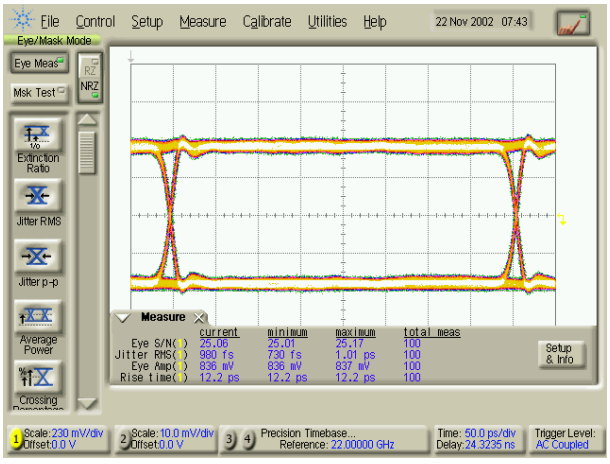
Input signal amplitude: 679 mV



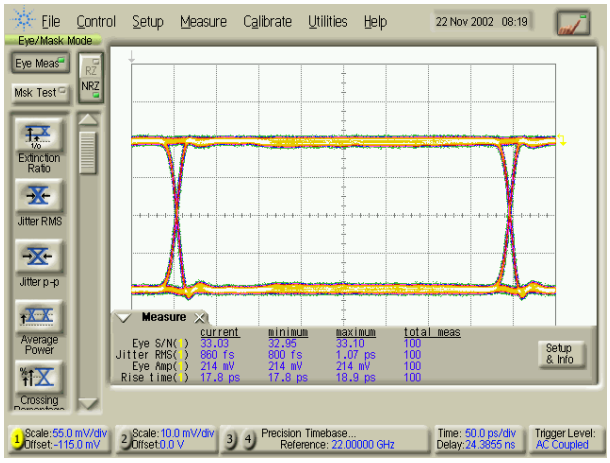
Output signal amplitude: 1.60 V



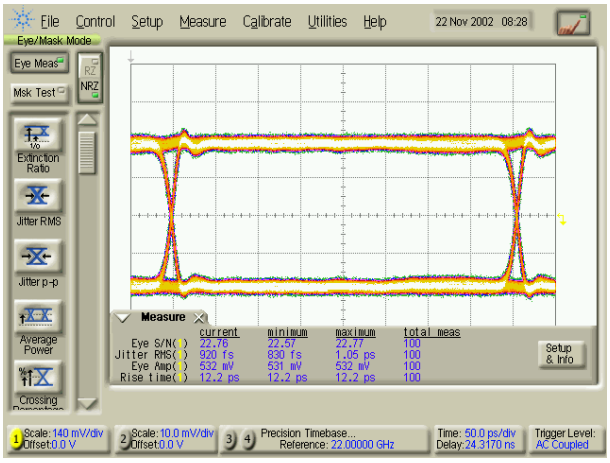
Input signal amplitude: 339 mV



Output signal amplitude: 836 mV



Input signal amplitude: 214 mV

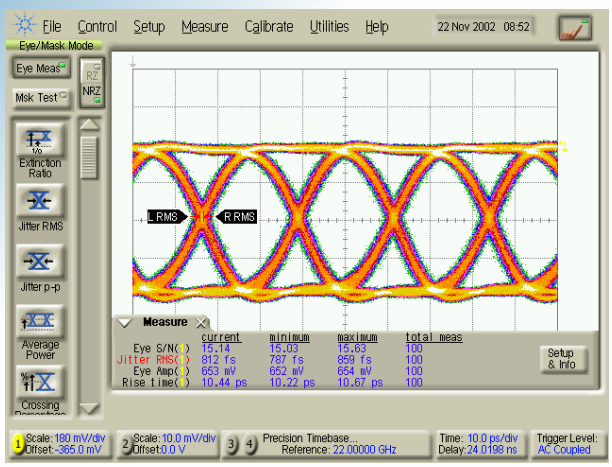


Output signal amplitude: 532 mV

Jitter measurements at 44 GBit/s

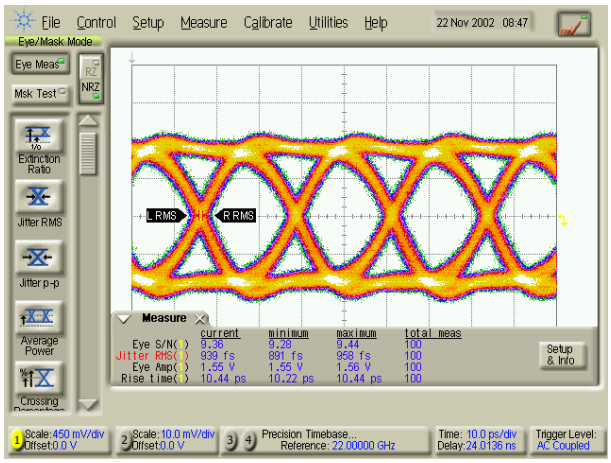
Measured with 50 GHz sampling module and standard timebase.

Input signal



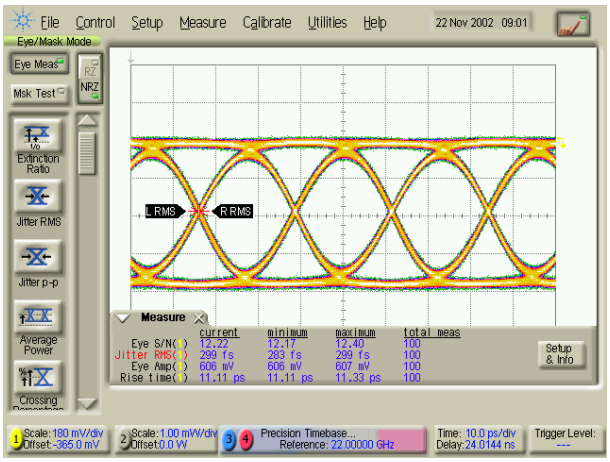
Jitter: 812 fs

1.5 V output from SHF 801 P

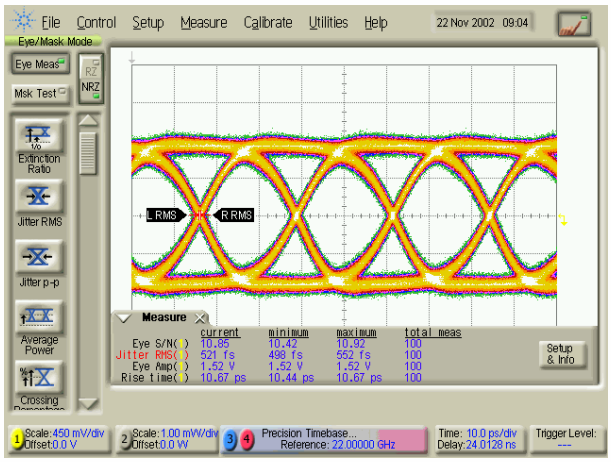


Jitter: 939 fs

Measured with 63 GHz sampling module and precision timebase.



Jitter: 299 fs



Jitter: 521 fs

The specification for jitter is based on the measurement using the 63 GHz sampling module and precision time base. The figure of <600 fs is **not** deconvoluted from the total system jitter; it is the figure displayed on the oscilloscope for the whole system (multiplexer, amplifier, sampling head and oscilloscope).

To deconvolute the jitter, we use the following formula:

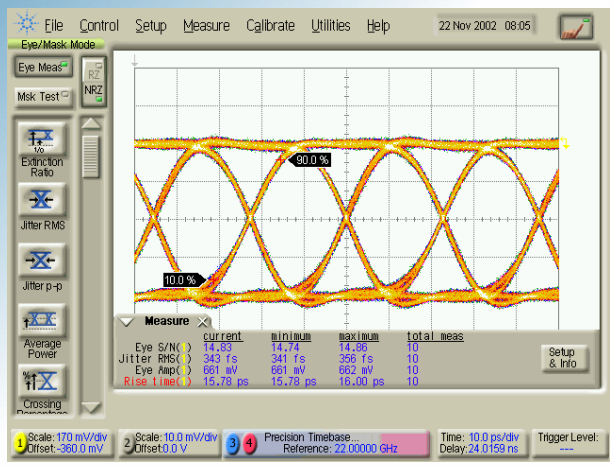
$$\text{amplifier jitter} = [(\text{total jitter})^2 - (\text{input signal jitter})^2]^{1/2}$$

This yields a jitter value of <500 fs.

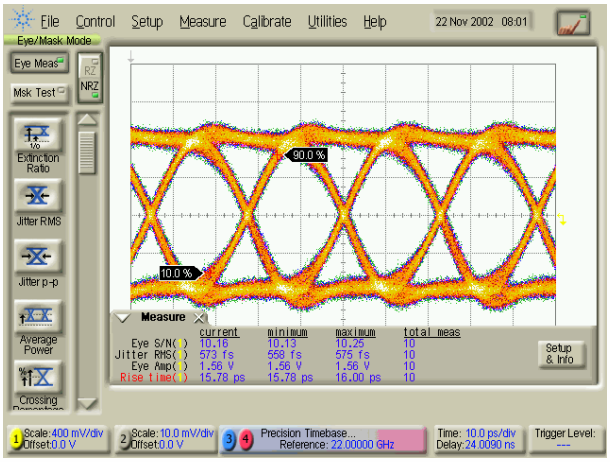
It is taken at an output level between 1 and 2 V. Using a standard time base and 50 GHz sampling module, we specify a maximum jitter figure of 1ps.

Rise/Fall times

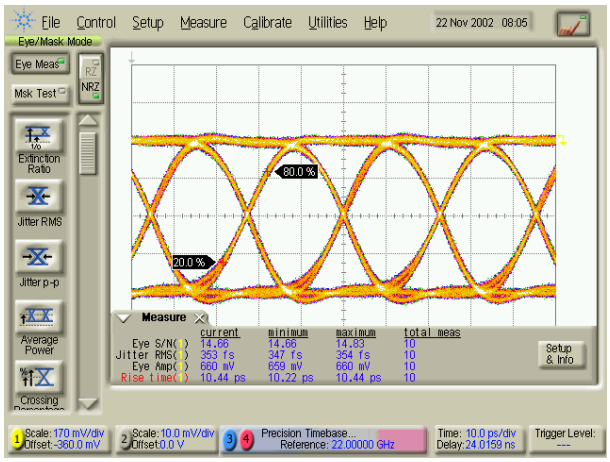
Input signal

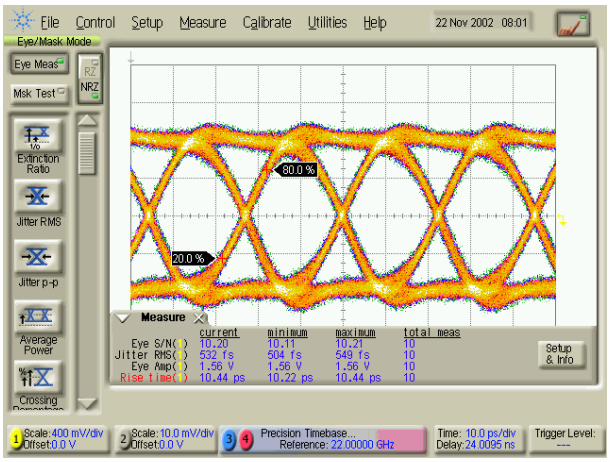


1.5 V output from SHF 801



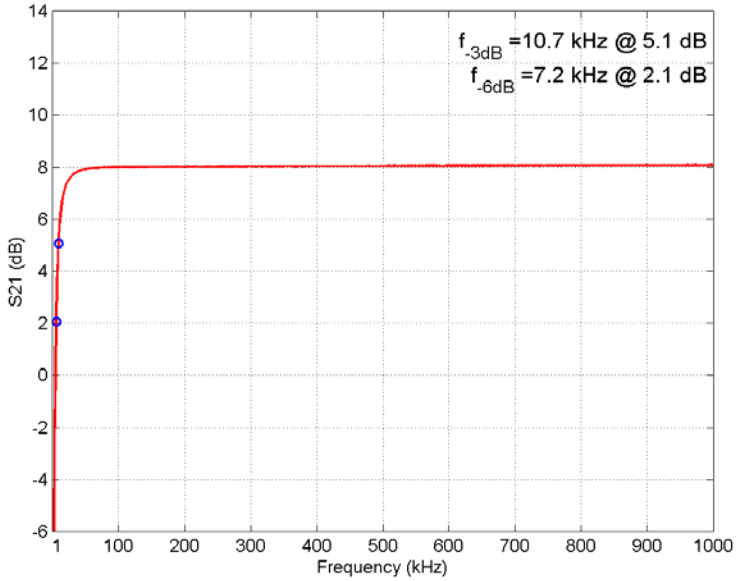
Rise time: 15.78 ps — Measured from 10% to 90% — Rise time: 15.78 ps



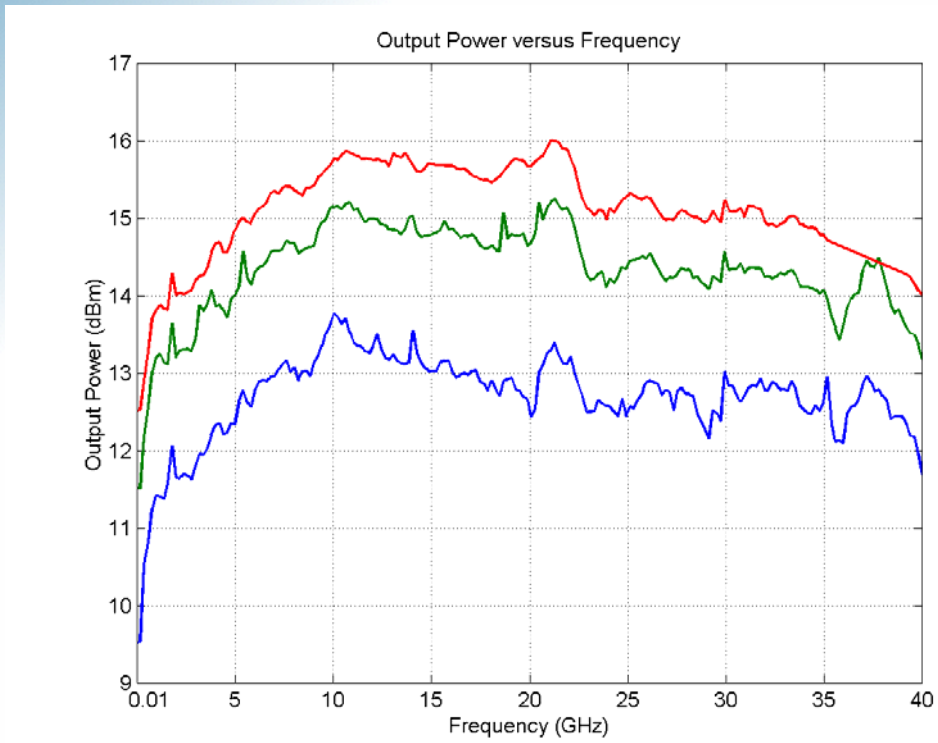


Rise time: 10.44 ps — Measured from 20% to 80% — Rise time: 10.44 ps

Low frequency response (<1 MHz)

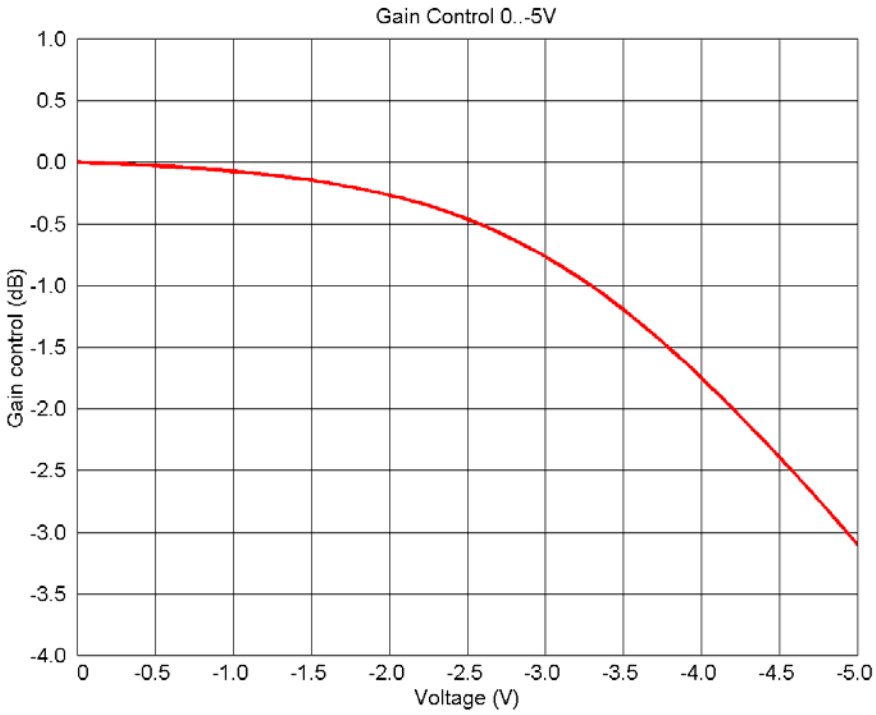


Saturation power



Top (red): 3 dB compression; Middle (green): 2 dB compression; Bottom (blue): 1 dB compression

Gain reduction function



All SHF amplifiers have a feature which allows the output gain to be reduced by up to approximately 3dB by applying a negative voltage to the gain reduction pin.

▪ Available Options

01: DC return on input

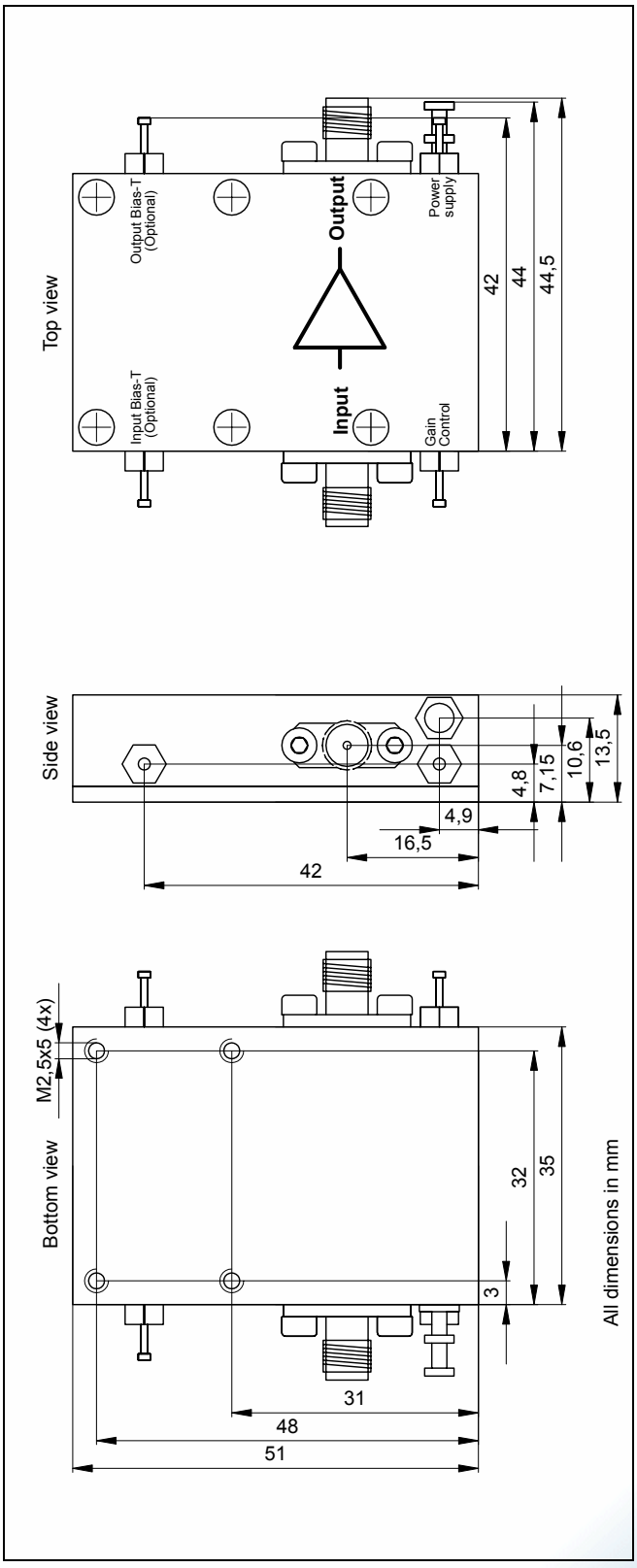
02: Built-in bias tee on input

03: DC return on output

04: Built-in bias tee on output

MP: Matches the phase of two amplifiers

The following options cannot be combined:
01 and 02
03 and 04
02 and 04



User Instructions

ATTENTION !

Electrostatic sensitive GaAs FET amplifier

1. To prevent damage through static charge build up, cables should be always discharged before connecting them to the amplifier!

2. The supply voltage can be taken from any regular 5.2…9 V, 0.13 A DC power supply and can be connected to the supply feedthrough filter via an ON/OFF switch.

3. The minimum supply voltage is 5.2 V. A higher one increases the power dissipation of the internal voltage stabilizer.

4. Using a 3 dB or 6 dB input attenuator will result in a 6 dB or 12 dB increase of the input return loss. For minimal degradation of amplifier rise time, these attenuators should have a bandwidth specification of greater than 65 GHz (V/1.85mm attenuators)!

5. An input signal of about 1.6 V_{pp} (equivalent to 8 dBm) will produce a saturated output swing of 2.8V_{pp}.

6. Higher input voltages will drive the output stage of the amplifier into saturation, leading to waveform peak clipping.

7. The input voltage should never be greater than 1.6 V_{pp} equivalent to 8 dBm input power.The input voltage without DC power supplied to the amplifier should never be greater than 2.8 V_{pp} (equivalent to 13 dBm input power).