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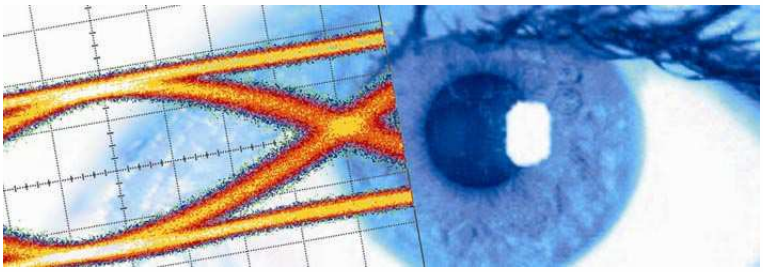
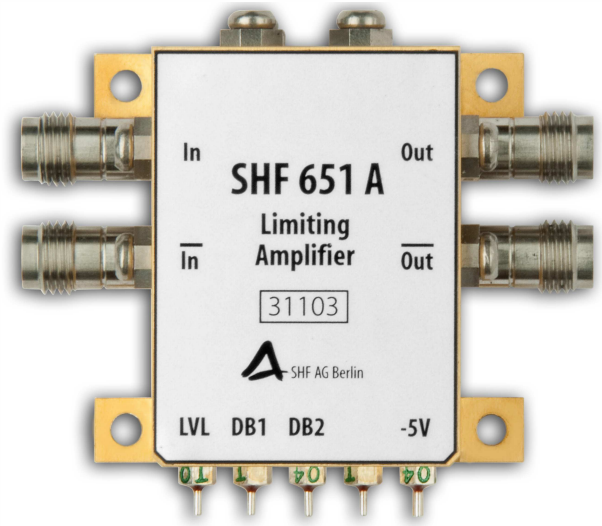


Datasheet

SHF 651 A

Limiting Amplifier



Description

The SHF 651 A Limiting Amplifier operates at data rates up to 56 Gbps and with clock signal up to 40 GHz for use in broadband test setups and telecom transmission systems. The AC-coupled differential inputs can be driven single ended as well by terminating the unused input. For input signals >150 mV the output voltage will be clipped to 650 mV.

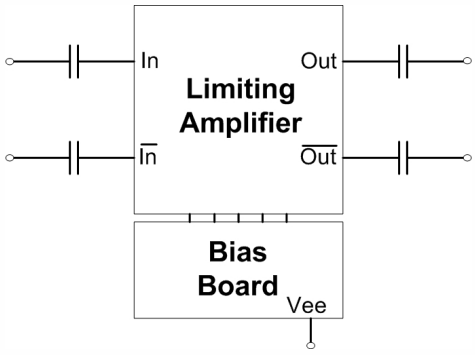
Features

- Supports data rates up to 56 GBit/s
- Supports clock frequencies up to 40 GHz
- Fast signal rise and fall times: < 8 ps
- Low power consumption: 650 mW
- Single-ended or differential input drive
- Differential output, 650 mV single ended output swing
- Bias Board
- Output Level Control

Applications

- 100G Ethernet development and prototyping
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block diagram



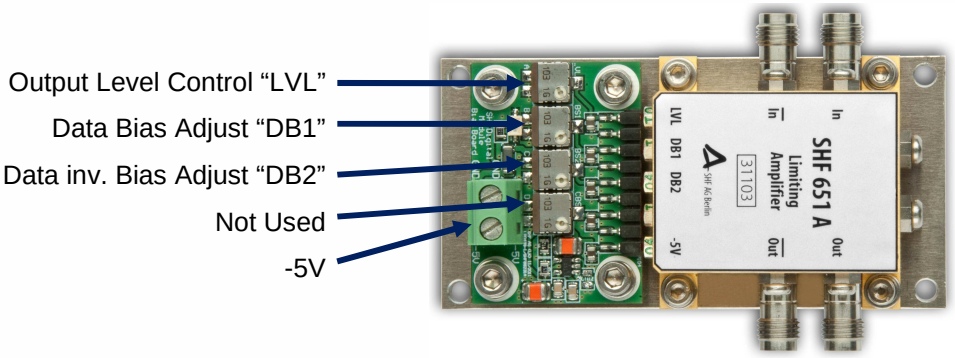
® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 651 A Limiting Amplifier. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level “LVL” and the input data bias voltages “DB1” and “DB2” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



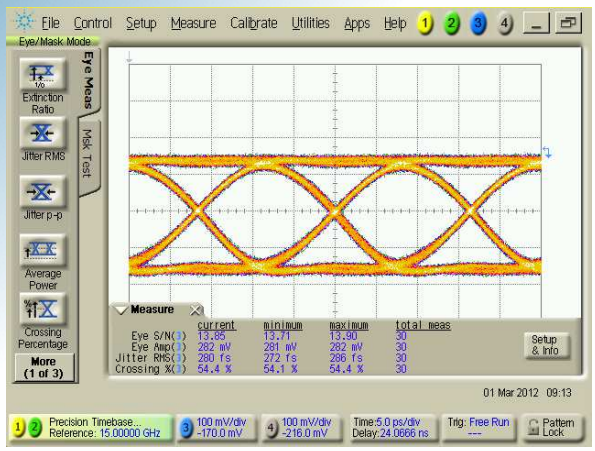
Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Minimum Data Rate	Gbps	$R_{in,min}$			1	
Maximum Data Rate	Gbps	$R_{in,max}$	50	56		
Input Amplitude	mV_{pp}	V_{in}			1000	
Input Sensitivity	mV_{pp}	V_{in}	80	50		See page 9
Output Parameters						
Output Amplitude	mV	V_{out}	580	650	900	Single ended, adjustable up to -3dB
Output Jitter, RMS value[1]	fs	J_{rms}		500	800	
Small Signal Gain	dB	G_p	20	22		$T_{ambient}$=25℃
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		130	150	
Power Dissipation	mW	P_d		650		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Output Level Adjust	V	LVL	-3.3		0	if not used, connect to gnd
Input Data Bias	V	DB1	-3.3	-1,65	0	
Input inv. Data Bias	V	DB2	-3.3	-1,65	0	
Conditions						
Operating Temperature	℃	$T_{ambient}$	15		35	

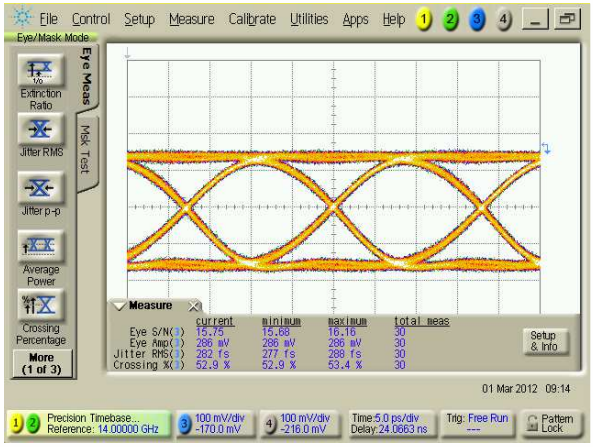
[1] Test condition: Input Signal $Jitter_{RMS}$ = 280 fs

Typical Output Eye Diagrams

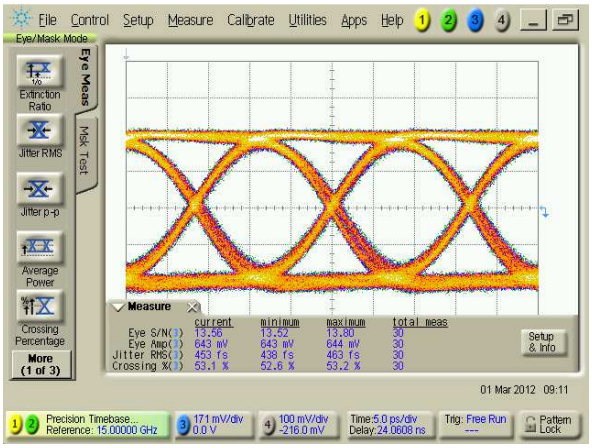
The measurements shown below had been performed using a SHF 12103 A BPG (PRBS 2^{31}-1), an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the Limiting Amplifier had been connected directly to the DCA input.



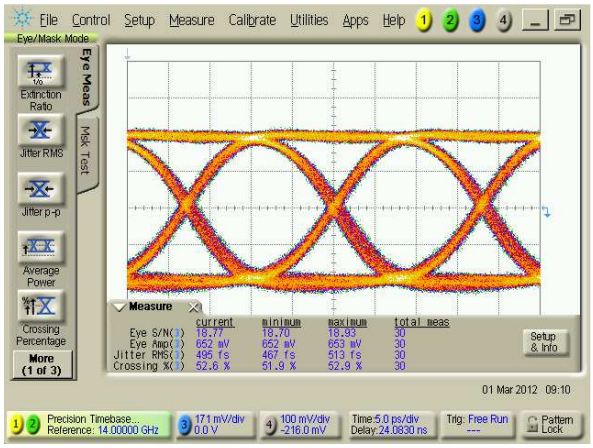
Input @ 60 Gbps



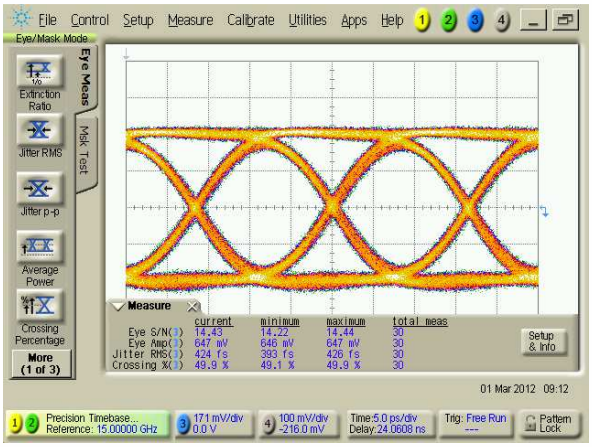
Input @ 56 Gbps



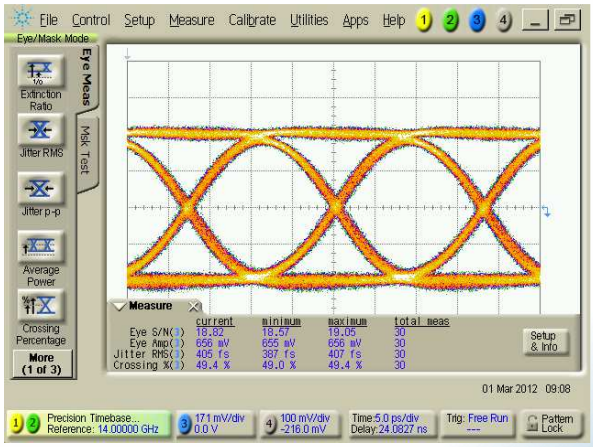
Output @ 60 Gbps



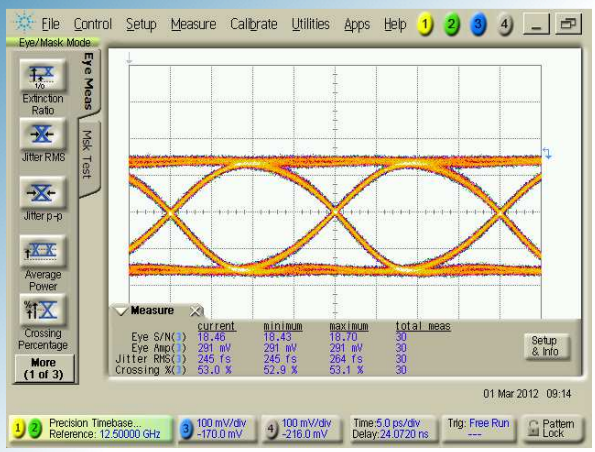
Output @ 56 Gbps



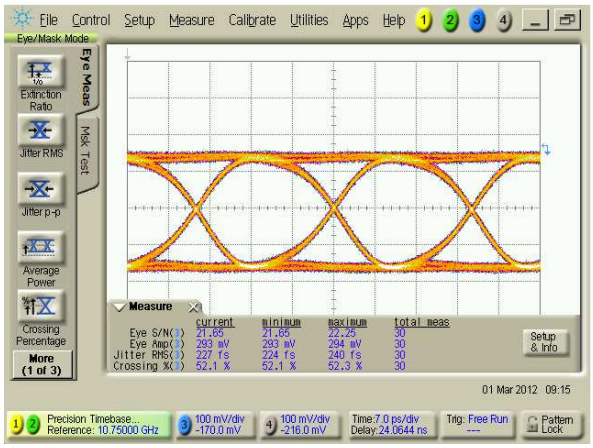
Output inv. @ 60 Gbps



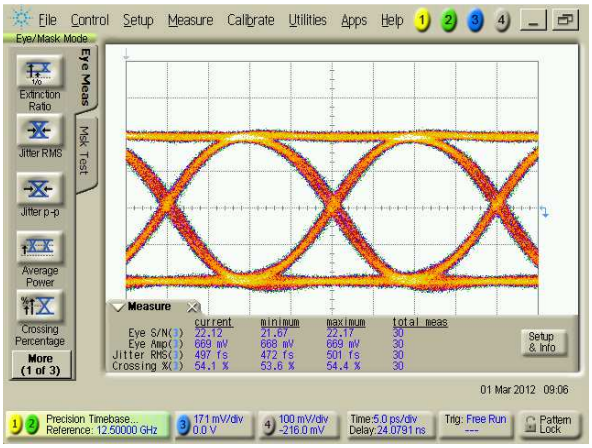
Output inv. @ 56 Gbps



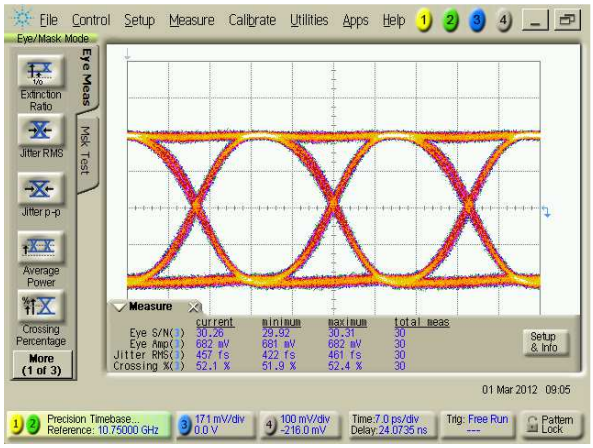
Input @ 50 Gbps



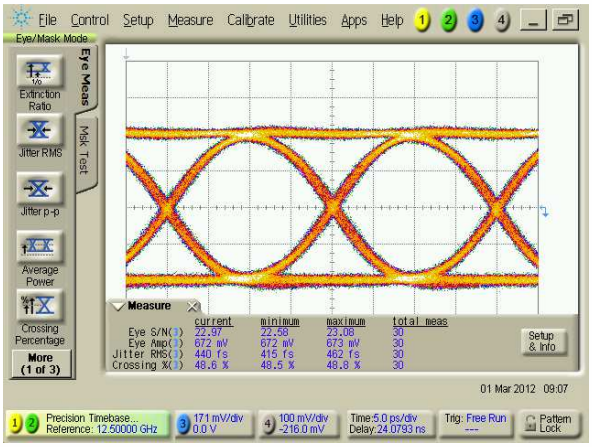
Input @ 43 Gbps



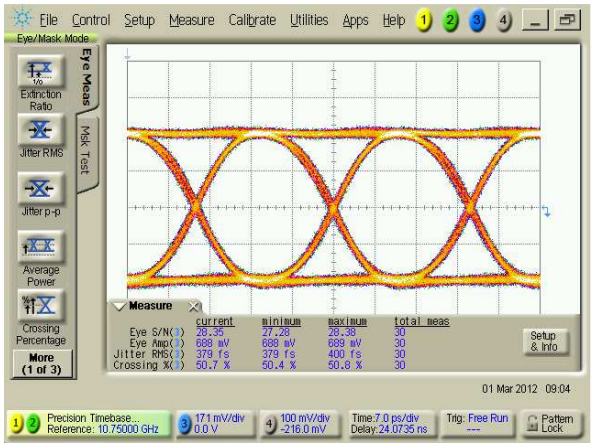
Output @ 50 Gbps



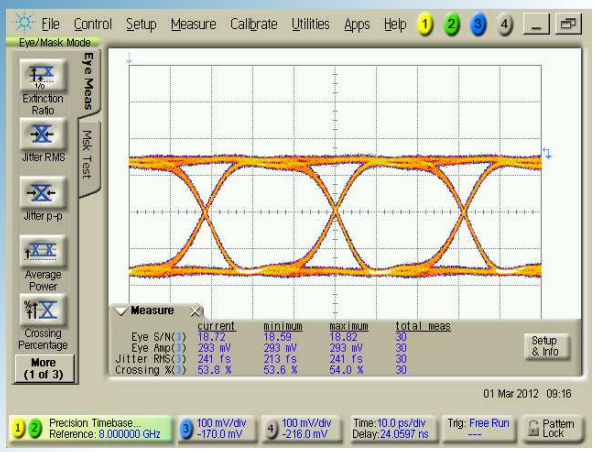
Output @ 43 Gbps



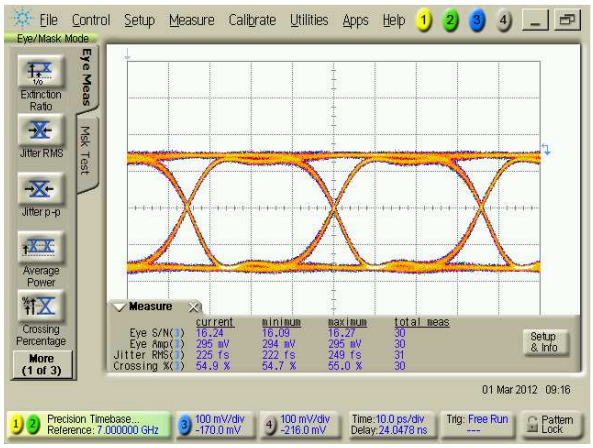
Output inv. @ 50 Gbps



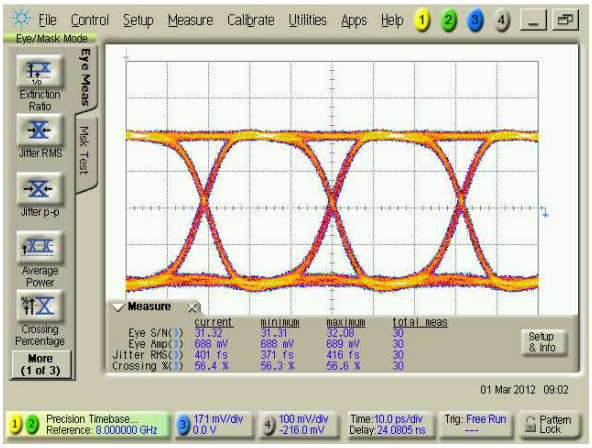
Output inv. @ 43 Gbps



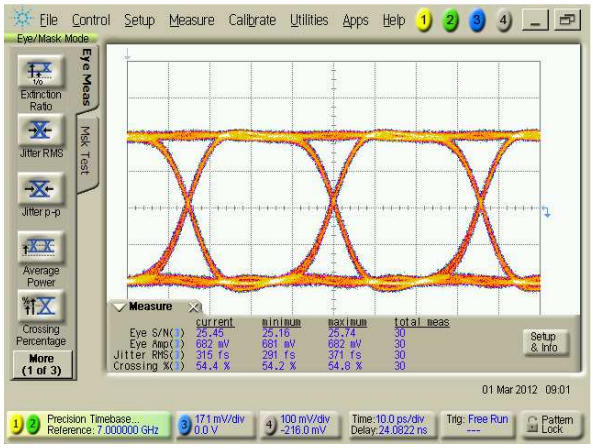
Input @ 32 Gbps



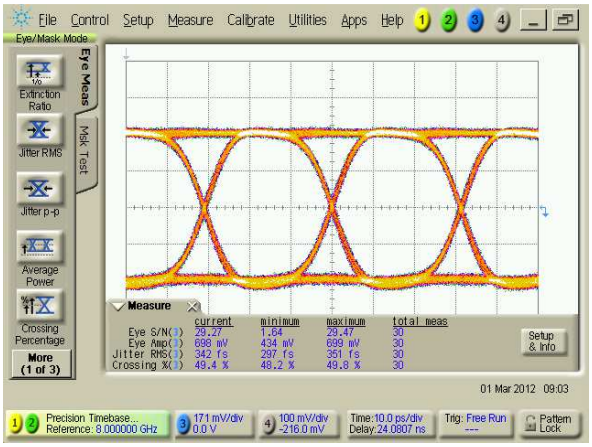
Input @ 28 Gbps



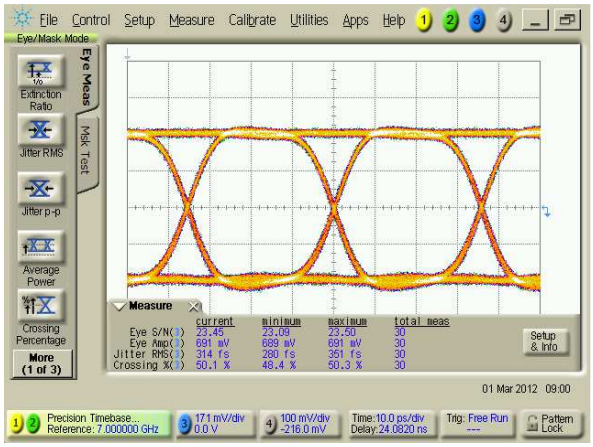
Output @ 32 Gbps



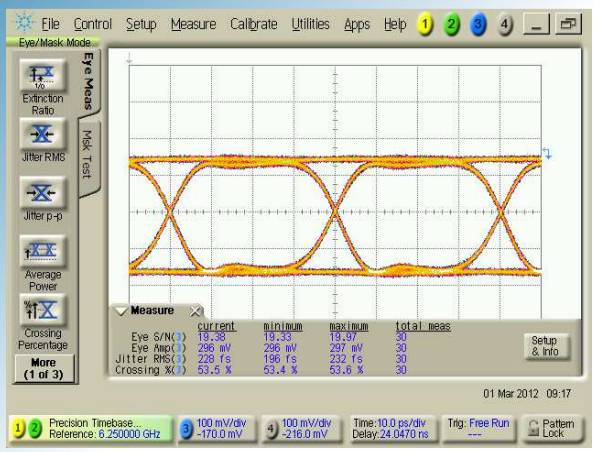
Output @ 28 Gbps



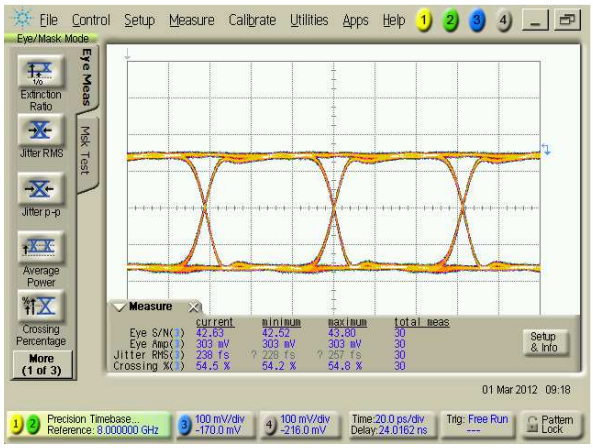
Output inv. @ 32 Gbps



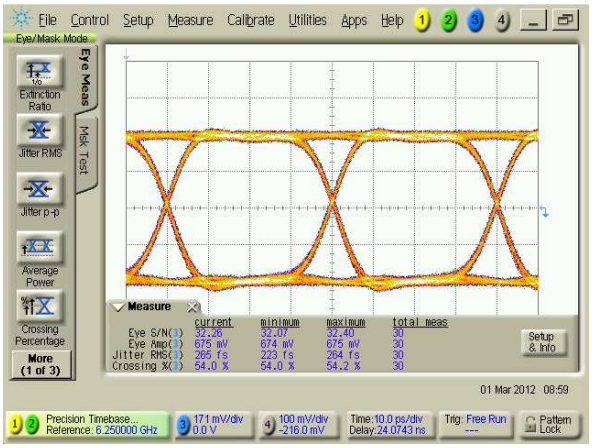
Output inv. @ 28 Gbps



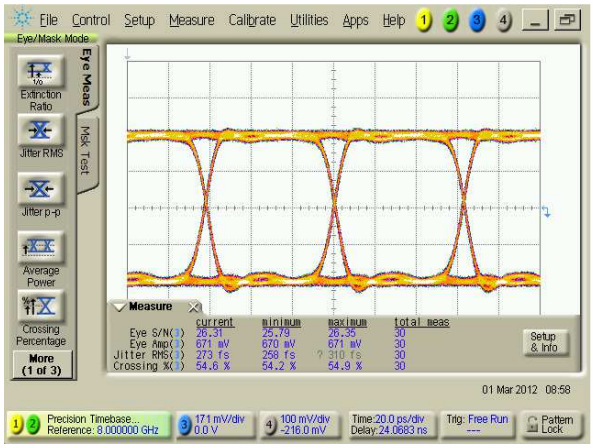
Input @ 25 Gbps



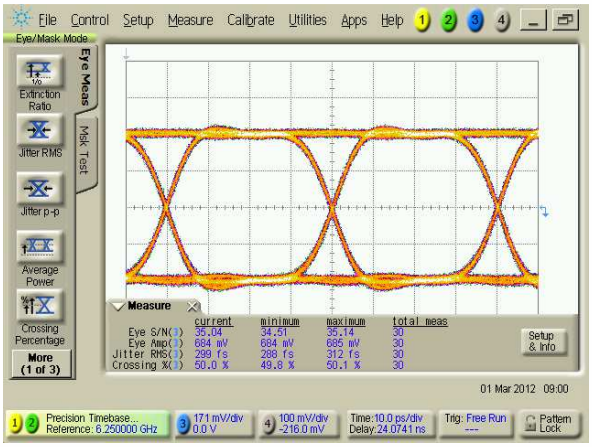
Input @ 16 Gbps



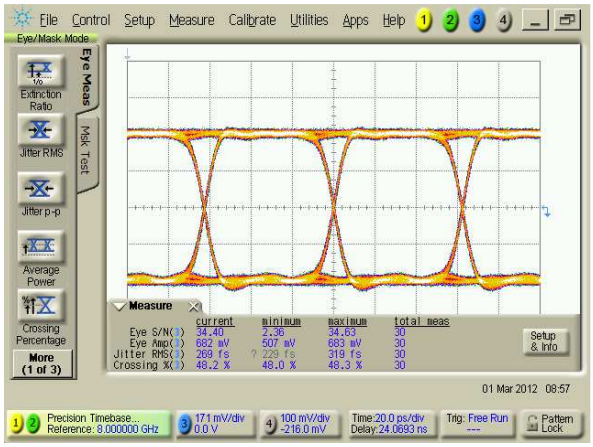
Output @ 25 Gbps



Output @ 16 Gbps



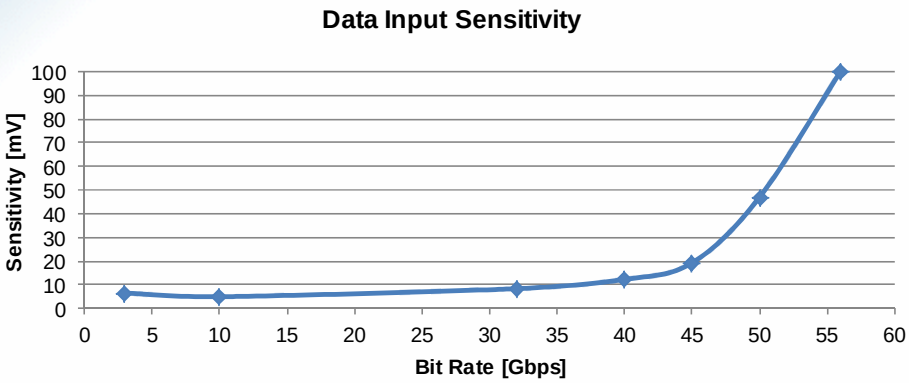
Output inv. @ 25 Gbps

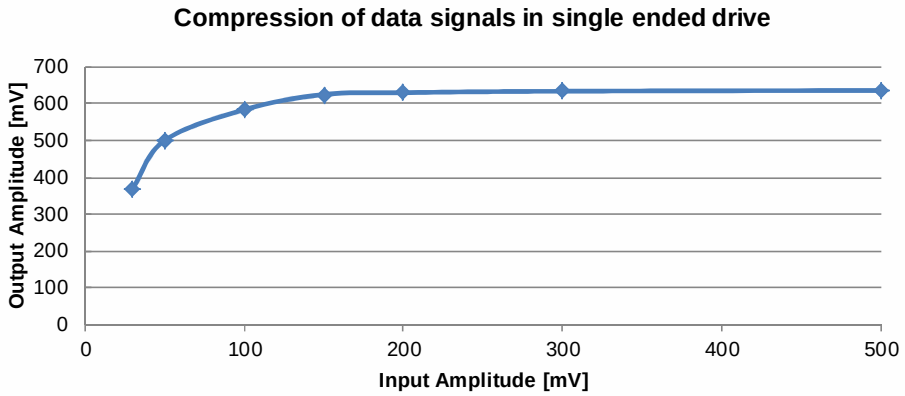


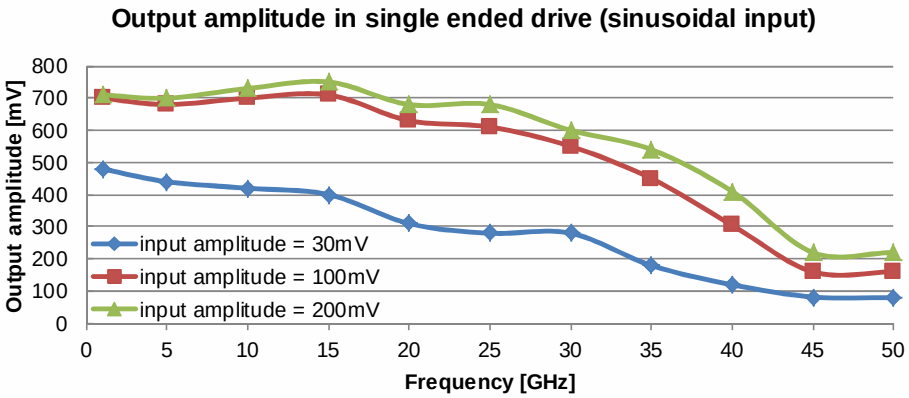
Output inv. @ 16 Gbps

Typical Results

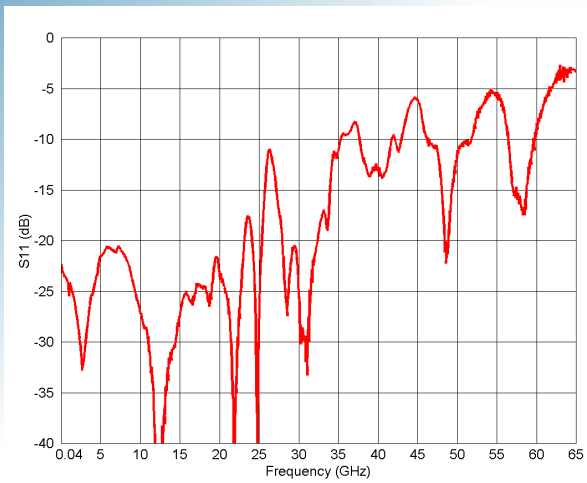
The measurements shown below had been performed using a SHF 12103 A BPG (PRBS 2^{31}-1), a SHF 11100 A Error Analyzer, an Agilent 86100D DCA with Precision Time Base Module (86107A) and a 70 GHz Sampling Head (86118A) to determine the output amplitude. In case of the sensitivity measurement the input signal had been reduced until a BER limit of $<10^{-9}$ had been achieved.

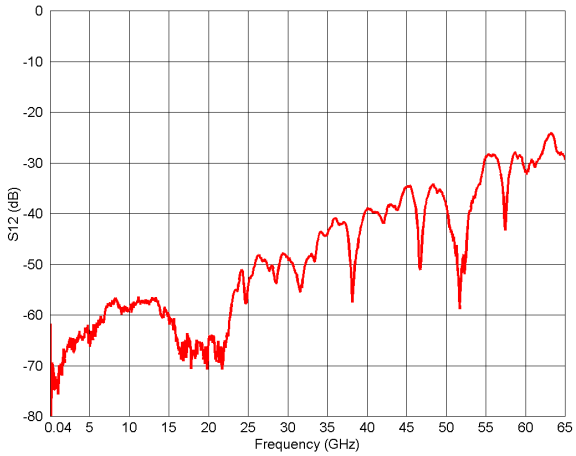


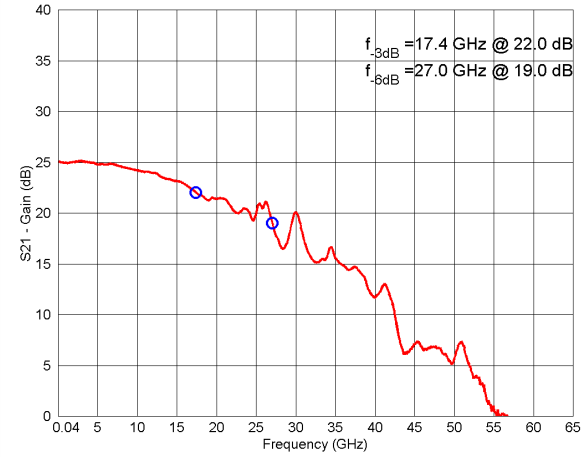


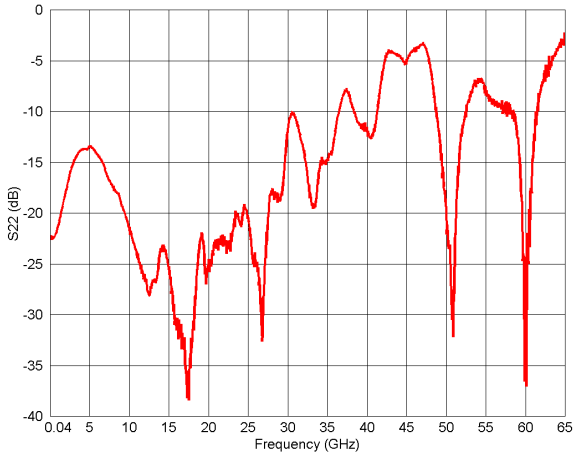


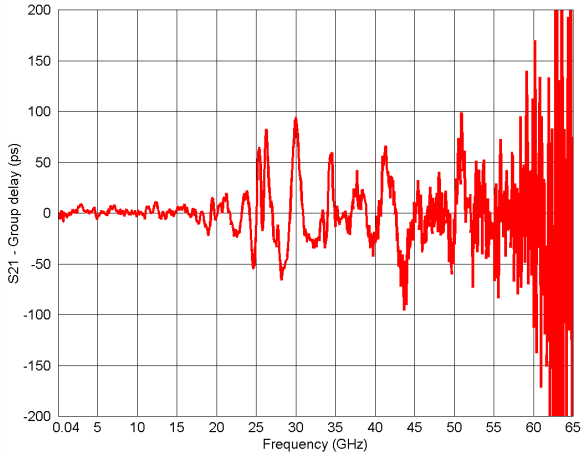
Typical S-Parameters

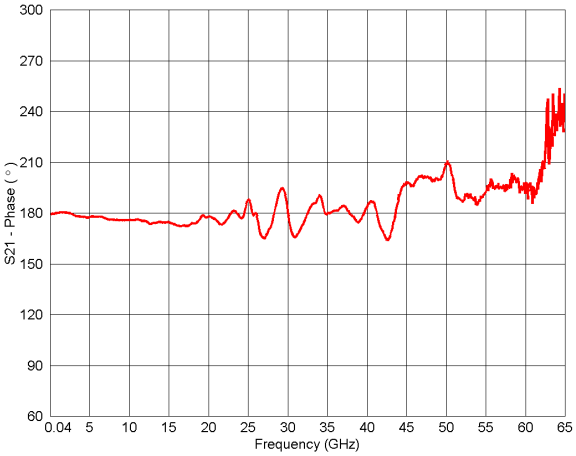






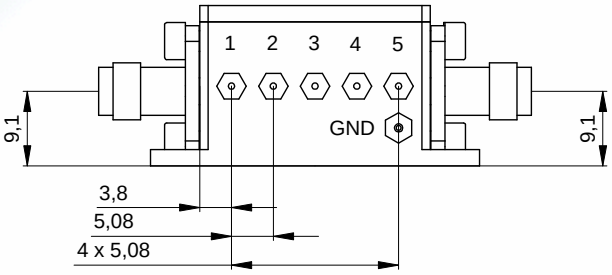


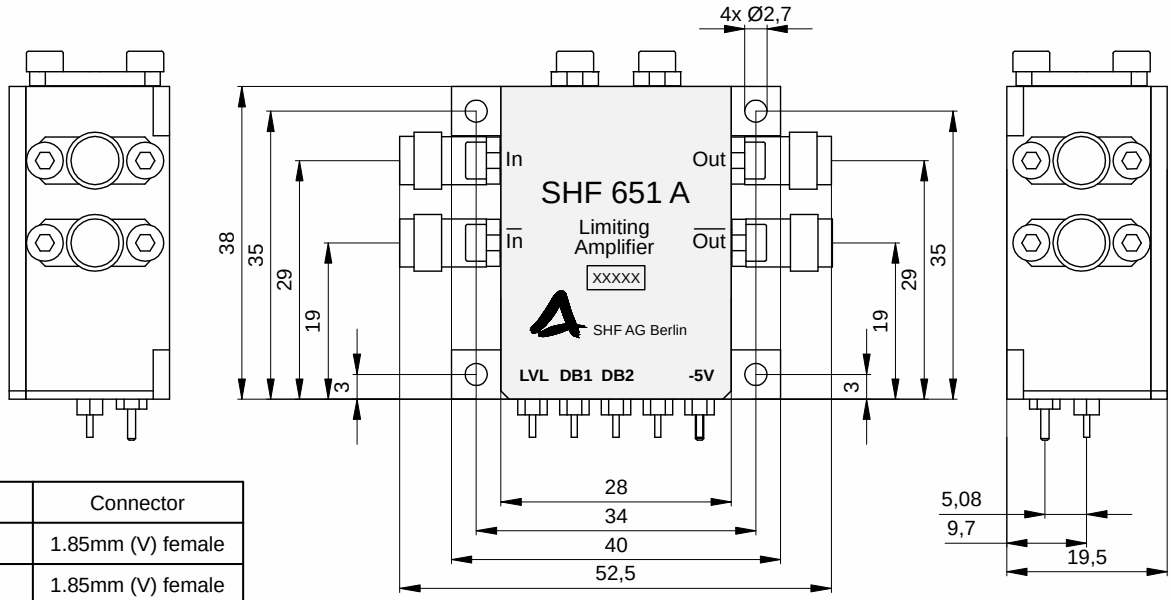




Aperture of Group Delay measurement: 100 MHz

Outline Drawing





Port	Connector
In	1.85mm (V) female
$\overline{\text{In}}$	1.85mm (V) female
Y	1.85mm (V) female
$\overline{\text{Y}}$	1.85mm (V) female

Pin	Designation
1	Level (LVL)
2	Data Bias 1 (DB1)
3	Data Bias 2 (DB2)
4	nc
5	-5V