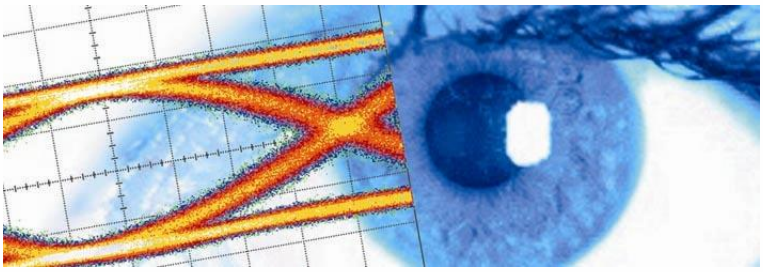
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany

Phone +49 30 772051-0 • Fax +49 30 7531078

E-Mail: sales@shf.de • Web: http://www.shf.de

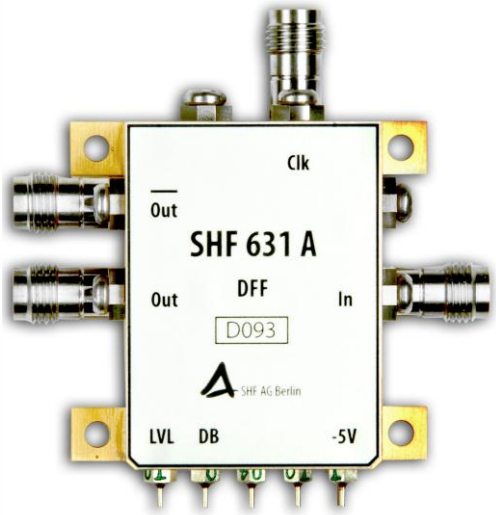


Datasheet

SHF 631 A

56 Gbps

D Flip Flop (DFF)



Description

The SHF 631 A is a re-timing and re-shaping D Flip-Flop (DFF) module capable of broadband operation up to 56 Gbps. AC-coupled and 50 Ω terminated data and clock inputs ensure proper line termination and uncomplicated application. Optimum bias point for the data input can be set using the potentiometer on the provided bias board.

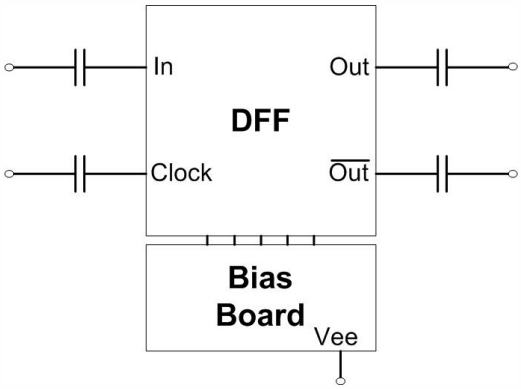
Features

- Broadband operation up to 56 Gbps
- Single ended inputs (data and clock)
- Differential output, 700 mV single ended output swing
- Output Level Control
- Bias Board

Applications

- 100G Ethernet development and prototyping
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block Diagram



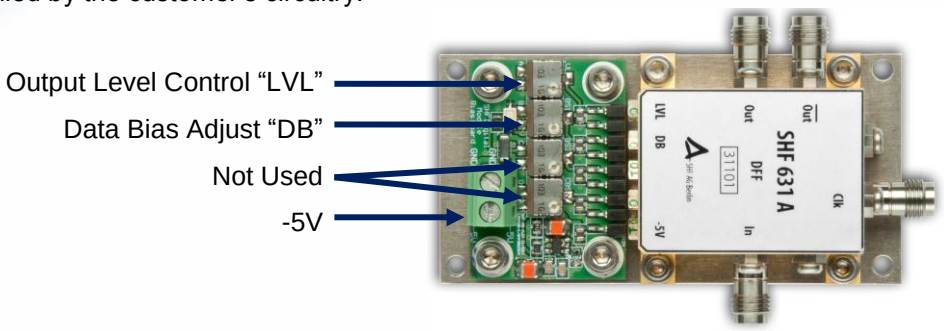
® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 631 A DFF. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level “LVL” and the input data bias “DB” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Minimum Input Data Rate	Gbps	$R_{in,min}$		1	2	@ 500mV$_{pp}$ clock input
Maximum Input Data Rate	Gbps	$R_{in,max}$	56			@ 500mV$_{pp}$ clock input
Data Input Voltage	mV$_{pp}$	$V_{data\ in}$			1000	
Data Input Sensitivity	mV	$V_{data\ in}$	100[1]			Eye Height, see page 8
Clock Input Frequency	GHz	f_{in}	2		56	
Clock Input Voltage	mV$_{pp}$	$V_{clk\ in}$	500[2]		1000	See page 8
Clock Phase Margin[3]	°	CPM	200 160			Up to 50 Gbps, Above 50 Gbps, see page 8
Output Parameters						
Output Amplitude	mV	V_{out}	600	700	900	Single ended, adjustable up to -3dB
Rise / Fall time	ps	t_r/t_f		7	10	20% / 80%
Output Jitter, RMS value[4]	fs	J_{rms}		400	600	
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		250	280	
Power Dissipation	mW	P_d		1250		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Output Level Adjust	V	LVL	-3.3		0	if not used, connect to gnd
Input Data Bias	V	DB	-3.3	-1,65	0	
Conditions						
Operating Temperature	°C	$T_{ambient}$	15		35	

[1] Test criteria: BER<10^{-9} ; to achieve best output eye performance, value should be higher

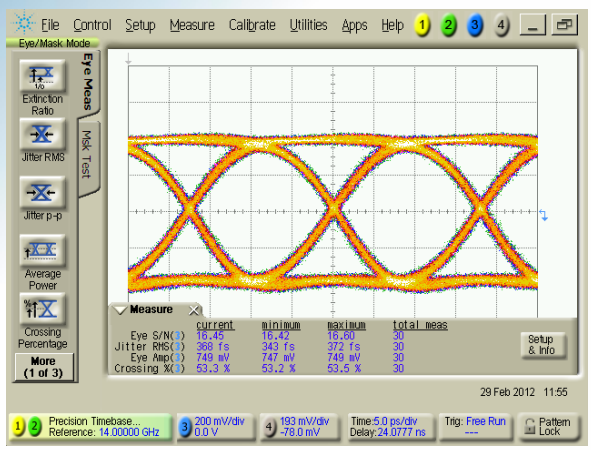
[2] Test criteria: BER<10^{-9} ; to achieve best output eye performance, value should be higher

[3] $$\text{Clock Phase Margin [deg]} = \frac{\text{Phase Margin (measured) [ps]} + \text{Peak - Peak - Source - Jitter [ps]}}{\text{Eye Length [ps]}} \cdot 360°$$

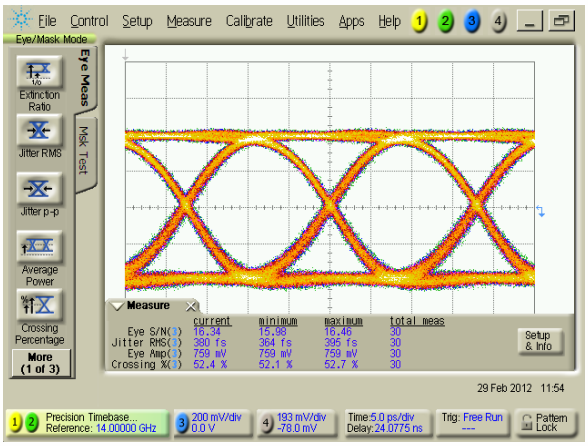
[4] Test condition: Input Signal Jitter$_{RMS}$ = 230 fs

Typical Output Eye Diagrams

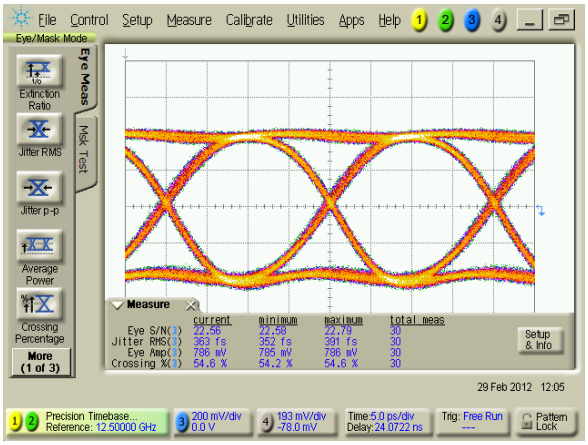
The measurements below had been performed using a SHF 12100 A Bit Pattern Generator (PRBS 2^{31}-1, $V_{amplitude}$ = 350 mV) and an Agilent 86100D Digital Communication Analyzer (DCA) with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the DFF module had been connected directly to the DCA input.



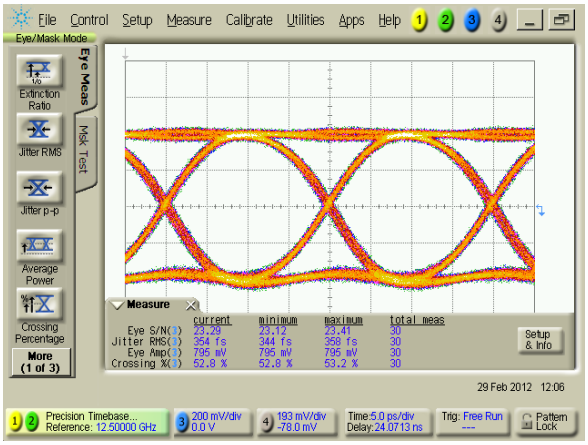
Out @ 56 Gbps



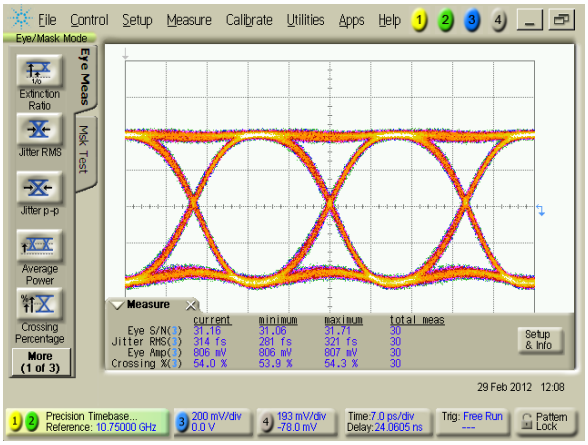
Out! @ 56 Gbps



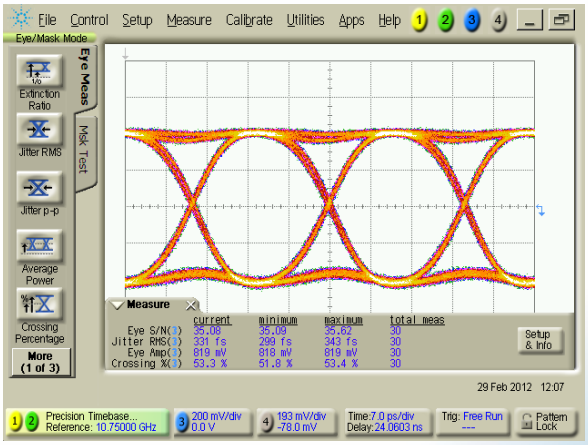
Out @ 50 Gbps



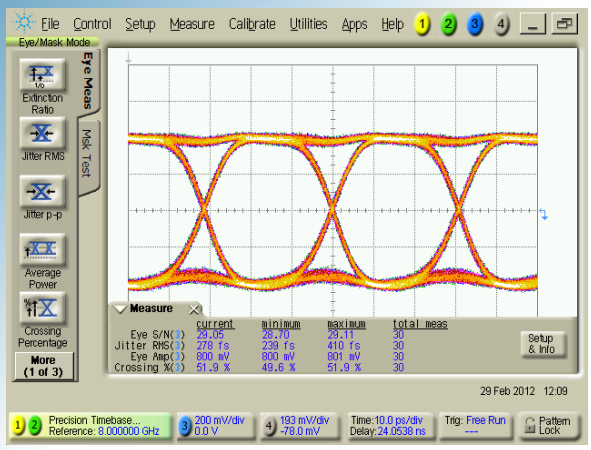
Out! @ 50 Gbps



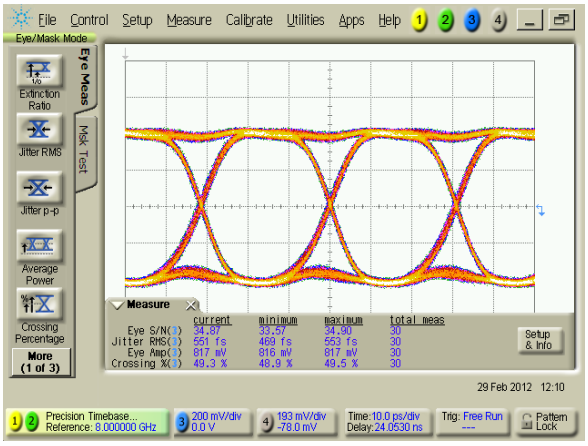
Out @ 43 Gbps



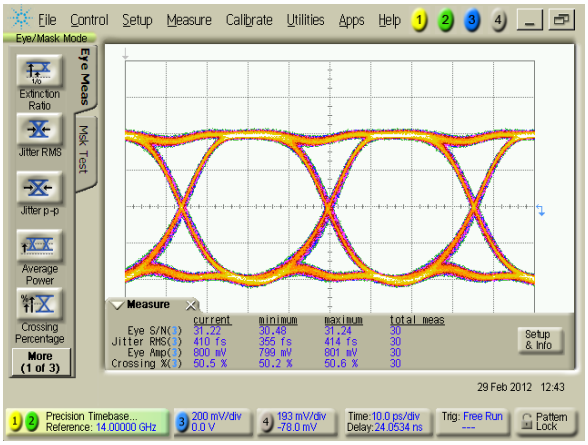
Out! @ 43 Gbps



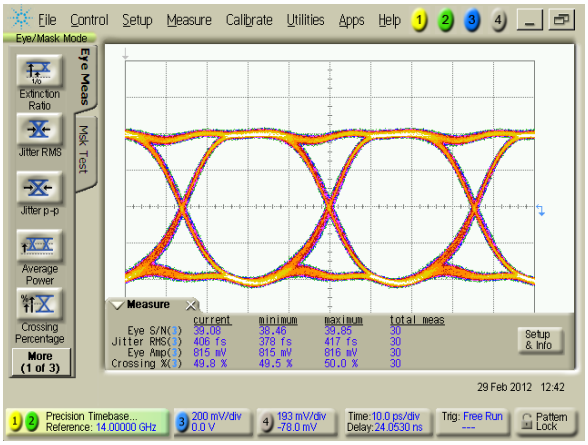
Out @ 32 Gbps



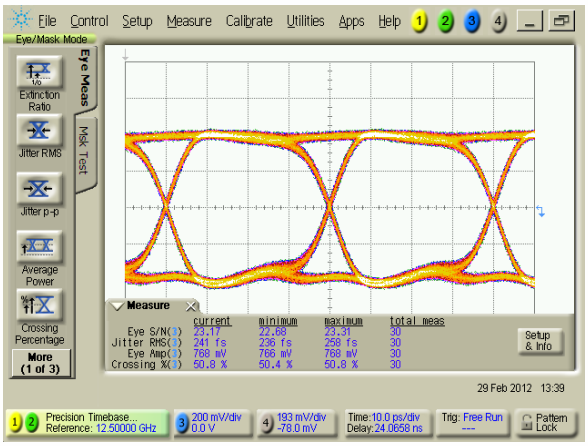
Out! @ 32 Gbps



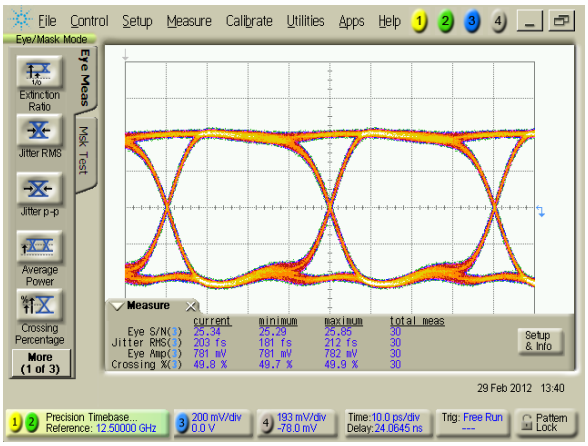
Out @ 28 Gbps



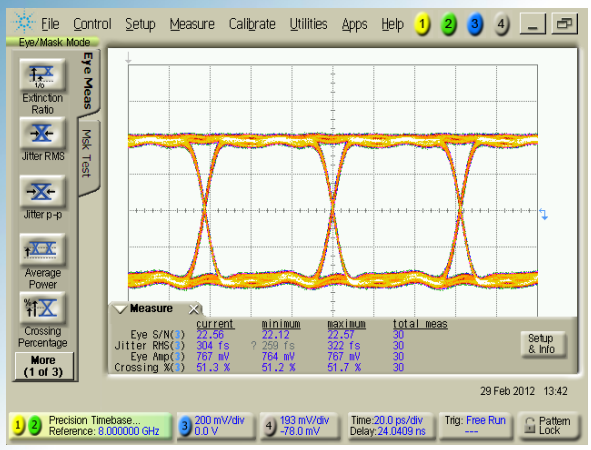
Out! @ 28 Gbps



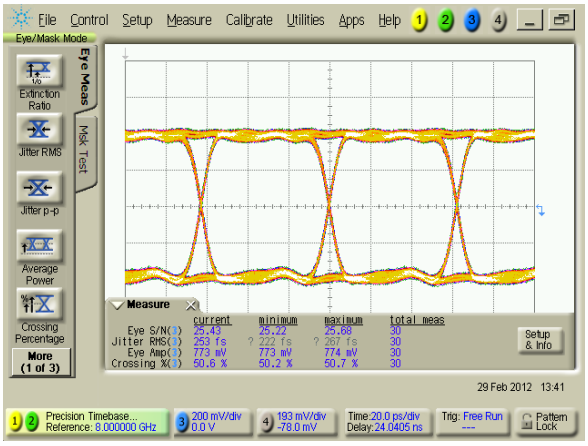
Out @ 25 Gbps



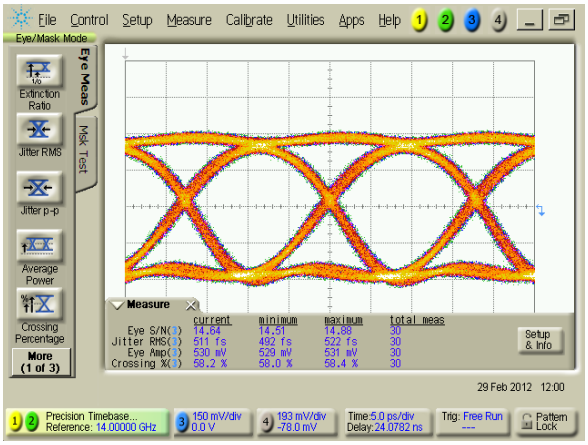
Out! @ 25 Gbps



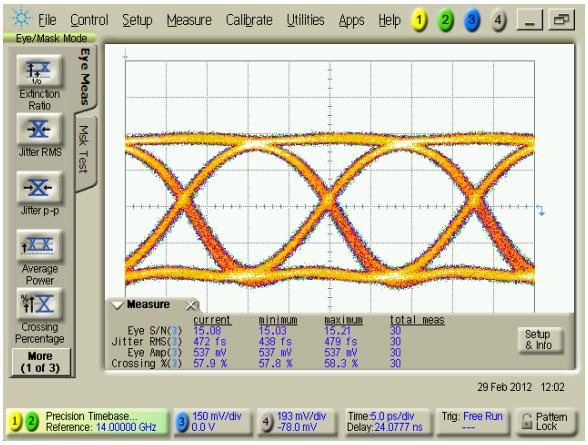
Out @ 16 Gbps



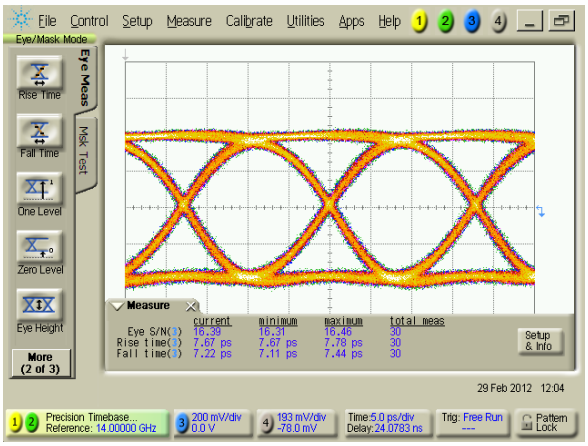
Out! @ 16 Gbps



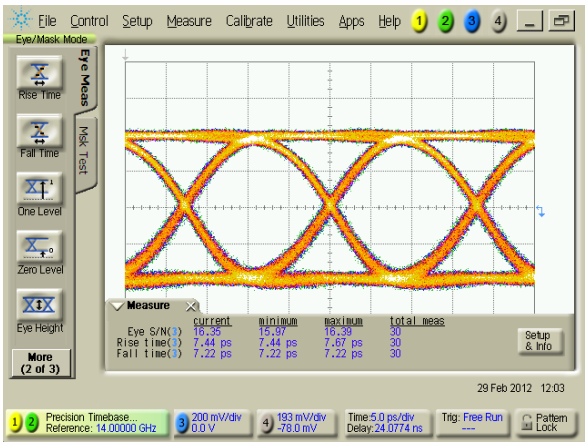
Out @ 56 Gbps, Level = -3dB



Out! @ 56 Gbps, Level = -3dB



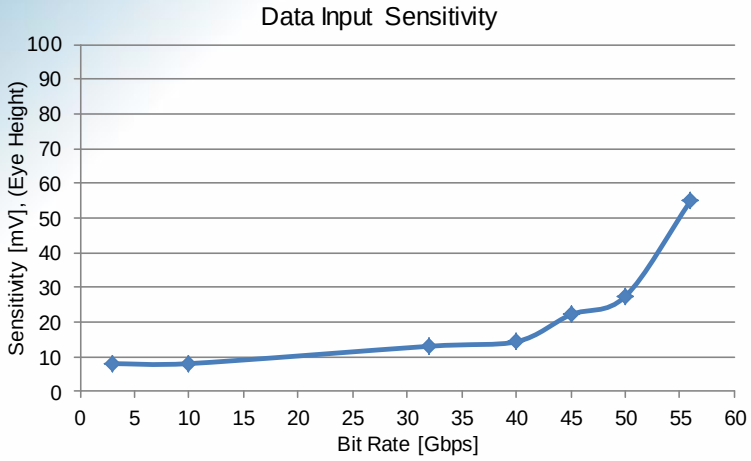
Out @ 56 Gbps, t_r/t_f



Out! @ 56 Gbps, t_r/t_f

Typical Results

The measurements shown below had been performed using a SHF 12103 A Bit Pattern Generator (PRBS 2^{31}-1), a SHF 11100 A Error Analyzer, an Agilent 86100B Digital Communication Analyzer with Precision Time Base Module (86107A) and a 70 GHz Sampling Head (86118A) to determine the eye height and jitter contribution of the input signal.

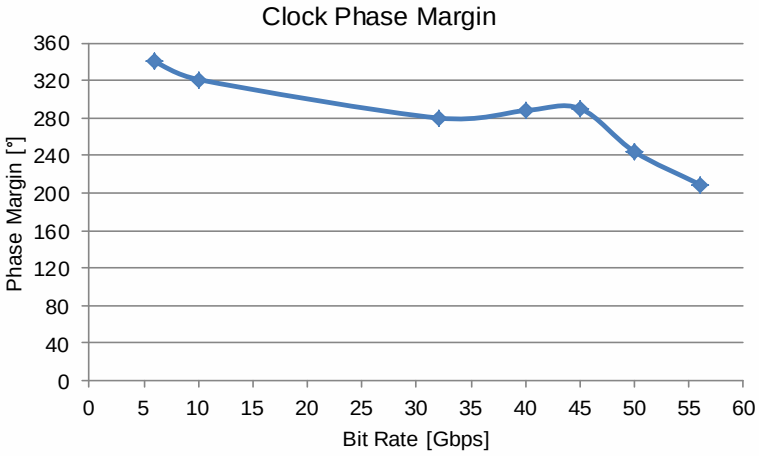


Measurement Conditions:

Clock Input Amplitude: 500mV$_{pp}$

Clock Input Jitter: 230fs

BER-Limit: 10^{-9}



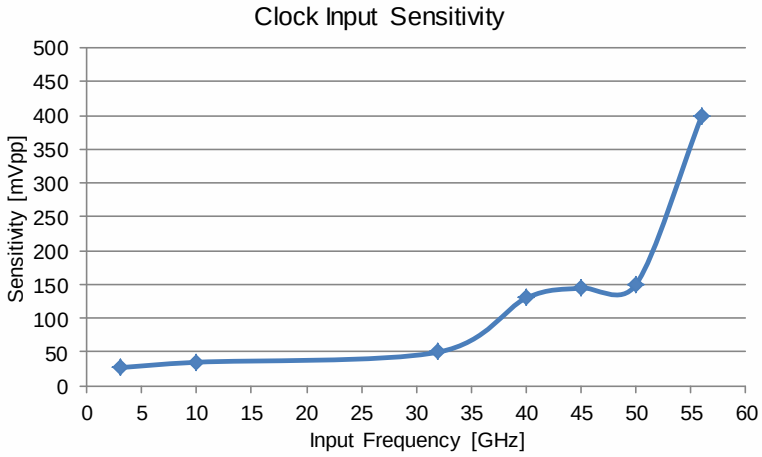
Measurement Conditions:

Data Input Eye Height: 100mV

Clock Input Amplitude: 500mV$_{pp}$

Clock Input Jitter: 230fs

BER-Limit: 10^{-9}



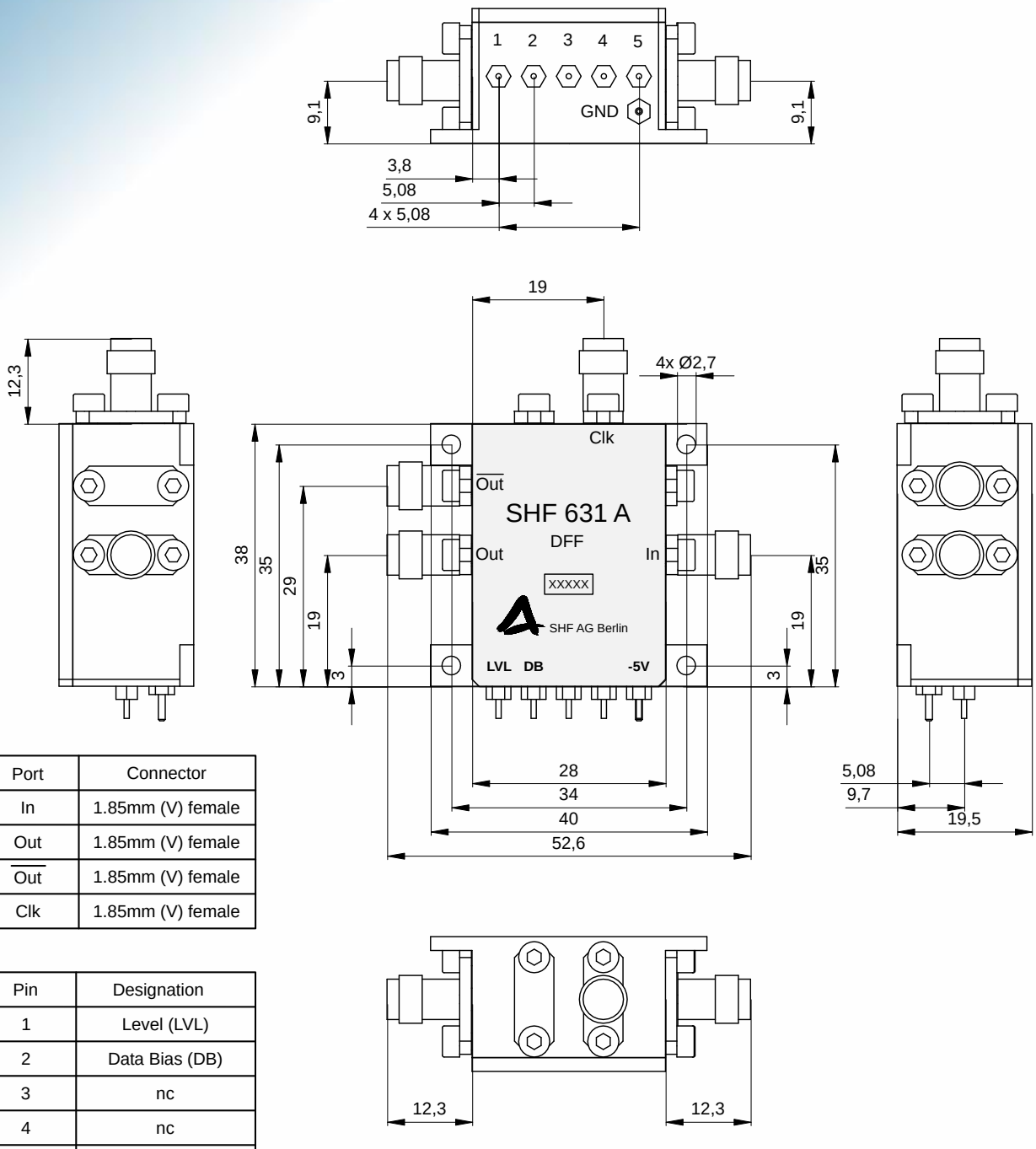
Measurement Conditions:

Data Input Eye Height: 100mV

Clock Input Jitter: 230fs

BER-Limit: 10^{-9}

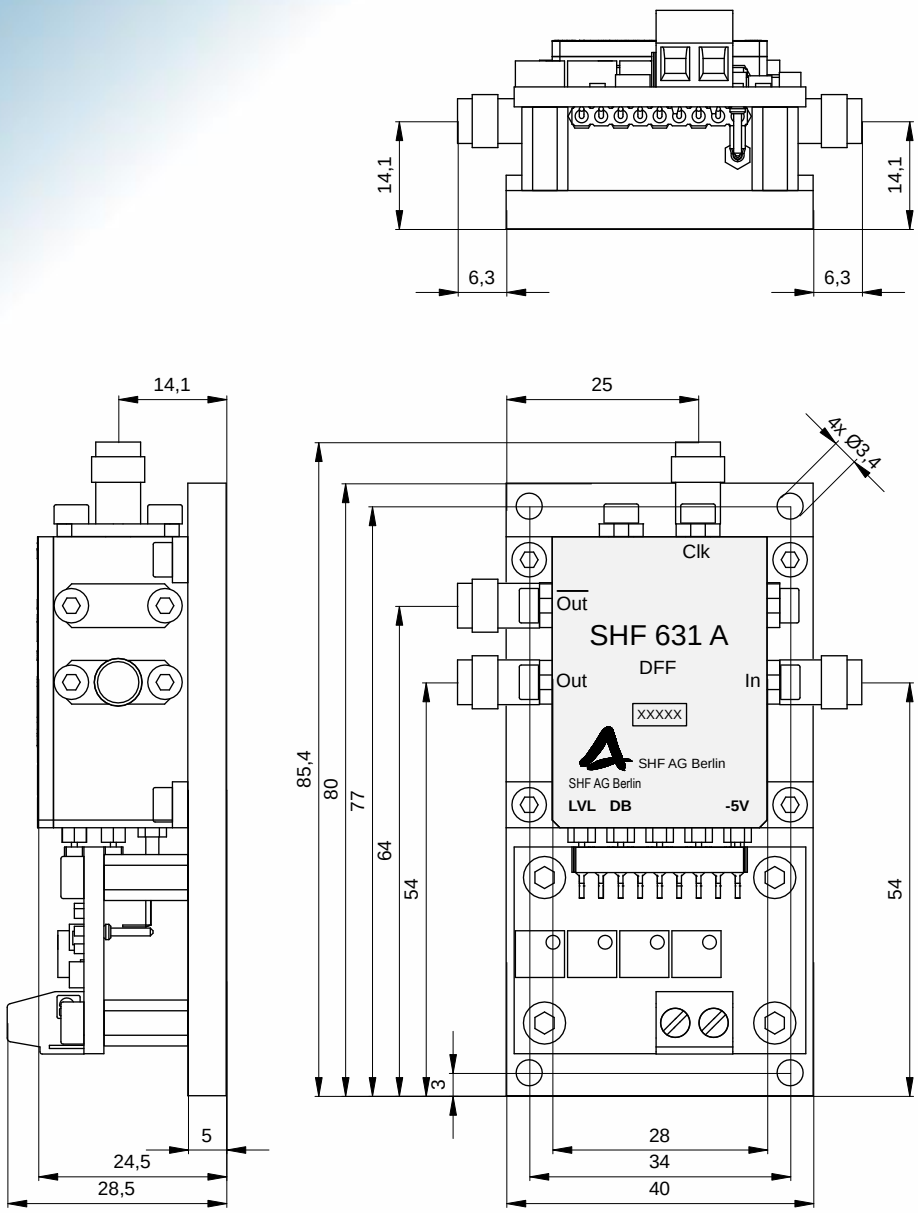
Outline Drawing – Module



Port	Connector
In	1.85mm (V) female
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
Clk	1.85mm (V) female

Pin	Designation
1	Level (LVL)
2	Data Bias (DB)
3	nc
4	nc
5	-5V

Outline Drawing – “Module + Bias Board”- Assembly



Port	Connector
In	1.85mm (V) female
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
Clk	1.85mm (V) female