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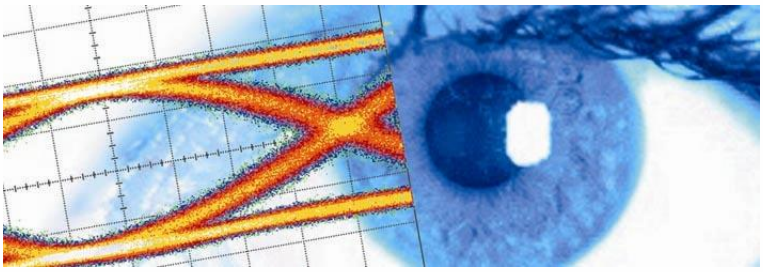


Datasheet

SHF 623 B

120 Gbps

1:2 Demultiplexer

Description

The SHF 623 B is a ROHS compliant 1:2 Demultiplexer operating at data rates up to 120 Gbps for use in broadband test setups and telecom transmission systems. An 120 Gbps single ended or differential serial data stream is accepted by the multiplexer and converted into two single ended data signals at a output data rate of 60 Gbps. A single ended clock signal with a frequency half of the input data rate drives the SHF 623 B. All RF in- and output ports are AC-coupled and internally terminated with 50 Ohm to GND. Unused in- or output ports should be terminated with 50 Ohm.

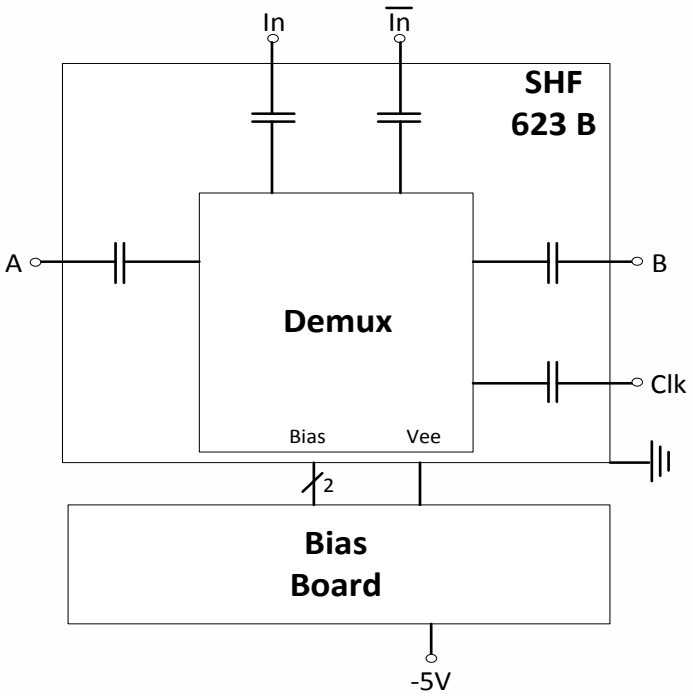
Features

- Broadband operation up to 120 Gbps
- Differential data input
- Data Input Sensitivity <100 mV
- Single ended data outputs
- Bias Board

Applications

- 100G, 200G and 400G system evaluation & development
- Telecom transmission
- Broadband test and measurement equipment

Block Diagram

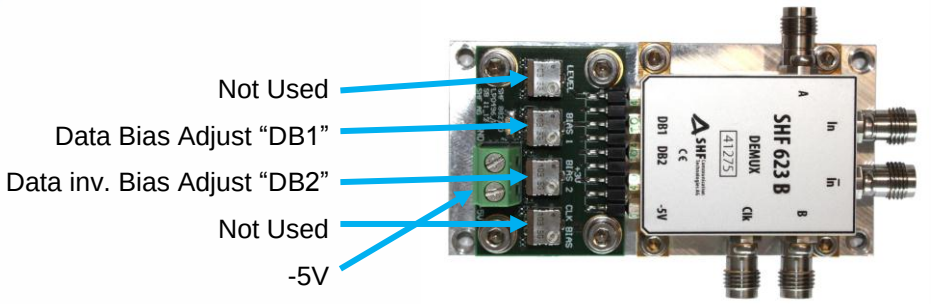


Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 623 B DEMUX. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust input data bias voltages “DB1” and “DB2” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$			900	Peak-to-Peak
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on Data Input Ports	V	V_{DCin}	-3		+3	AC coupled input
External DC Voltage on Clock Input Port	V	V_{DCin}	-6		+6	AC coupled input
External DC Voltage on RF Output Ports	V	V_{DCout}	-6		+6	AC coupled output
DC Supply Voltage	V	V_{ee}	-5.5		0	

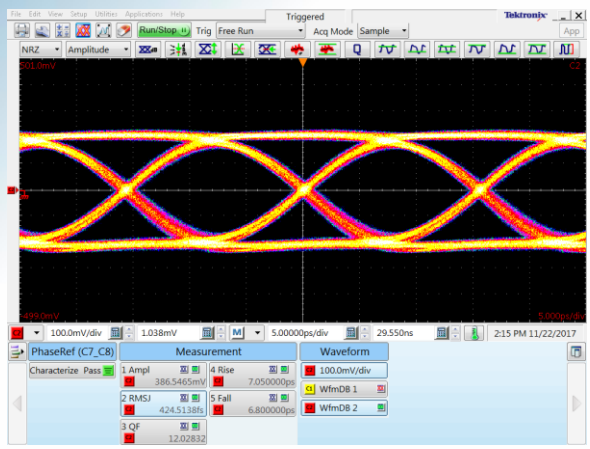
Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Minimum Input Data Rate	Gbps	$R_{in,min}$			10	
Maximum Input Data Rate	Gbps	$R_{in,max}$	120			
Data Input Voltage	mV	$V_{data\ in}$		400	800	Eye Amplitude
Data Input Sensitivity	mV	$V_{data\ in}$	120 70 50			> 110 Gbps > 64 Gbps ≤ 64 Gbps Eye height; On scope display
Min. Clock Input Frequency	GHz	$f_{in,min}$			5	
Max. Clock Input Frequency	GHz	$f_{in.max}$	60			
Clock Input Voltage	mV	$V_{clk\ in}$	300	400	800	Peak-to-Peak
Output Parameters						
Output Amplitude	mV	V_{out}	350	400		Eye Amplitude; Single ended
Rise / Fall time	ps	t_r/t_f		6.5	9	20% / 80%; On scope display
Output Jitter, RMS value[1]	fs	J_{rms}		400	600	
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		510	600	
Power Dissipation	mW	P_d		2550		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Input Data Bias	V	DB1	-3.3	-1,65	0	
Input inverted Data Bias	V	DB2	-3.3	-1,65	0	
Conditions						
Operating Temperature	°C	$T_{ambient}$	15		35	

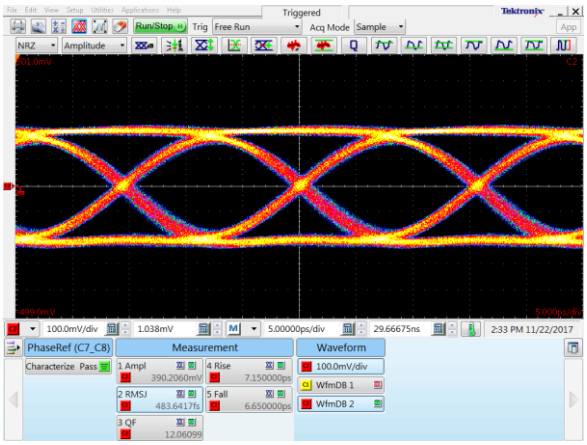
[1] Test condition: Input Signal $Jitter_{RMS}$ = 230 fs

Typical Output Eye Diagrams

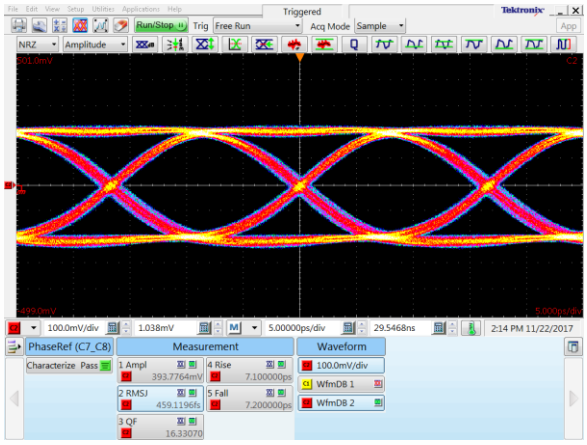
The measurements below had been performed using a SHF 603 A MUX (PRBS 2^{31}-1) and a Tektronix DSA8300 with Phase Reference Module (82A04B) and 70 GHz Sampling Head (80N01). The outputs of the demultiplexer module had been connected by 6 dB attenuators to the DSA input.



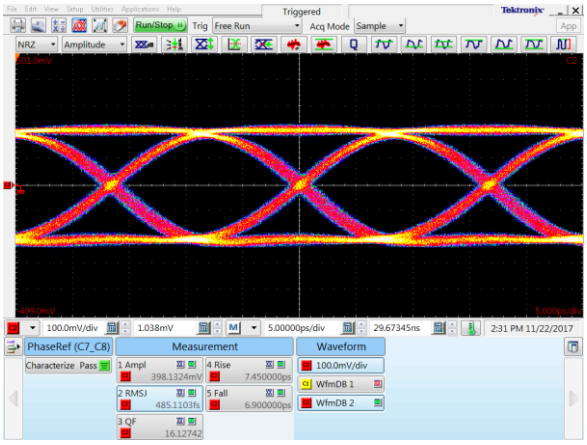
Out A @ 64 Gbps Output Bitrate



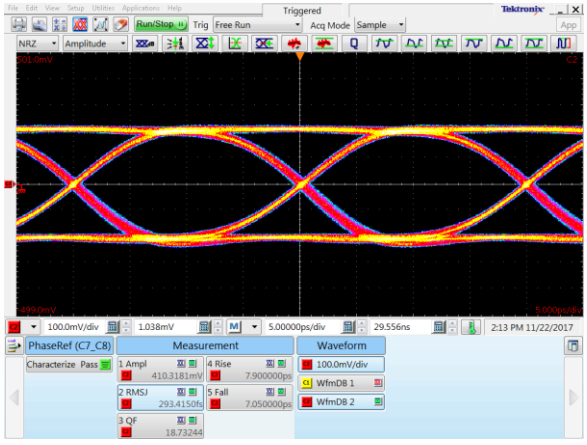
Out B @ 64 Gbps Output Bitrate



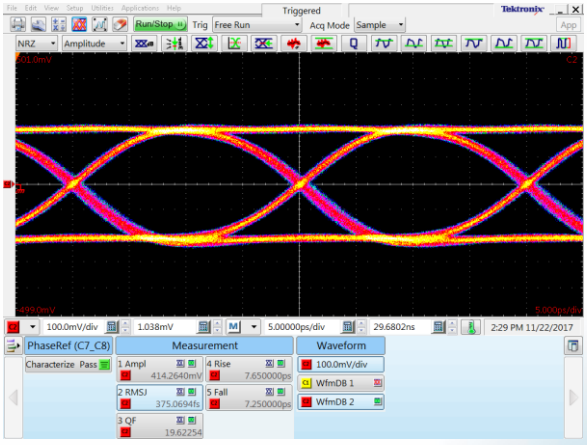
Out A @ 60 Gbps Output Bitrate



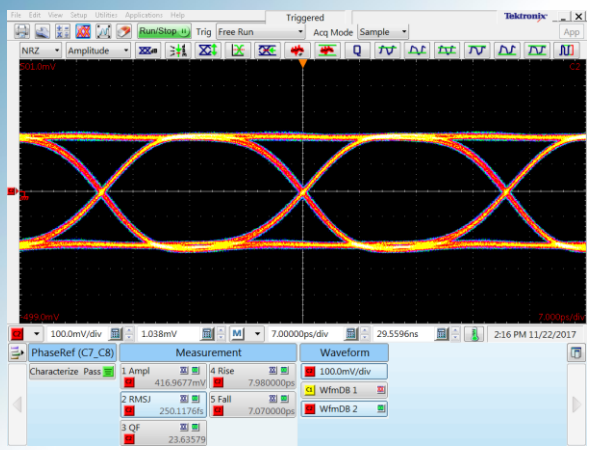
Out B @ 60 Gbps Output Bitrate



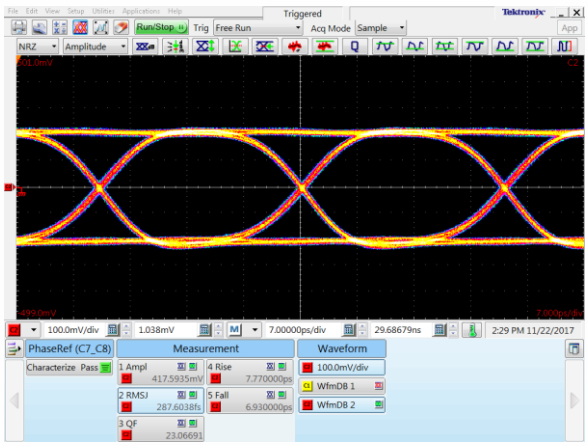
Out A @ 50 Gbps Output Bitrate



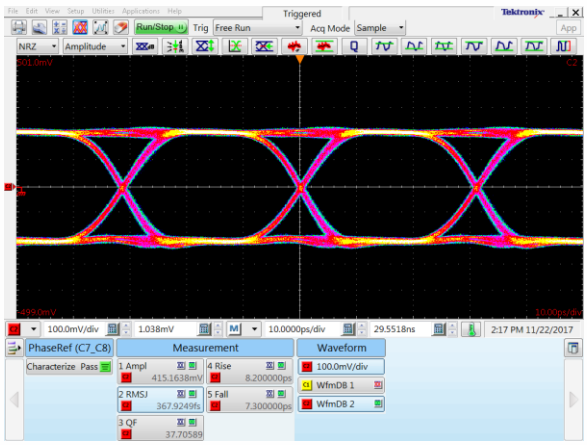
Out B @ 50 Gbps Output Bitrate



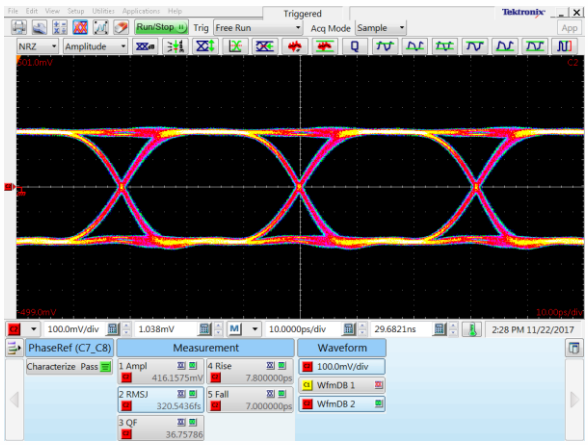
Out A @ 40 Gbps Output Bitrate



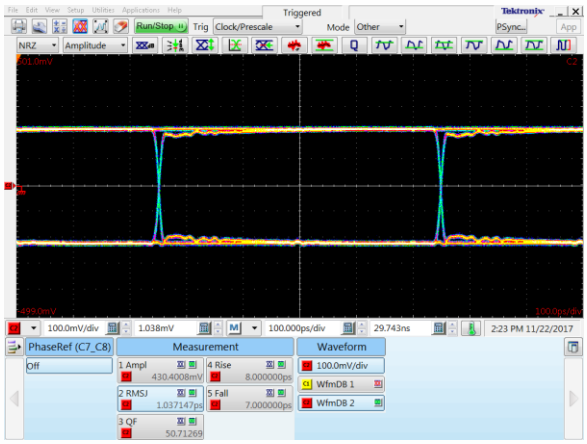
Out B @ 40 Gbps Output Bitrate



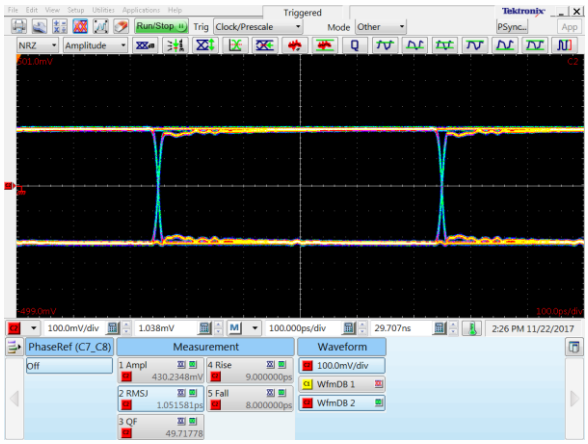
Out A @ 32 Gbps Output Bitrate



Out B @ 32 Gbps Output Bitrate



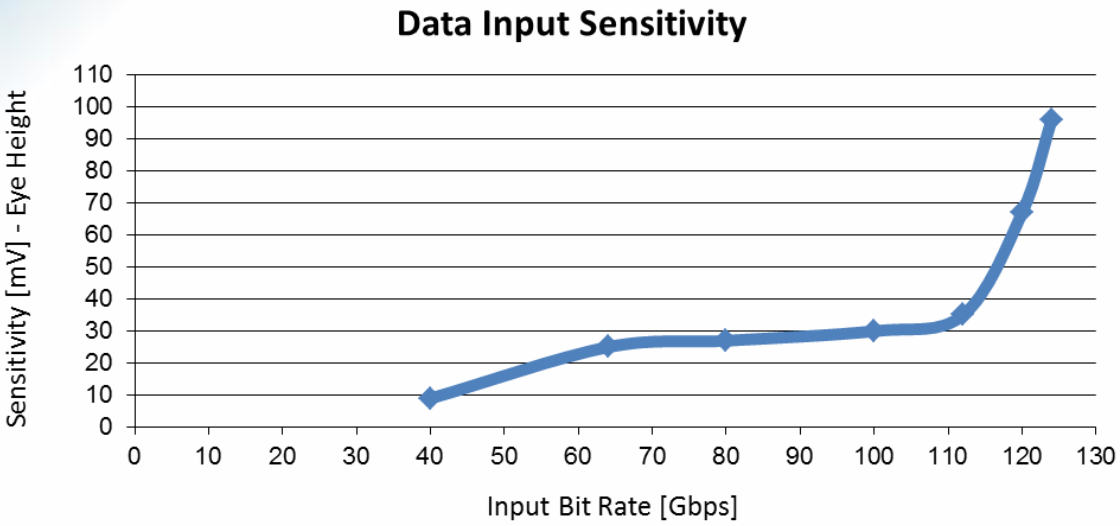
Out A @ 2 Gbps Output Bitrate

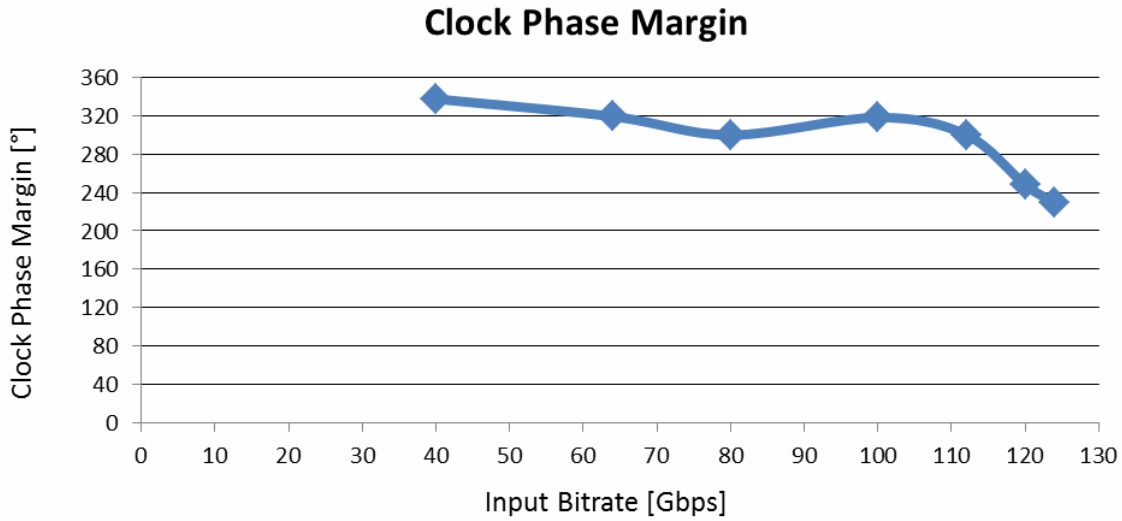


Out B @ 2 Gbps Output Bitrate

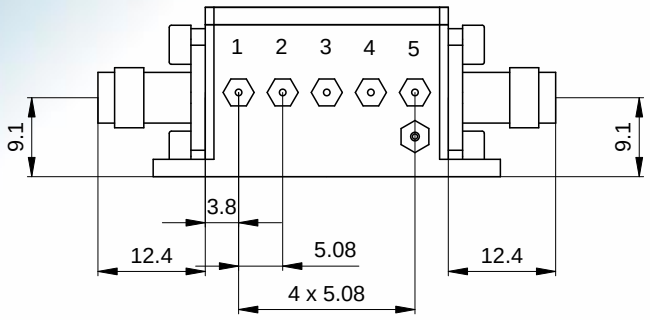
Typical Performance

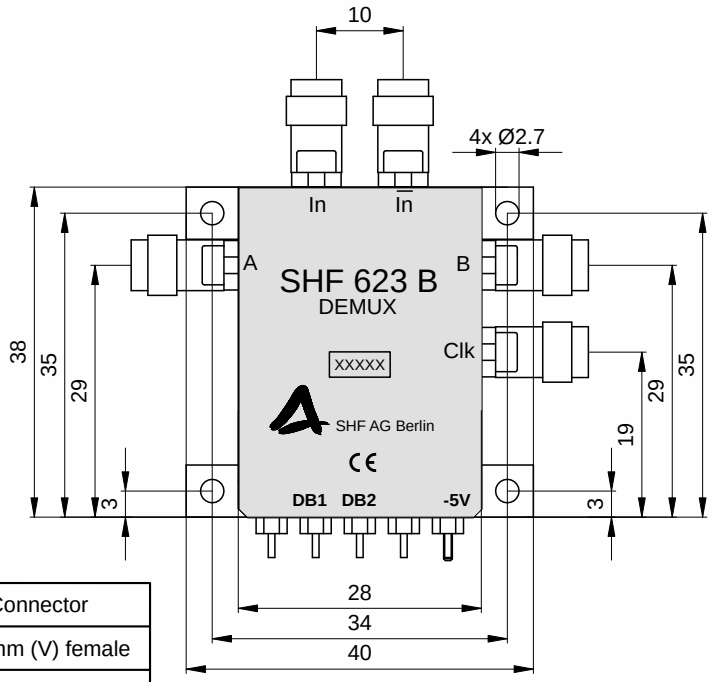
The measurements shown below had been performed using a SHF 603 A MUX (PRBS 2^{31}-1), a SHF 11104 A Error Analyzer, a Tektronix DSA8300 with Phase Reference Module (82A04B) and 70 GHz Sampling Head (80N01) to determine the eye height and jitter contribution of the input signal. In case of the sensitivity measurement the input signal had been reduced until a BER limit of $<10^{-9}$ was achieved. For the clock phase margin measurement, an input signal with an eye height of 100 mV has been applied and the phase of the clock signal was varied until the BER reached the 10^{-9} limit.

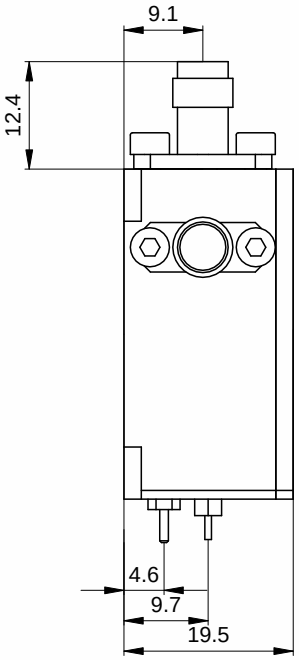




Outline Drawing – Module





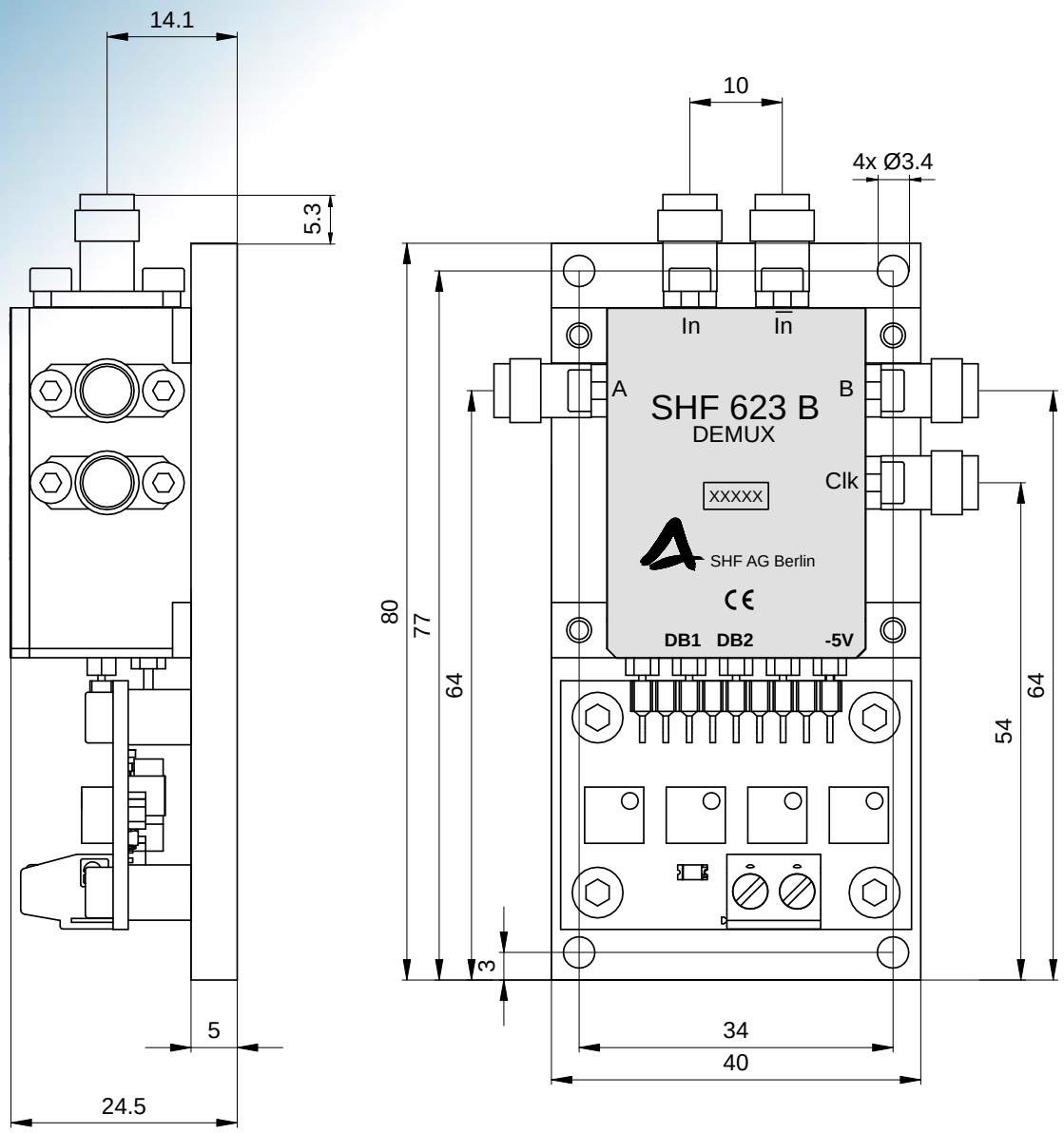


Port	Connector
In	1.85mm (V) female
$\overline{\text{In}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female

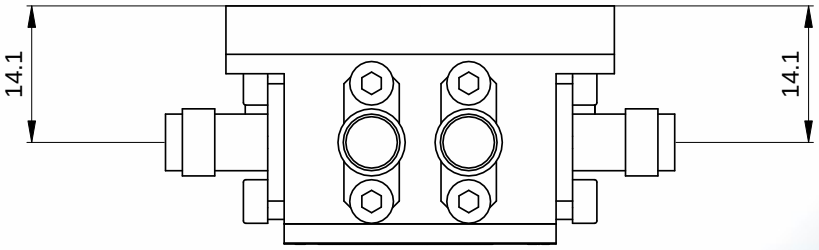
Pin	Designation
1	nc
2	DB1
3	DB2
4	nc
5	-5V

All dimensions in mm

Outline Drawing – “Module + Bias Board”- Assembly

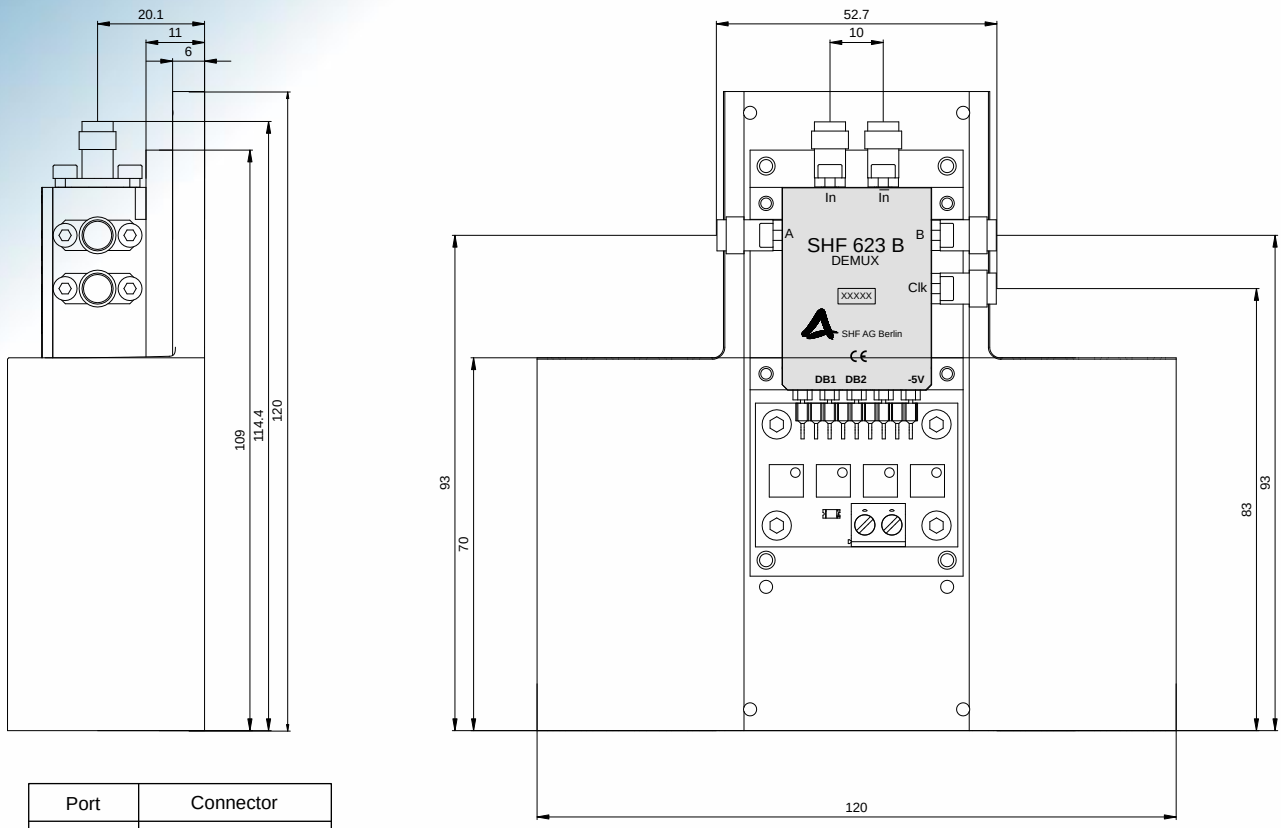


Port	Connector
In	1.85mm (V) female
$\overline{\text{In}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female



All dimensions in mm

Outline Drawing – “Module + Bias Board”- Assembly with Heat Sink



Port	Connector
In	1.85mm (V) female
$\overline{\text{In}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female

All dimensions in mm