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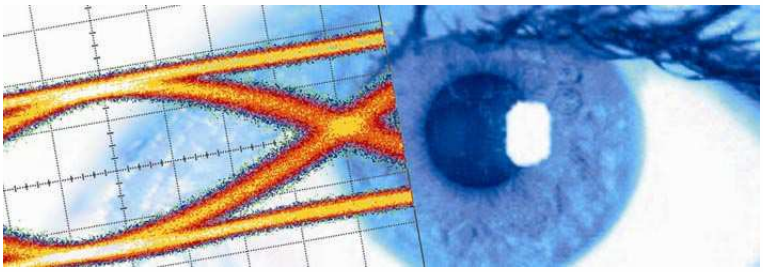
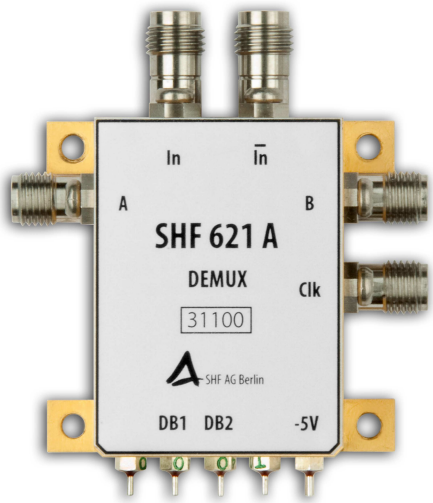


Datasheet

SHF 621 A

60 Gbps

1:2 Demultiplexer



Description

The SHF 621 A is a 1:2 demultiplexer operating at data rates up to 60 Gbps for use in broadband test setups and telecom transmission systems. A 60 Gbps single ended serial data stream is accepted by the demultiplexer and converted into two single ended data signals at a nominal output data rate of 30 Gbps. A single ended clock signal (nominally 30 GHz) with a frequency half of the input data rate drives the SHF 621 A. All in- and output ports are AC-coupled. Unused in- or output ports should be terminated.

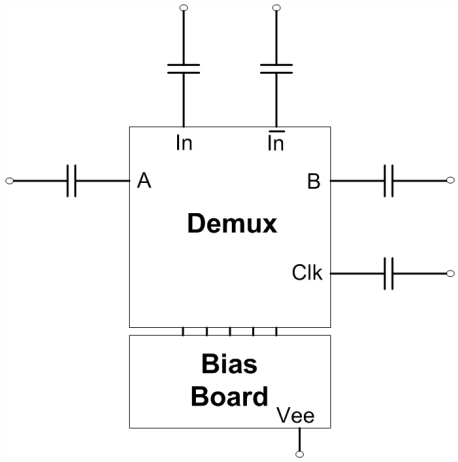
Features

- Broadband operation up to 60 Gbps
- Differential data inputs
- Data Input Sensitivity <50 mV
- Single ended clock input and data outputs
- Bias Board

Applications

- 100G Ethernet development and prototyping
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block Diagram



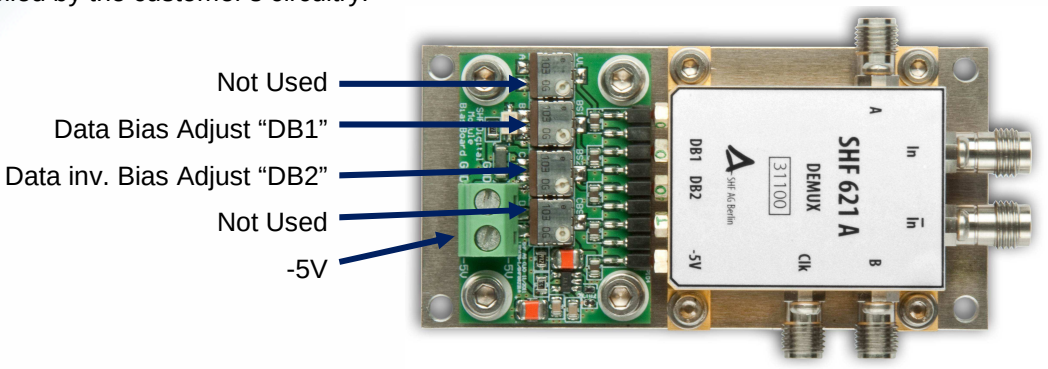
® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 621 A DEMUX. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust input data bias voltages “DB1” and “DB2” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



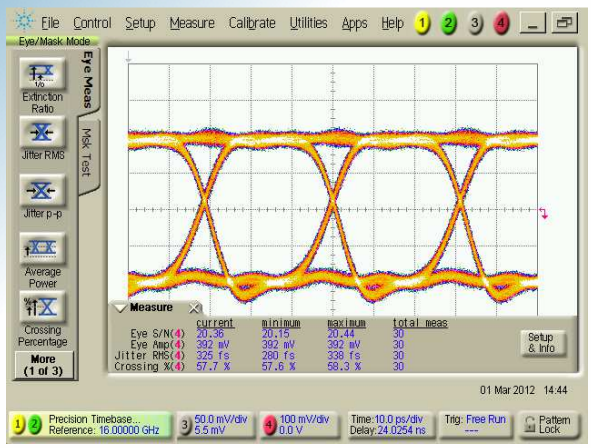
Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Minimum Input Data Rate	Gbps	$R_{in,min}$		1	2	@ 500mV$_{pp}$ clock input
Maximum Input Data Rate	Gbps	$R_{in,max}$	60	64		@ 500mV$_{pp}$ clock input
Data Input Voltage	mV$_{pp}$	$V_{data\ in}$			1000	
Data Input Sensitivity	mV	$V_{data\ in}$	50			Eye Height, see page 8
Clock Input Frequency	GHz	f_{in}	2		30	
Clock Input Voltage	mV$_{pp}$	$V_{clk\ in}$	300		1000	See page 8
Output Parameters						
Output Amplitude	mV	V_{out}	350	380		Single ended
Rise / Fall time	ps	t_r/t_f		8	10	20% / 80%
Output Jitter, RMS value[1]	fs	J_{rms}		400	500	
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		300	330	
Power Dissipation	mW	P_d		1500		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Input Data Bias	V	DB1	-3.3	-1,65	0	
Input inverted Data Bias	V	DB2	-3.3	-1,65	0	
Conditions						
Operating Temperature	℃	$T_{ambient}$	15		35	

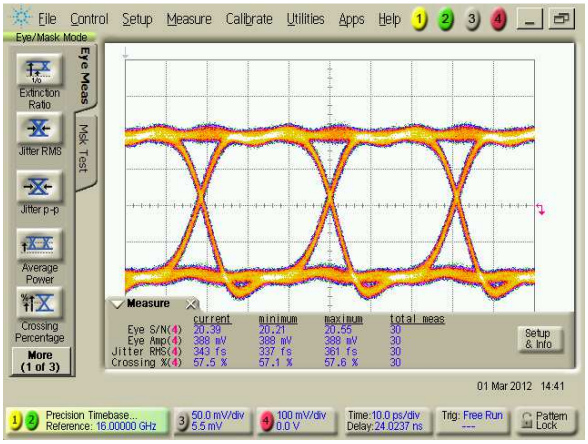
[1] Test condition: Input Signal Jitter$_{RMS}$ = 230 fs

Typical Output Eye Diagrams

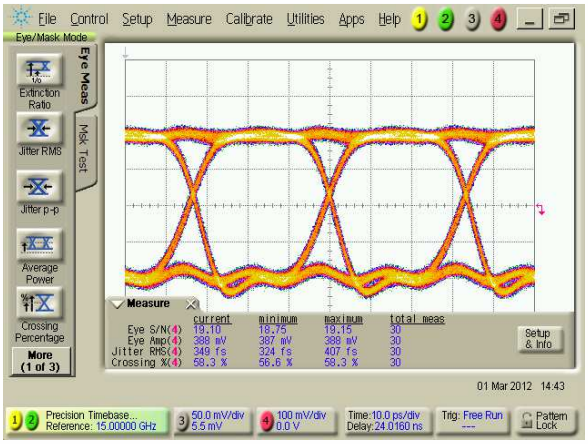
The measurements below had been performed using a SHF 12103 A BPG (PRBS 2^{31}-1) and an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the demultiplexer module had been connected directly to the DCA input.



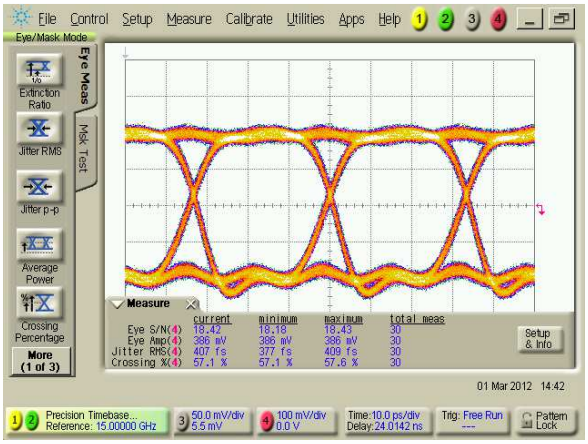
Out A @ 32 Gbps



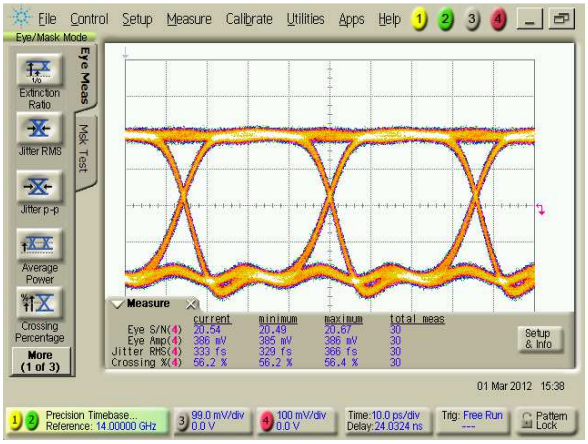
Out B @ 32 Gbps



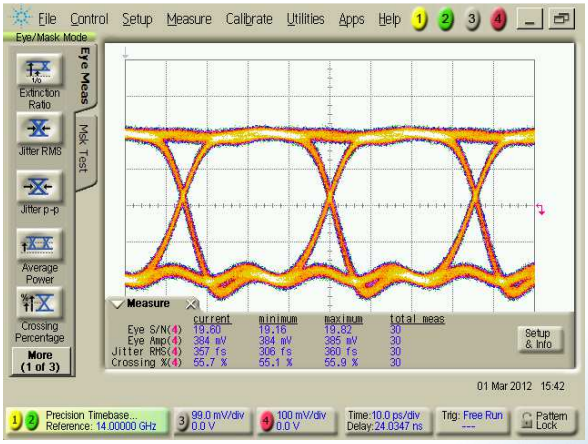
Out A @ 30 Gbps



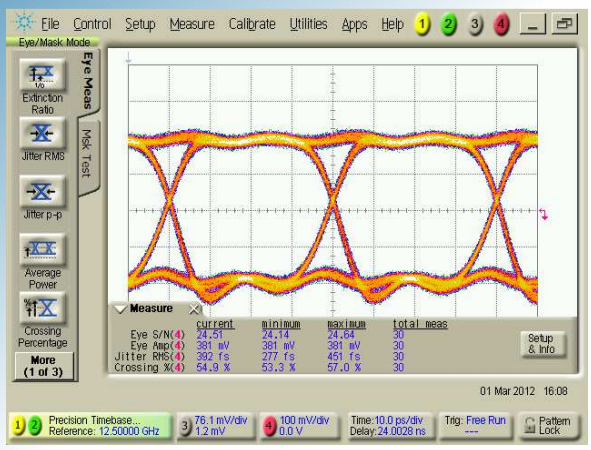
Out B @ 30 Gbps



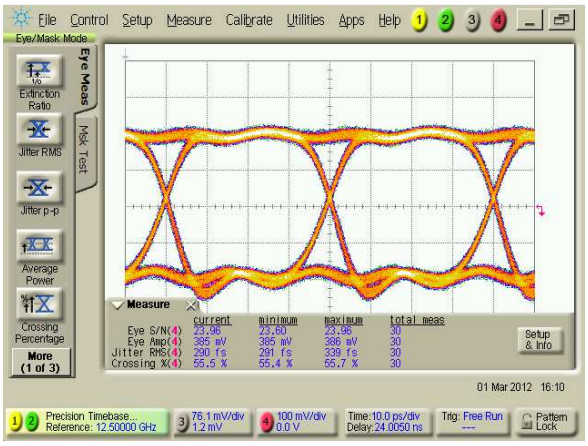
Out A @ 28 Gbps



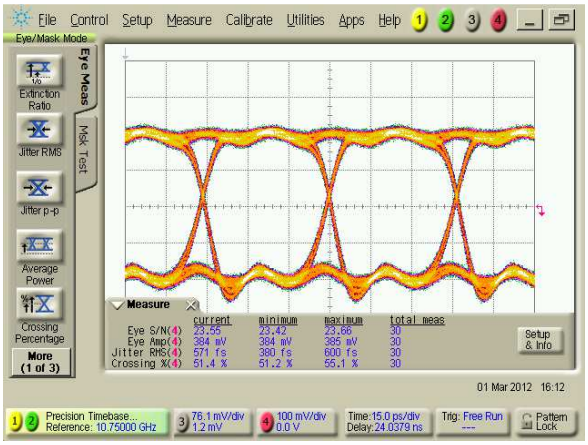
Out B @ 28 Gbps



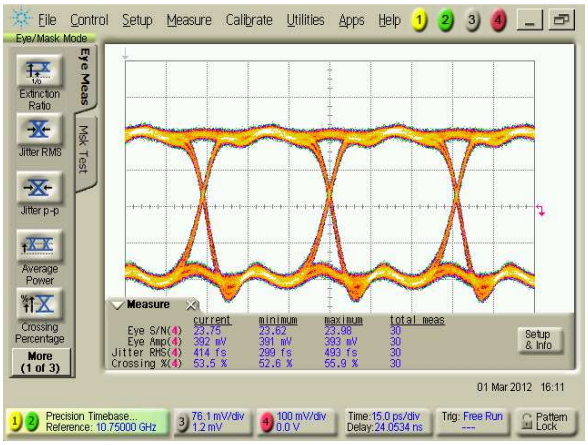
Out A @ 25 Gbps



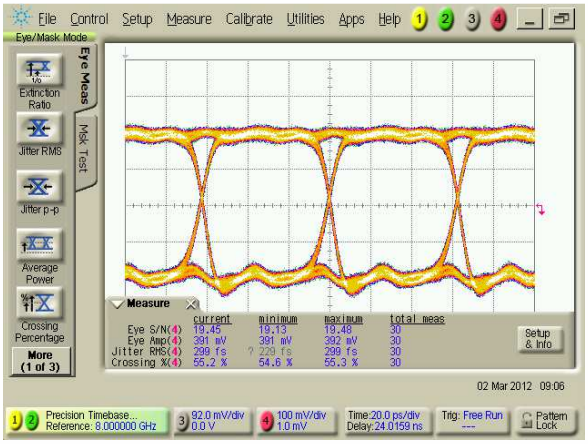
Out B @ 25 Gbps



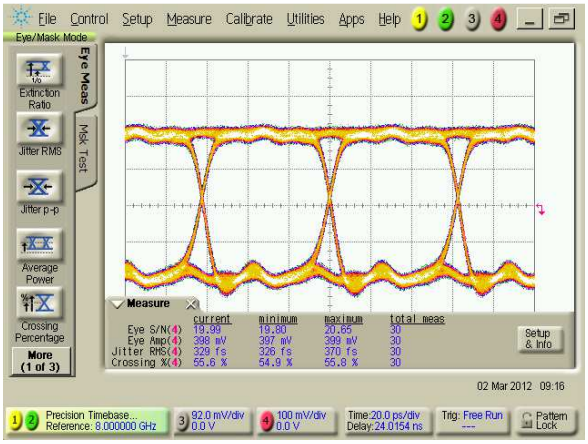
Out A @ 21,5 Gbps



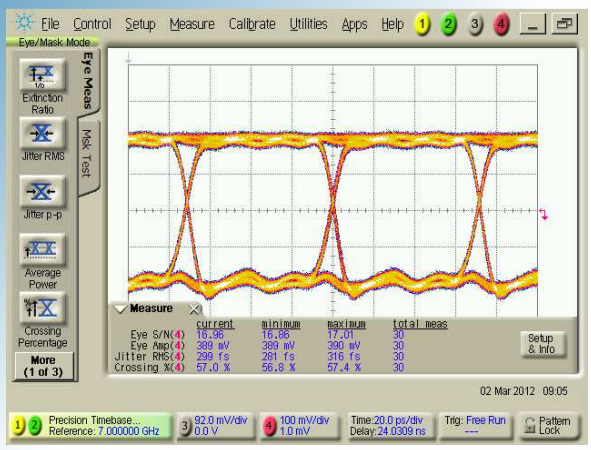
Out B @ 21,5 Gbps



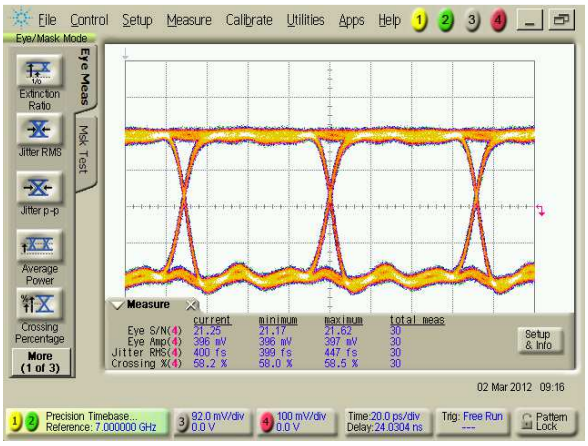
Out A @ 16 Gbps



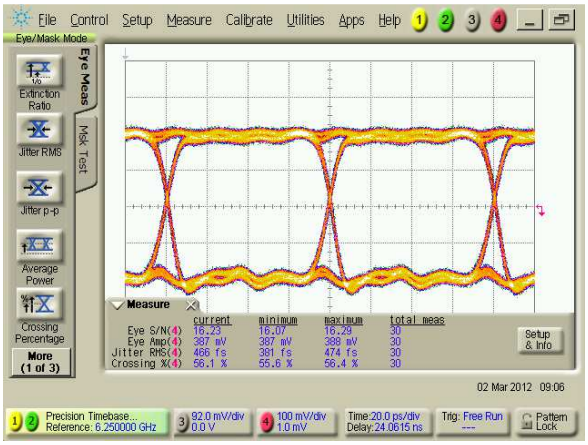
Out B @ 16 Gbps



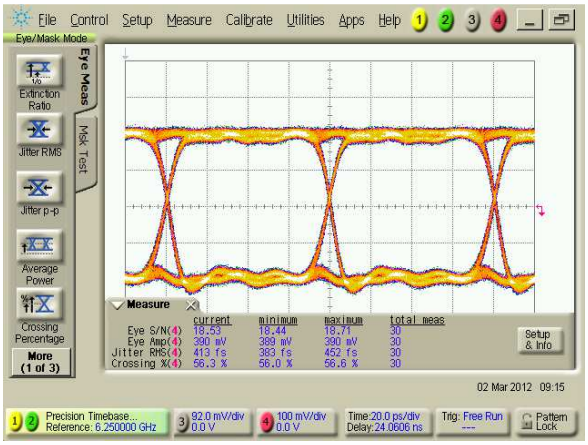
Out A @ 14 Gbps



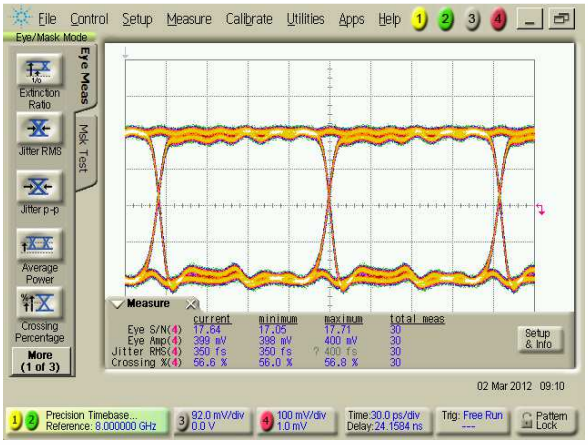
Out B @ 14 Gbps



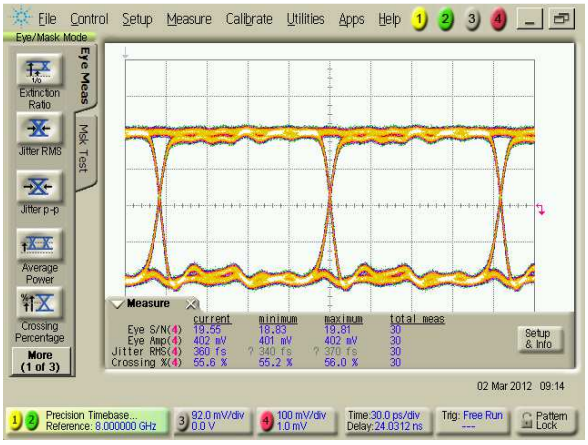
Out A @ 12,5 Gbps



Out B @ 12,5 Gbps



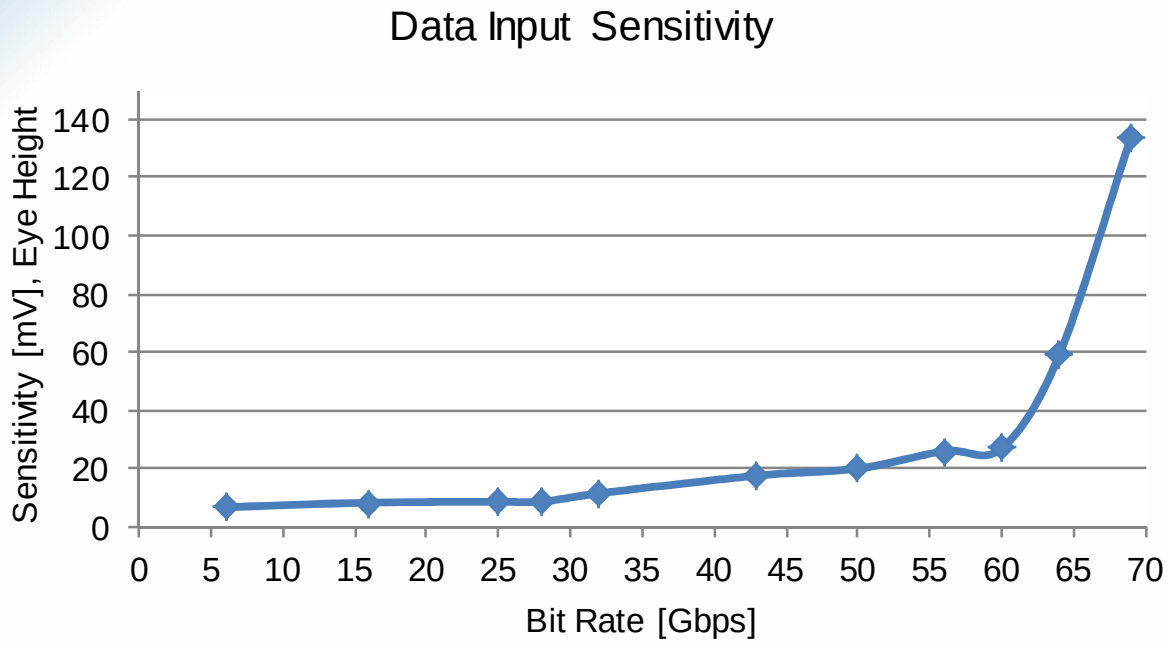
Out A @ 8 Gbps

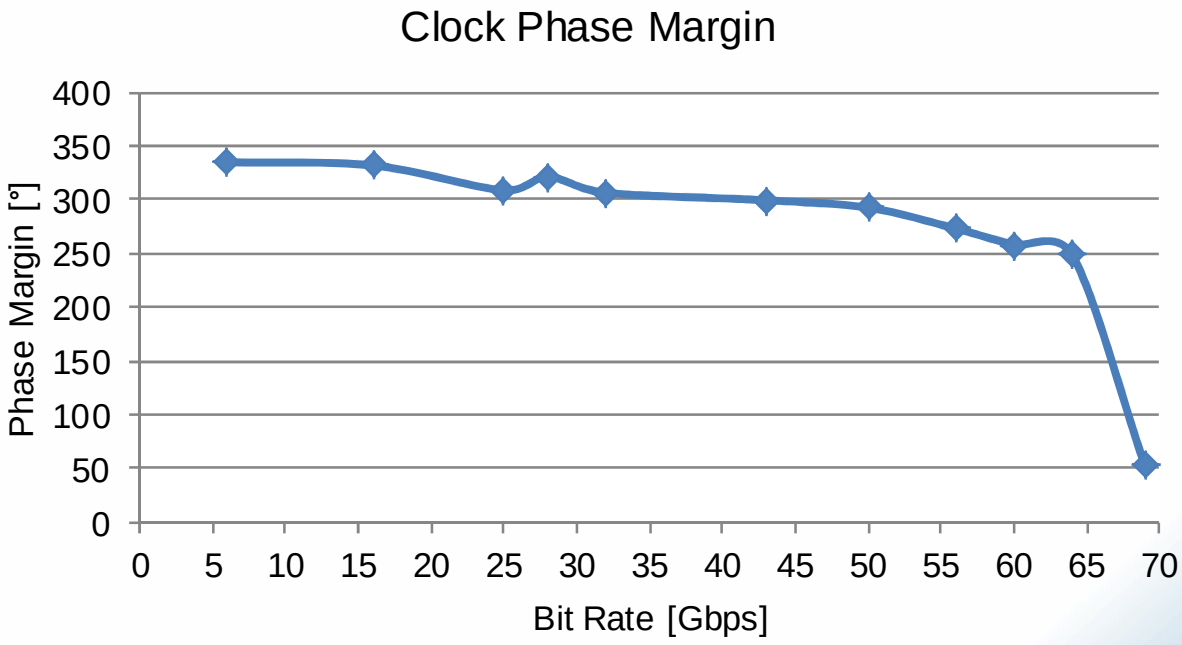


Out B @ 8 Gbps

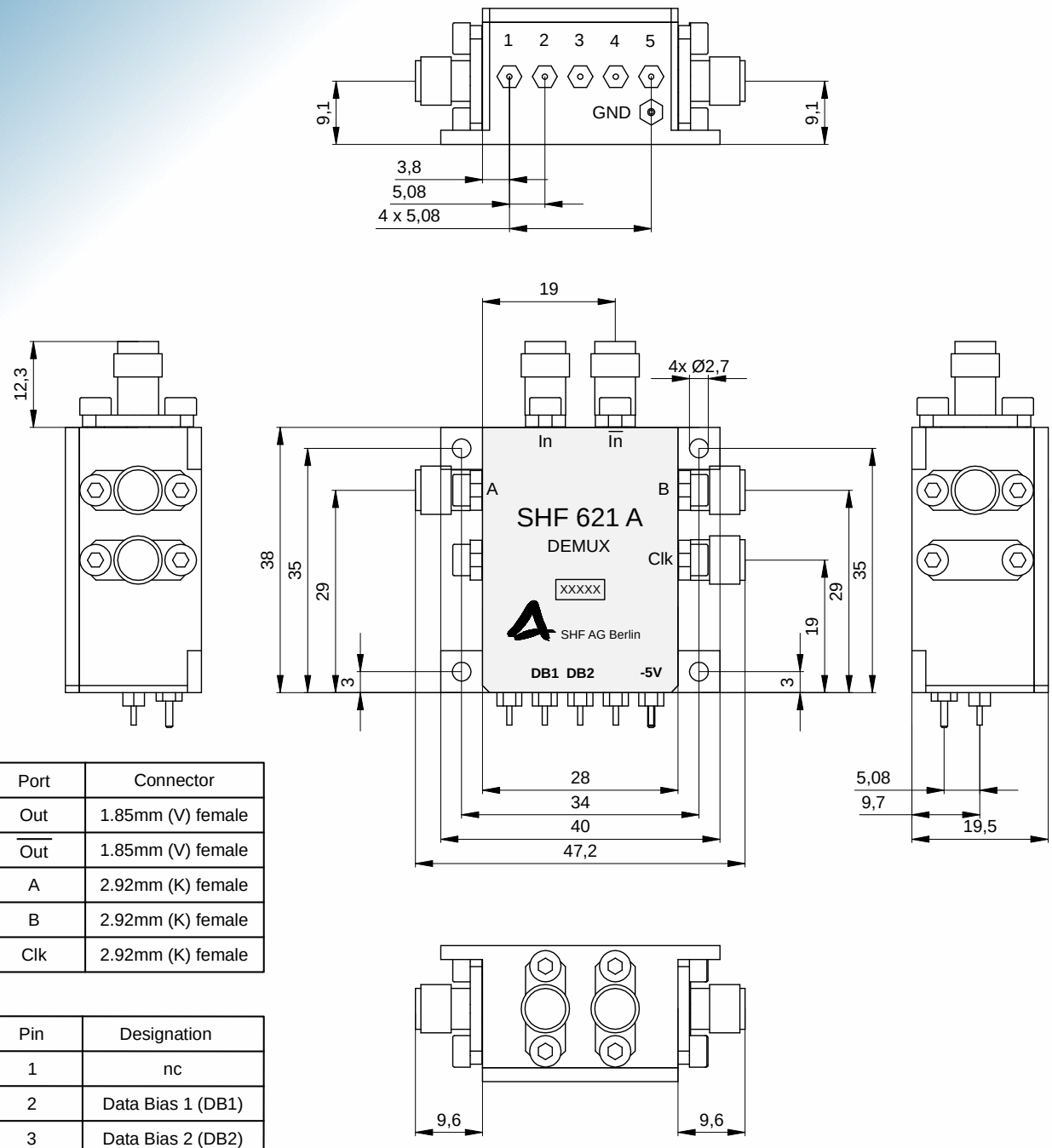
Typical Results

The measurements shown below had been performed using a SHF 601 A (PRBS 2^{31}-1, $V_{EyeHeight}$ = 100 mV), a SHF 11100 A Error Analyzer, an Agilent 86100D DCA with Precision Time Base Module (86107A) and a 70 GHz Sampling Head (86118A) to determine the eye height and jitter contribution of the input signal. In case of the sensitivity measurement the input signal had been reduced until a BER limit of $<10^{-9}$ was achieved. For the clock phase margin measurement the phase of the clock signal was varied until the BER reached the 10-9 limit.





Outline Drawing



Port	Connector
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
A	2.92mm (K) female
B	2.92mm (K) female
Clk	2.92mm (K) female

Pin	Designation
1	nc
2	Data Bias 1 (DB1)
3	Data Bias 2 (DB2)
4	nc
5	-5V