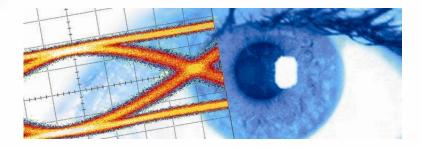


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# Datasheet SHF 616 B 128 GBaud PAM4 Multiplexer



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The SHF 616 B is a PAM4 Multiplexer operating at PAM4 baud rates up to 128 GBaud (256 Gbps) for use in broadband test setups and telecom transmission systems.

The SHF 616 B is driven by four single ended serial NRZ data streams. Each two of these signals are multiplexed to two binary data steam of double the speed. These two high speed signals are internally combined to one differential PAM4 signal. With a programmable SHF BPG (e.g. the SHF 12105 A) you have full control of the patterns into the PAM4-MUX. The SHF BCC Control Center software package unifies the BPG to PAM4-MUX combination to virtually one 128 GBaud PAM4-Bit Pattern Generator. A typical setup is shown in the figure 1 below.

A single ended clock signal with a frequency equivalent to the input data rate is required to drive the SHF 616 B. For data regeneration purposes all input data signals are re-sampled to mitigate any signal impairments resulting e.g. from long cables. Therefore, it is possible to place the PAM4-MUX very close to the DUT. Clock input port is AC-coupled. Data input and output ports are DC-coupled.

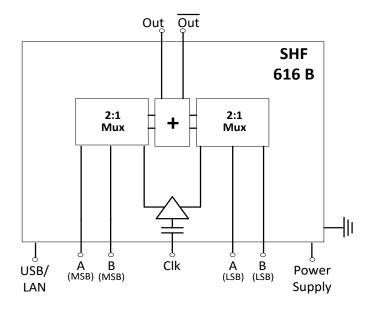
#### Features

- Broadband operation up to 128 GBaud
- Differential data output, 0.7 V differential output swing (0.35 V in single-ended operation)
- Single ended clock and data inputs
- Latched (re-timed and re-shaped) input ports
- Output amplitude & input threshold level control (remote by software)

### **Applications**

- 100 Gbps (100GbE), 200 Gbps (200GbE), 400 Gbps (400GbE) & 1 Tbps (TbE) system evaluation
- Broadband test and measurement equipment
- PAM4 and Advanced Modulation Experiments

#### **Block Diagram**



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Housed in a small benchtop case, this remote head can be easily embedded in the customer's test environment close to the DUT.



Figure 1 - Typical setup with SHF clock source, SHF BPG and the PAM4-MUX

The easy to use software package, SHF BCC Control Center is the most convenient way to control the MUX. The software reads the individual calibration tables of the multiplexers and sets the contribution of the bias voltages accordingly. The symmetry of the output signal can be set and is displayed in the graphical user interface (GUI). The duty cycle (clock bias) of the multiplexer stages as well as the input threshold level for the DC-coupled data inputs can be set. This enables the user to generate a perfect signal just by a few intuitive clicks.

	616 @ 0	
SHF 616 B PAM4 Multiplexer	Center ready Network	Off
Output   Output   On Off   Amplitude Symmetry   355 mV   44 >>>		
Version: 1.0 Serial: 49851 Option: 0 Server: 0.10.12 Kerne	el: 0.7.5 CPU: 40000000 Hz	Factory preset

BCC Control Center - SHF 616 B

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## **Absolute Maximum Ratings**

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	V <sub>data in</sub>			900	Peak-to-Peak
Clock Input Voltage	mV	V <sub>clk in</sub>			900	Peak-to-Peak
External DC Voltage on RF Clock Input Port	V	V <sub>DCin</sub>	-10		+10	AC coupled input
External DC Voltage on RF Data Input Ports	V	V <sub>DCin</sub>	-0.6		+0.1	DC coupled inputs
DC Supply Voltage	V	V <sub>cc</sub>			13.0	

## **Specifications**

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Min. Input Data Rate	Gbps	R <sub>in,min</sub>			1	
Max. Input Data Rate	Gbps	R <sub>in,max</sub>	64 <sup>1</sup>			
Data Input Voltage	mV	V <sub>data in</sub>	300		800	Eye amplitude; 500 mV recommended
External DC Voltage on RF Data Input Ports	V	V <sub>DCin</sub>	-0.5		0	DC coupled inputs
Min. Clock Input Frequency	GHz	f <sub>in,min</sub>			1	
Max. Clock Input Frequency	GHz	f <sub>in,max</sub>	64			
Clock Input Voltage	mV	$V_{\text{clk in}}$	300		800	Peak-to-Peak; 500 mV recommended
External DC Voltage on RF Clock Input Port	V	V <sub>DCin</sub>	-9		+9	AC coupled input

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<sup>&</sup>lt;sup>1</sup> The upper baud rate limit is defined by the absence of errors (BER <  $10^{-12}$ ) of a NRZ output generated with the MSB + LSB bit synchronized. The PAM4-MUX operates beyond this limit as shown in the typical eye diagrams below. However, it is just not currently possible to verify a true BER beyond this limit.



Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment	
Output Parameters							
Min. Output Data Rate	GBaud	R <sub>out,min</sub>			2		
Max. Output Data Rate	GBaud	R <sub>out,max</sub>	128 <sup>2</sup>				
Output Voltage <sup>3</sup>	mV	V <sub>out</sub>	300 270	350 320		≤ 100 GBaud > 100 GBaud Eye amplitude; Single ended; DC coupled; Full scale; Adjustable up to -6 dB	
Rise / Fall Time	ps	t <sub>r</sub> / t <sub>f</sub>		5	6	20%80%; Full scale; deconvolved <sup>4</sup>	
Equivalent Output Bandwidth	GHz	BW	37	44		Derived from Rise Time using formula <sup>5</sup> ; -3 dB bandwidth	
Differential Output Skew	ps	t <sub>skew</sub>		1	2		
General	_	_					
Supply Voltage	V	Vc	+11.5	+12	+12.5	2.1 mm DC Power Jack	
Supply Current	mA	Ι <sub>c</sub>		1000	1100		
Power Dissipation	W	Pd		12	13.2	@ V <sub>C</sub> = +12V	
Operating Temperature	°C	Tambient	10		35		
Height	mm	Н		50.8			
Width	mm	W		221.4			
Depth	mm	D		177			
Weight	g	m		1700			

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<sup>&</sup>lt;sup>2</sup> The upper baud rate limit is defined by the absence of errors (<  $10^{-12}$ ) of a NRZ output generated with the MSB + LSB bit synchronized. The PAM4-MUX operates beyond this limit as shown in the typical eye diagrams below. However, it is just not currently possible to verify a true BER beyond this limit.

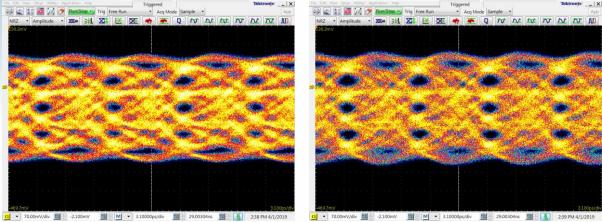
<sup>&</sup>lt;sup>3</sup> During start up / shut down of the SHF 616 B and turning on / off the RF outputs, voltage spikes up to +0.7 V can occur at the data output ports

<sup>&</sup>lt;sup>4</sup> Calculation based on typical rise / fall times from oscilloscope data sheet and with a NRZ output generated by bit synchronization of the MSB + LSB  $t_{r \ deconvolved} = \sqrt{(t_{r \ measured})^2 - (t_{r \ oscilloscope})^2} = \sqrt{(t_{r \ meas})^2 - (3.68 \ ps)^2}$ 

<sup>&</sup>lt;sup>5</sup> Calculation based on formula:  $BW = \frac{0.22}{Tr}$ 



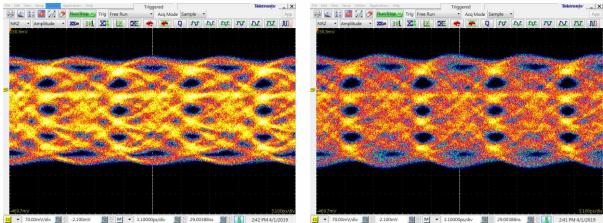
The measurements below had been performed using a SHF 12105 A Bit Pattern Generator (PRBS 2<sup>31</sup>-1) and a Tektronix DSA 8300 Digital Serial Analyzer (DSA) with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Module (80E11). The outputs of the PAM4 MUX module had been connected directly to the DSA input.



#### **PAM4 Output Signal Measurement**

Out @ 130 GBaud

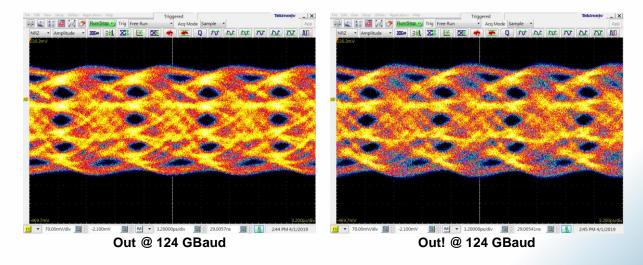
Out! @ 130 GBaud



Out @ 128 GBaud

📓 🕂 M 🔹 3.10000ps/div 📓 🗄 29.00388ns 📓 🕆 🚺 2:41 PM 4

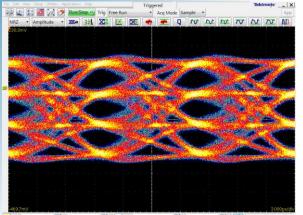
Out! @ 128 GBaud

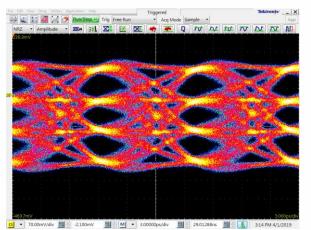


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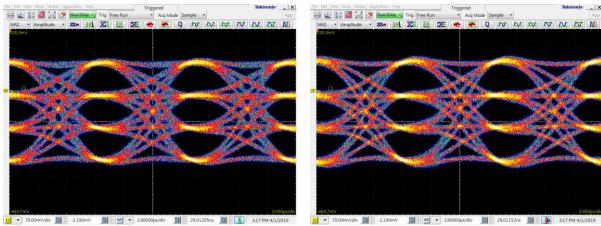




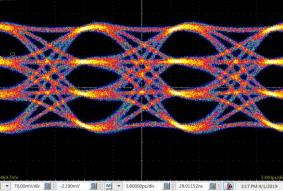
■ • M • 3.0 29.01288ns Out @ 100 GBaud

Out! @ 100 GBaud

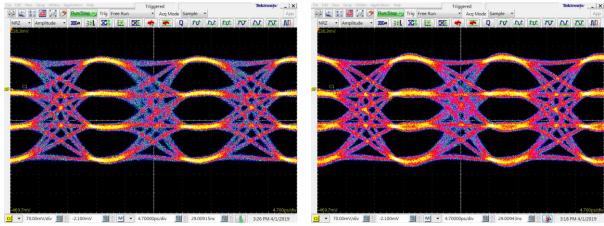
Tektronix \_\_\_\_X



Out @ 80 GBaud



Out! @ 80 GBaud



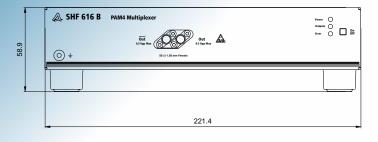
Out @ 64 GBaud

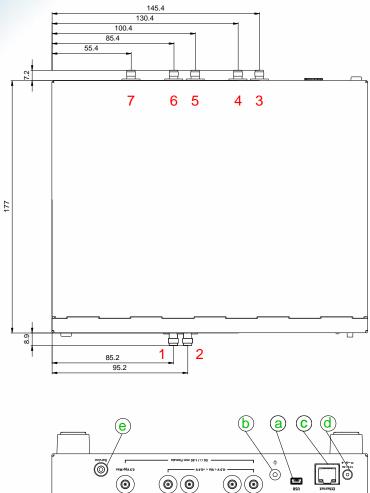
Out! @ 64 GBaud

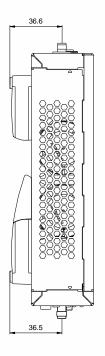
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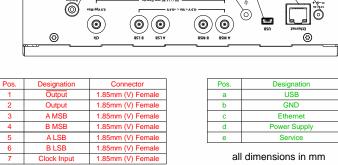












mm (V) Female	d	Power Supply
mm (V) Female	е	Service
mm (V) Female		
mm (V) Female	all	dimensions in mm

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A LSB B LSB

Clock Inc

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