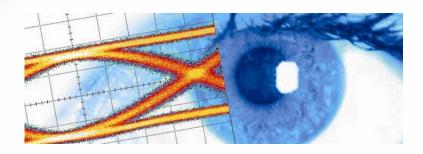


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# Datasheet SHF 614 C 60 GBaud 6-Bit DAC







# **Description**

The SHF 614 C is a 6-Bit Digital-to-Analog Converter (DAC) operating at symbol rates up to 60 GBaud for use in broadband test setups and telecom transmission systems. Up to six single ended serial data streams are accepted by the DAC and converted into one differential 64-level data signal. By using less than six input ports it is possible to generate 2-level NRZ as well as 4, 8, 16 or 32-level output signals.

With a programmable SHF BPG (e.g. SHF 12104 A or SHF 12105 A) one has full control of the patterns into the DAC. Therefore our BPG/DAC combination can be seen as a full blown remote head non-interleaved 60 GBaud Arbitrary Waveform Generator (AWG).

A single ended clock signal with the same frequency as the data rate is required to drive the SHF 614 C. For data regeneration purposes all input data signals are re-sampled to mitigate any signal impairments resulting e.g. from long cables. Therefore, it becomes possible to place the DAC very close to the DUT. Clock input port and data output ports are AC-coupled. Data input ports are DC-coupled.

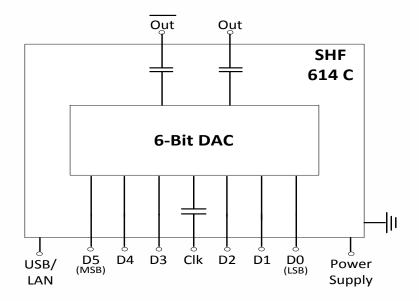
### **Features**

- Broadband operation up to 60 GBaud
- Output baud rate = sample rate
- Differential data output, 3.0 V differential output swing (1.5 V in single-ended operation)
- Single ended clock and data inputs
- Latched input ports
- Output amplitude & input threshold level control (remote by software)

# **Applications**

- 100, 200, 400 Gbps and 1 Tbps system evaluation & development
- Broadband test and measurement equipment
- PAM-N, OFDM, Advanced Modulation Experiments

# **Block Diagram**







# **Ease of Use**

The SHF 614 C DAC module, the power supply and cooling measures are housed in a small benchtop case which can be embedded easily in the customer's test environment. It is to be connected to a computer either by Ethernet or USB.



Fig. 2: SHF 614 C

The DAC is controlled by the easy to use SHF Control Center (SCC) software package. The software reads the individual calibration tables of the DAC and sets the contribution of the bias voltages accordingly. The amplitude of the individual eye openings as well as the input threshold level for the DC-coupled data inputs can be set and is displayed in the graphical user interface (GUI). This enables the user to generate a perfect signal with a few intuitive clicks.

This SCC software interface does further support the user in case the SHF 614 C DAC is connected to another SHF instrument. For example, if the DAC is connected to a SHF 12105 A Bit Pattern Generator (BPG) the software unifies the two discrete instruments to one single Arbitrary Waveform Generator (AWG). The user can program any signal trace desired at the DACs output; the SCC automatically translates the desired output waveform to the six individual binary patterns which are stored in the BPGs user pattern memory and sent to the DACs inputs.

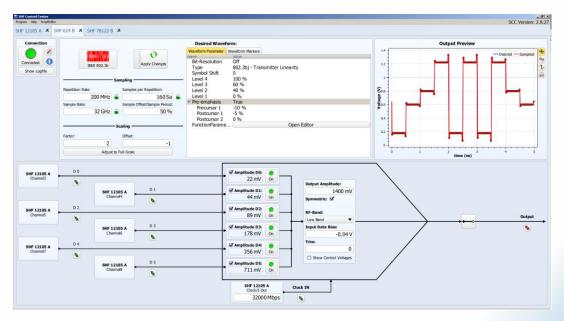


Fig. 3: Connection diagram of BPG to DAC of the SCC





bsolute Maximum	Rating	gs				
Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	V <sub>data in</sub>			900	Peak-to-Peak
Clock Input Voltage	mV	V <sub>clk in</sub>			900	Peak-to-Peak
External DC Voltage on RF Clock Input Port	V	$V_{DCin}$	-10		+10	AC coupled input
External DC Voltage on RF Data Input Ports	V	$V_{DCin}$	-0.5		0	DC coupled inputs
External DC Voltage on RF Output Ports	V	$V_{DCout}$	-10		+10	AC coupled outputs
DC Supply Voltage	V	V <sub>cc</sub>			13.0	

# **Specifications**

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Min. Input Data Rate	Gbps	$R_{\text{in,min}}$			1	
Max. Input Data Rate	Gbps	R <sub>in,max</sub>	60			
Data Input Voltage	mV	V <sub>data in</sub>	300		800	Eye Amplitude; 500 mV recommended
External DC Voltage on RF Data Input Ports	V	$V_{DCin}$	-0.5		0	DC coupled inputs
Min. Clock Input Frequency	GHz	f <sub>in,min</sub>			1	
Max. Clock Input Frequency	GHz	f <sub>in,max</sub>	60			
Clock Input Voltage	mV	V <sub>clk in</sub>	300		800	Peak-to-Peak; 500 mV recommended
External DC Voltage on RF Clock Input Port	V	$V_{DCin}$	-10		+10	AC coupled input



Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Output Parameters						
Min. Output Data Rate	GBaud	R <sub>out,min</sub>			1	
Max. Output Data Rate	GBaud	$R_{\text{out,max}}$	60			
Output Voltage	mV	$V_{out}$	1300	1512		Eye Amplitude; Single ended; Full scale; Adjustable up to -6 dB → see page 7
Rise / Fall Time	ps	t <sub>r</sub> / t <sub>f</sub>		8.2	10	20%80%; deconvolved <sup>1</sup>
Equivalent Output Bandwidth	GHz	BW	22	27		Derived from Rise Time using formula <sup>2</sup> ; -3 dB bandwidth
Differential Output Skew	ps	t <sub>skew</sub>		±1	±2	
Power Requirements						
Supply Voltage	V	Vc	+11.5	+12	+12.5	2.1 mm DC Power Jack
Supply Current	mA	Ic		1350	1450	
Power Dissipation	W	$P_d$		16.2	17.4	@ V <sub>C</sub> = +12V
Conditions						

 $\mathsf{T}_{\mathsf{case}}$ 

10

1 Calculation based on typical rise / fall times from oscilloscope data sheet:  $t_{r\,deconvolved} = \sqrt{(t_{r\,measured})^2 - (t_{r\,oscilloscope})^2} = \sqrt{(t_{r\,meas})^2 - (3.68\,ps)^2}$ 

Module Temperature<sup>3</sup>

 $<sup>\</sup>frac{3}{t_r}/t_r$  of the output data signal can be slightly decreased by applying additional cooling measures like heat sinks or cooling fans.



<sup>&</sup>lt;sup>2</sup> Calculation based on formula:  $BW = \frac{0,22}{Tr}$ 



# **Typical Output Amplitudes**

Below mentioned values assume no attenuation to be set in the control software. The output amplitude of the DAC can be reduced by 0 to 6 dB by making the appropriate setting in the control software.

Input D5	Input D4	Input D3	Input D2	Input D1	Input D0	Typical Output Amplitude [mV]
-	-	-	-	-	On	24
-	-	-	-	On	-	48
-	-	-	On	-	-	96
-	-	On	-	-	-	192
-	On	-	-	-	-	384
On	-	-	-	-	-	768

The typical output amplitude of a multilevel signal can be calculated by accumulating the typical output amplitudes of all applied input ports of the DAC as shown in the table above. Thus the full scale output swing (all inputs active) accumulates as follows:

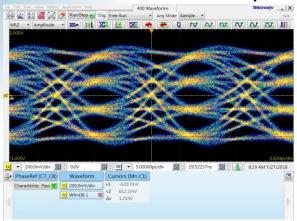
On On On On On 1512
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# **Typical Output Eye Diagrams**

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2<sup>31</sup>-1) and a Tektronix DSA 8300 Digital Serial Analyzer (DSA) with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Module (80E11). The outputs of the DAC module had been connected directly to the DSA input with a 10 dB attenuator.

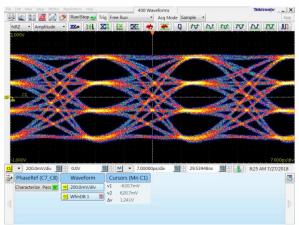
### **4-Level Output Signal Measurement**

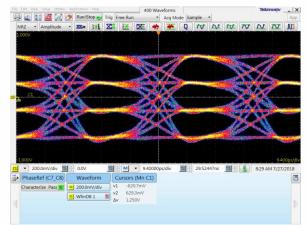


| RandStope | Trig free Run | Aque Mode | Sample | App | Aque | A

Out @ 60 GBaud

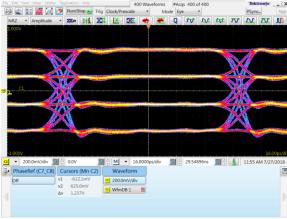
Out @ 56 GBaud





Out @ 43 GBaud

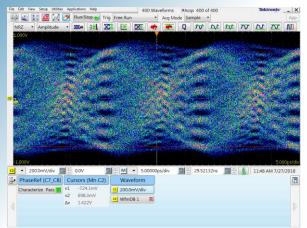
Out @ 32 GBaud



Out @ 10 GBaud



# **8-Level Output Signal Measurement**

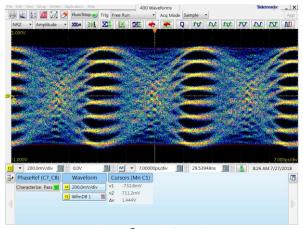


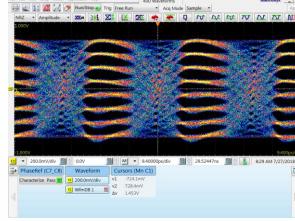
400 Waveforms #Acqs 400 of 400

Takeronys | Acqs 400 of 400 | Acqs 400 | Acqs 400 of 400 | Acqs 400 |

Out @ 60 GBaud

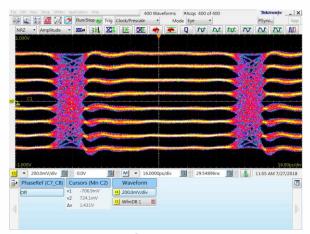
Out @ 56 GBaud





Out @ 43 GBaud

Out @ 32 GBaud

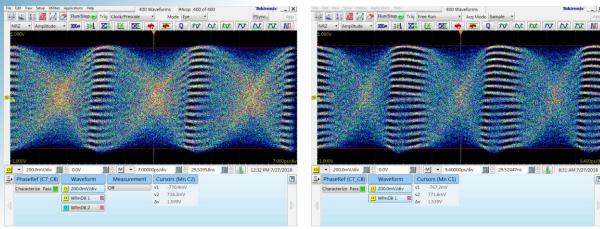


Out @ 10 GBaud



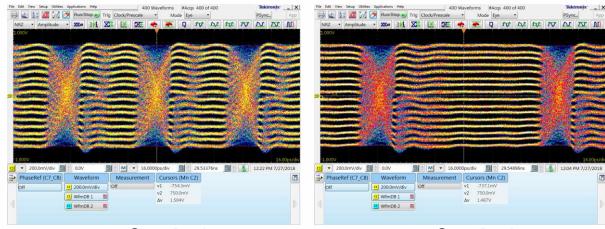


### **16-Level Output Signal Measurement**



Out @ 43 GBaud

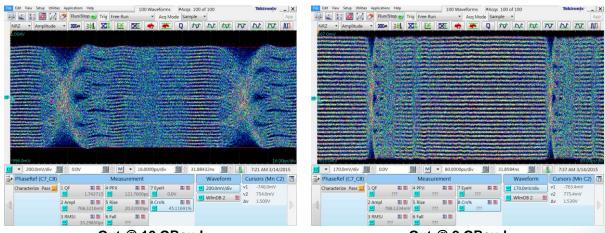
Out @ 32 GBaud



Out @ 20 GBaud

Out @ 10 GBaud

### **32-Level Output Signal Measurement**



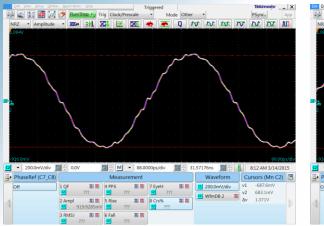
Out @ 10 GBaud

Out @ 2 GBaud





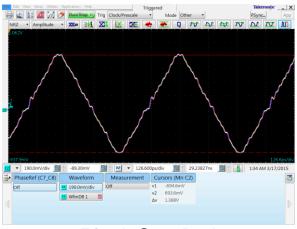
# **Arbitrary Waveform Generation (4-Bit Mode)**



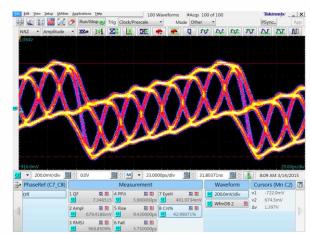
Triggered Warming Warming Cook/Pressale - Mode Other - Mo

Sine @ 60 GBaud

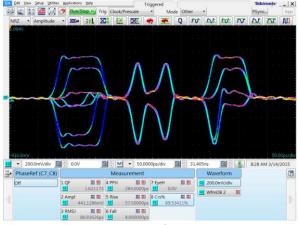
Saw @ 60 GBaud







Stepped Eye @ 60 GBaud

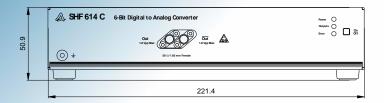


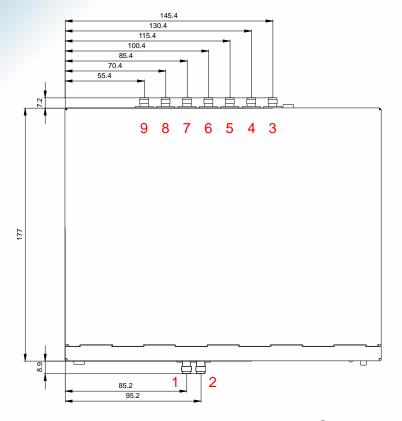
"SHF"- writing @ 60 GBaud

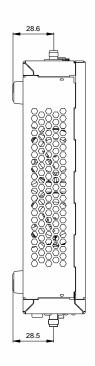


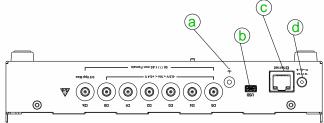


# Outline Drawing - SHF 614 C









Pos.	Designation			
а	GND			
b	Mini USB			
С	Ethernet RJ45			
d	Power Supply			

all dimensions in mm

Pos.	Designation	Connector
1	DAC Ouput	1.85mm (V) Female
2	DAC Ouput	1.85mm (V) Female
3	D5 Input	1.85mm (V) Female
4	D4 Input	1.85mm (V) Female
5	D3 Input	1.85mm (V) Female
6	D2 Ouput	1.85mm (V) Female
7	D1 Input	1.85mm (V) Female
8	D0 Input	1.85mm (V) Female
9	Clock Input	1.85mm (V) Female