

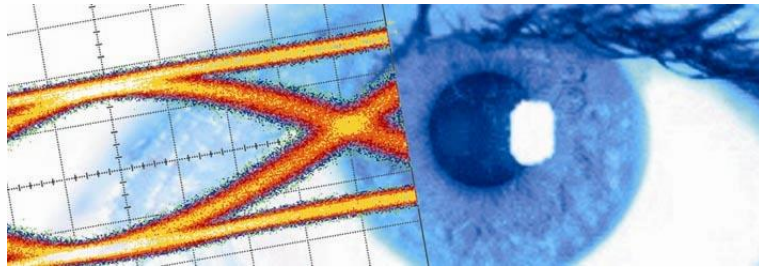


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# Datasheet

## SHF 613 A

### 60 GBaud 3-Bit DAC





## Description

The SHF 613 A is a 3-Bit Digital-to-Analog Converter (DAC) operating at symbol rates up to 60 GBaud for use in broadband test setups and telecom transmission systems. Three single ended serial data streams of up to 60 Gbps are accepted by the DAC and converted into one differential 8-level data signal of up to 60 GBaud. By using two input ports only it is possible to generate 4-level output signals. A single ended clock signal with the same frequency as the data rate drives the SHF 613 A. Thus the baud rate of the resulting PAM signal is as fast as the sample rate of the system.

For data regeneration purposes all input data signals are re-sampled to mitigate any signal impairments resulting e.g. from long cables. Therefore, it becomes possible to place the DAC very close to the DUT. All RF input and output ports are AC-coupled.

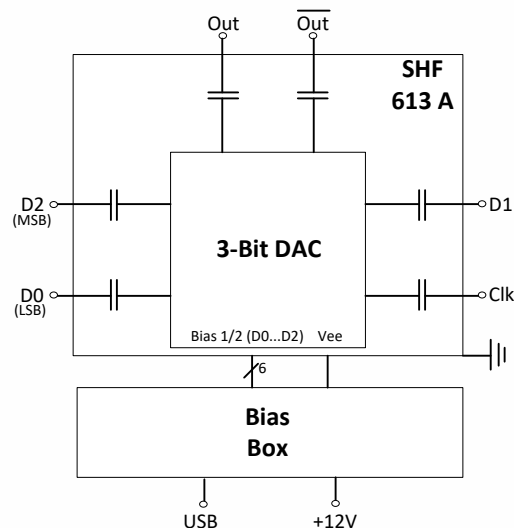
## Features

- Broadband operation up to 60 GBaud
- Output baud rate = sample rate
- Differential data output, 600 mV single ended output swing
- Single ended clock and data inputs
- Latched input ports
- Output level control
- Bias Box

## Applications

- 100G, 200G and 400G system evaluation & development
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel<sup>®</sup>
- Broadband test and measurement equipment

## Block Diagram



<sup>®</sup> Fibre Channel is a registered trademark of the Fibre Channel Industry Association

SHF reserves the right to change specifications and design without notice - SHF 613 A - V004 – October 31, 2019 Page 2/18



## Module Description

At delivery, the Bias Box SHF 88120 B is mounted on a common base plate, together with the SHF 613 A 3-Bit DAC (Fig.1). All bias voltages are provided by this Bias Box which is controlled by a PC via a USB interface. The easy to use software package is a complementary part of each delivery. For system applications it is possible to remove the Bias Box. In that case the operating voltages have to be supplied by the customer's circuitry. It is recommended to use the Bias Box only with the delivered power supply. Using other power supplies can damage the Bias Box.

The provided heat sink can be disassembled by the customer. In this case it is required to provide other cooling measures to ensure that the maximum case temperature specified on page 6 will not be exceeded.



Fig. 1: "SHF 613 A + Bias Box"-Assembly

## Option Case

With Option Case (Fig.2) the SHF 613 A DAC module, the power supplies, cooling measures and the Mini-SMP to 1.85 mm panel adaptors are housed in a small benchtop case that can be easily embedded in the customer's test environment.

With "Option Case Dual Channel" one common clock signal has to be applied externally and drives both DACs.



Fig. 2: SHF 613 A – incl. Opt. Case

### Configurations for Option Case

- Single Channel: One DAC module, power supplies, cooling measures and 1.85 mm panel adaptors are housed in a small benchtop case.
- Dual Channel: Two DAC modules, power supplies, cooling measures and 1.85 mm panel adaptors are housed in a small benchtop case.



## Ease of Use

The easy to use software package, SHF 600 Series Control is the most convenient way to control the DAC. The software reads the individual calibration tables of the DAC and sets the contribution of the bias voltages accordingly. The amplitude of the individual eye openings can be set and is displayed in the graphical user interface (GUI). This enables the user to generate a perfect signal just by a few intuitive clicks.

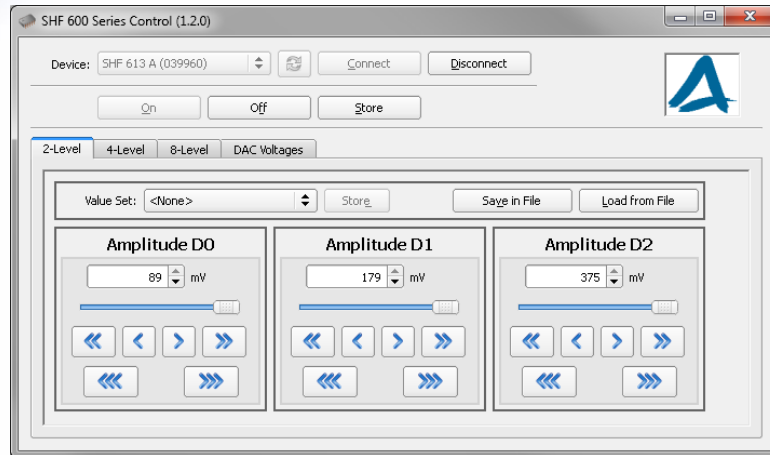


Fig. 3: “SHF 600 Series Control” – GUI

With Option Case, the software package, SHF BCC Control Center is the most convenient way to control the DAC. The software reads the individual calibration tables of the DAC and sets the contribution of the bias voltages accordingly. The amplitude of the individual eye openings can be set and is displayed in the graphical user interface (GUI).

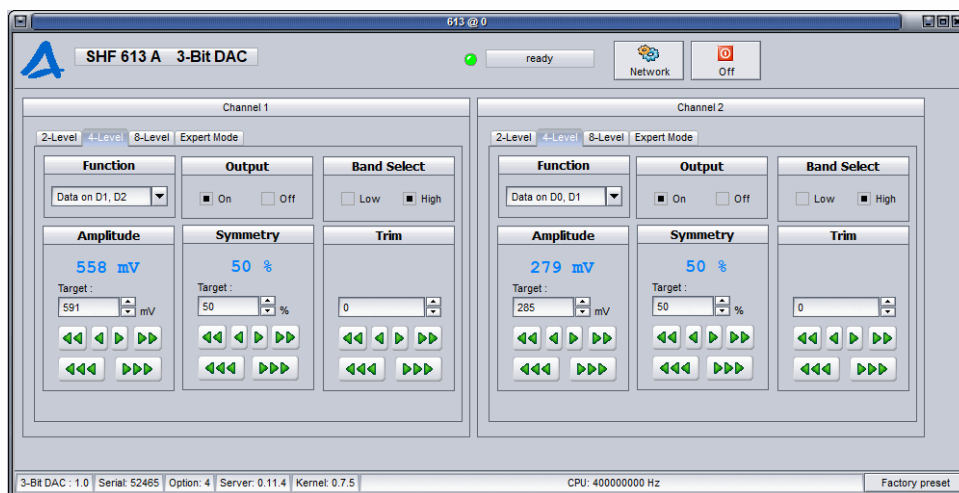


Fig. 4: “SHF BCC Control Center” – GUI

At delivery, the software package for a MS Windows installation including a 1.5m USB cable will be provided. Control software for other operating systems is available on request.



## Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
<b>Input Parameters</b>						
Data Input Voltage	mV <sub>pp</sub>	V <sub>data in</sub>	300	500	800	Clock input amplitude = 500mV
Clock Input Frequency	GHz	f <sub>in</sub>	1		60	
Clock Input Voltage	mV <sub>pp</sub>	V <sub>clk in</sub>	300	500	800	Data input amplitude = 500mV
<b>Output Parameters</b>						
Minimum Output Data Rate	GBaud	R <sub>out,min</sub>			1	
Maximum Output Data Rate	GBaud	R <sub>out,max</sub>	60			
Output Amplitude	mV	V <sub>out</sub>	590	730	850	Single ended, full scale, adjustable up to -6 dB, see table on page 5
Rise- / Fall Time	ps	t <sub>r</sub> /t <sub>f</sub>		6.1	7.1	20%...80%, deconvolved <sup>1</sup>
Equivalent Output Bandwidth	GHz	BW	31	36		Derived from Rise Time using formula <sup>2</sup> , -3 dB bandwidth
<b>Power Requirements (incl. Bias Box)</b>						
Supply Voltage	V	V <sub>ee</sub>	+11.5	+12	+12.5	
Supply Current	mA	I <sub>ee</sub>		520	540	
Power Dissipation	W	P <sub>d</sub>		6.2		@ V <sub>EE</sub> = +12V
<b>Power Requirements (DAC-Module only)</b>						
Supply Voltage	V	V <sub>ee</sub>	-5.2	-5	-4.8	
Supply Current	mA	I <sub>ee</sub>		1000	1100	
Power Dissipation	W	P <sub>d</sub>		5		@ V <sub>EE</sub> = -5V

<sup>1</sup> Calculation based on typical rise/fall times from oscilloscope data sheet:  $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

<sup>2</sup> Calculation based on formula:  $BW = \frac{0.22}{T_r}$



Power Requirements (with Option Case Single Channel)						
Supply Voltage	V	$V_c$	-11.5	+12	+12.5	2.1 mm DC Power Jack
Supply Current	mA	$I_c$		800	900	
Power Dissipation	W	$P_d$		9.6	10.8	@ $V_c = +12V$
Power Requirements (with Option Case Dual Channel)						
Supply Voltage	V	$V_c$	-11.5	+12	+12.5	2.1 mm DC Power Jack
Supply Current	mA	$I_c$		1450	1600	
Power Dissipation	W	$P_d$		17.4	20	@ $V_c = +12V$
Bias Voltages						
Bias Adjust 1 for D0, D1 & D2	V	$V_{Bias1}$	-3.3		0	
Bias Adjust 2 for D0, D1 & D2	V	$V_{Bias2}$	-3.3		0	
Conditions						
Case Temperature <sup>3</sup>	°C	$T_{case}$	10		45	

## Typical Output Amplitudes

Below mentioned values assume no attenuation to be set in the control software. The output amplitude of the DAC can be reduced by 0 to -6 dB by making the appropriate setting in the control software.

Output Amplitude				
Input D2 (MSB)	Input D1	Input D0 (LSB)	Minimum Output Amplitude [mV]	Maximum Output Amplitude [mV]
-	-	On	80	130
-	On	-	160	240
On	-	-	350	480

The typical output amplitude of a multilevel signal can be calculated by accumulating the typical output amplitudes of all applied input ports of the DAC as shown in the table above. Thus the full scale output swing (all inputs active) accumulates as follows:

On	On	On	590	850
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<sup>3</sup> tr / tf of the output data signal can be slightly decreased by applying additional cooling measures like heat sinks or cooling fans.

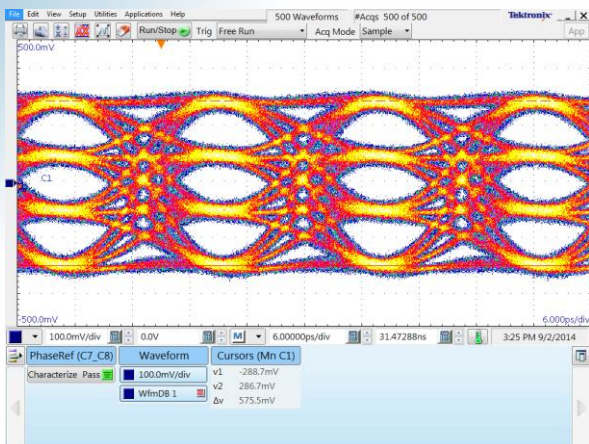




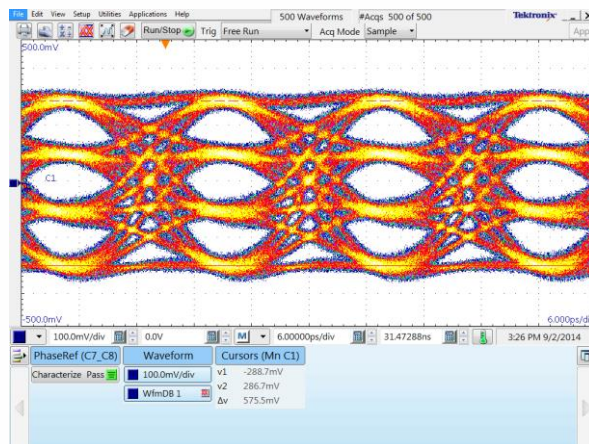
## Typical Output Eye Diagrams

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2<sup>31</sup>-1) and a Tektronix DSA 8300 Digital Serial Analyzer (DSA) with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Module (80E11). The outputs of the DAC module had been connected directly to the DSA input with a 6 dB attenuator.

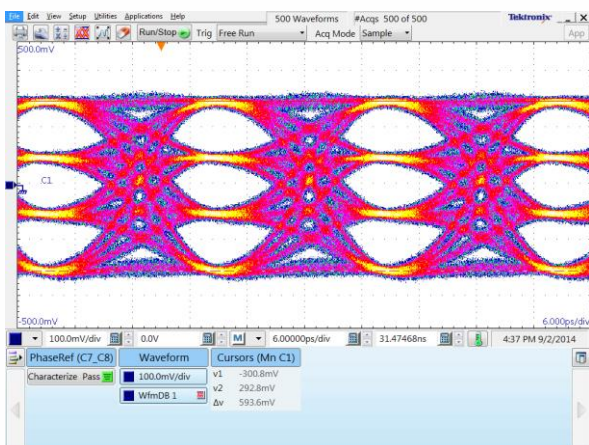
### 4-Level Output Signal Measurement



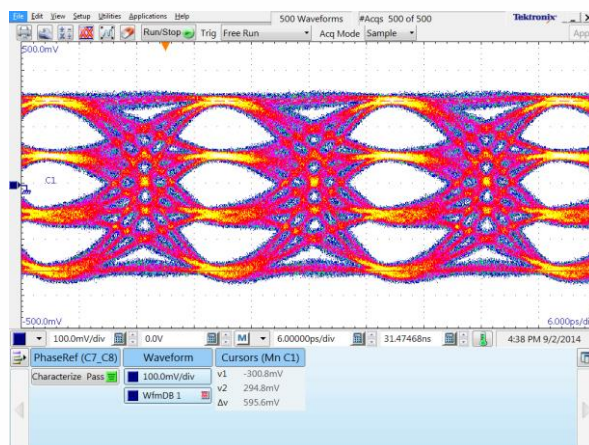
Out @ 60 GBaud



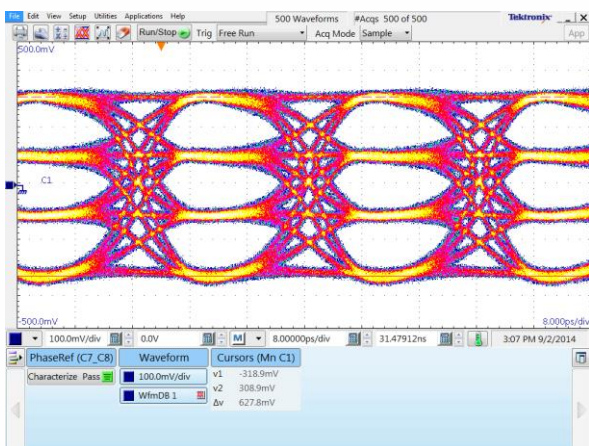
Out! @ 60 GBaud



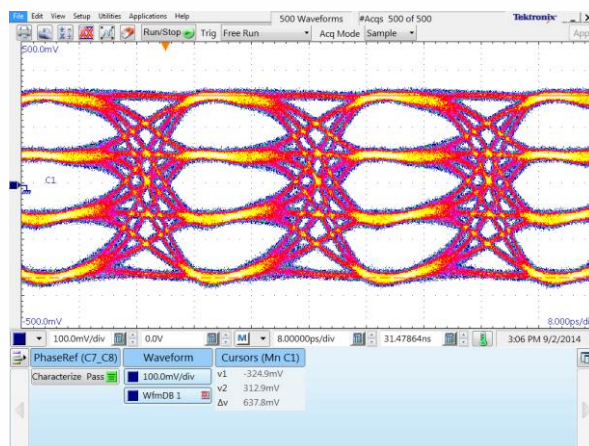
Out @ 56 GBaud



Out! @ 56 GBaud

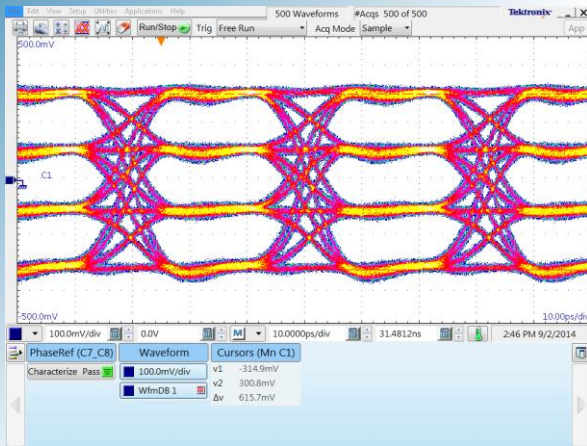


Out @ 43 GBaud

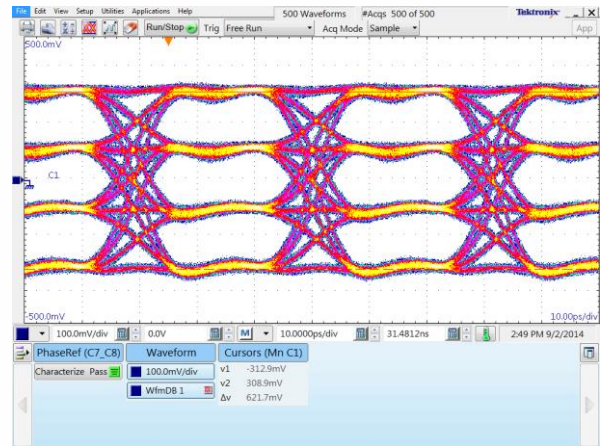


Out! @ 43 GBaud

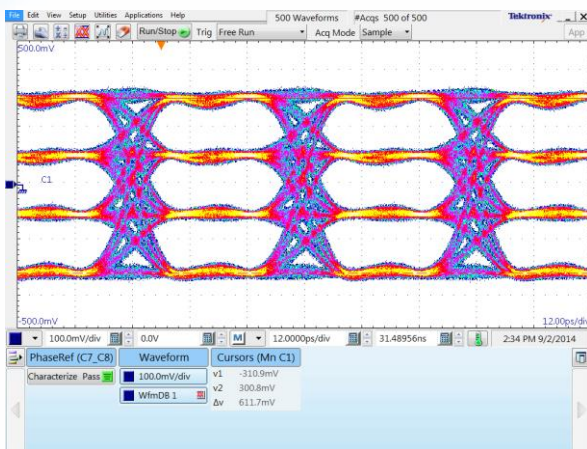




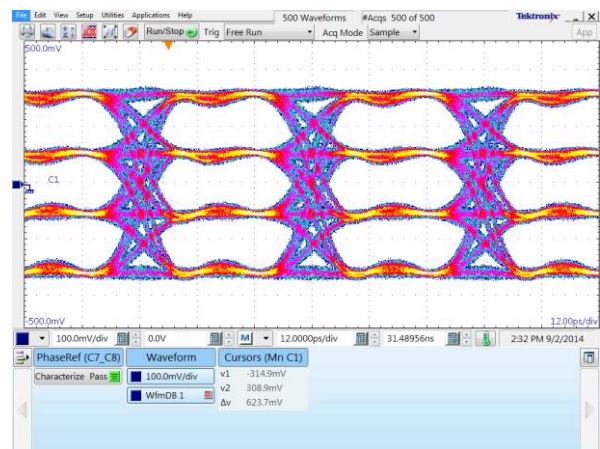
**Out @ 32 GBaud**



**Out! @ 32 GBaud**



**Out @ 28 GBaud**

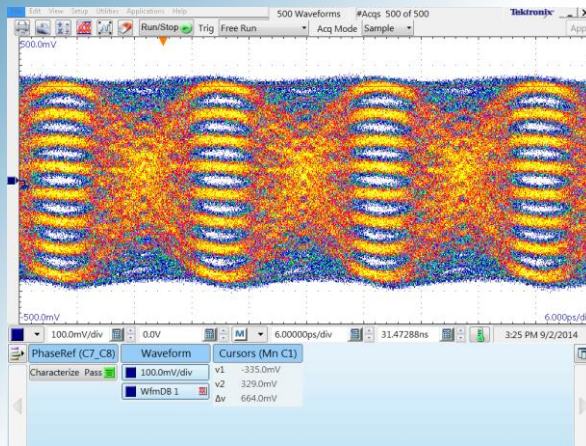


**Out! @ 28 GBaud**

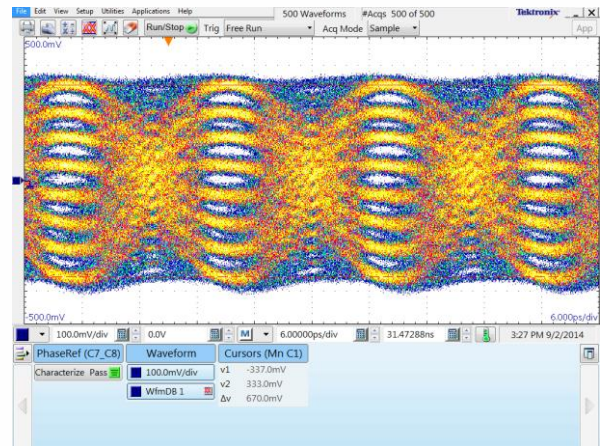




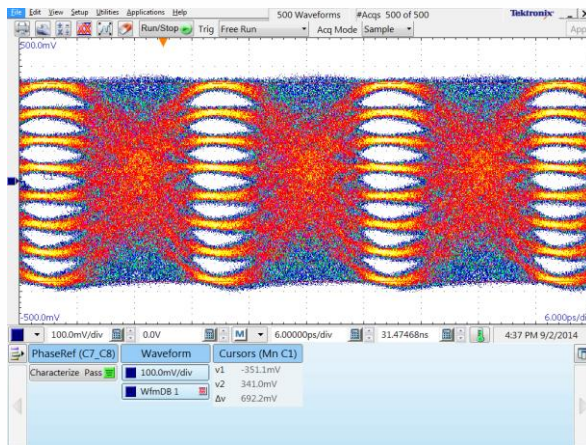
## 8-Level Output Signal Measurement



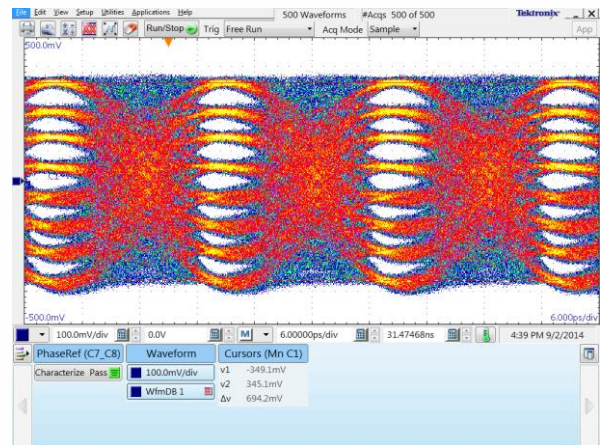
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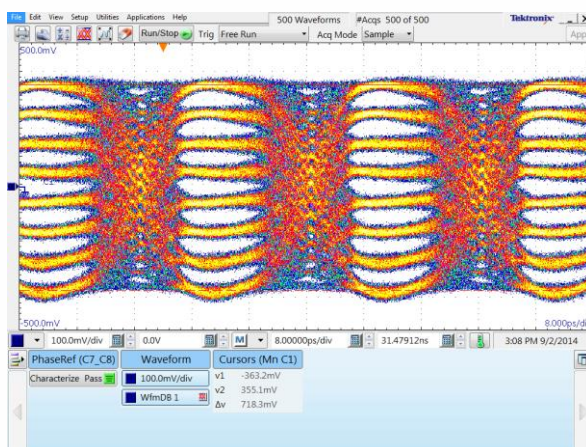
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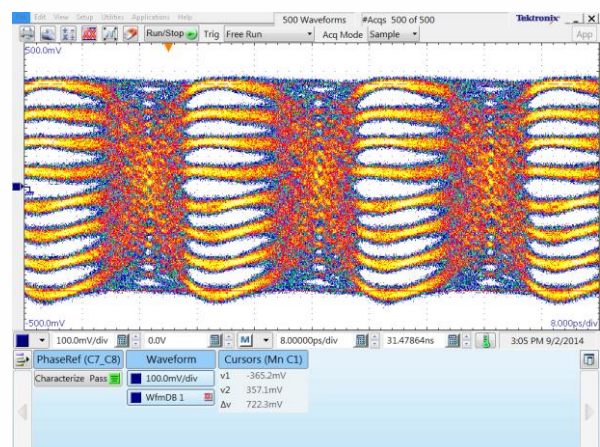
Out @ 56 GBaud



Out! @ 56 GBaud

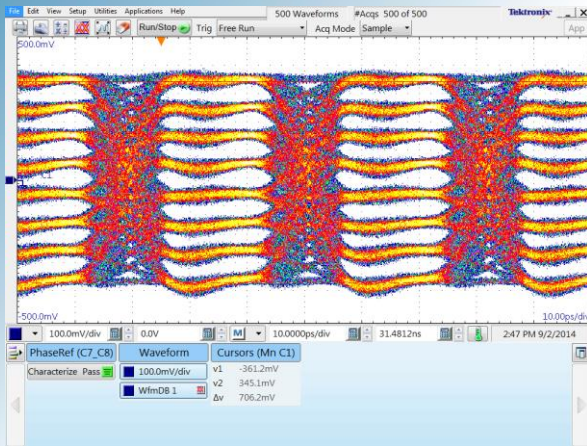


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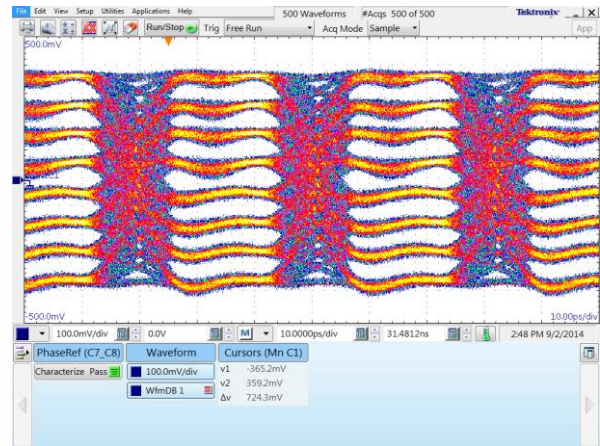


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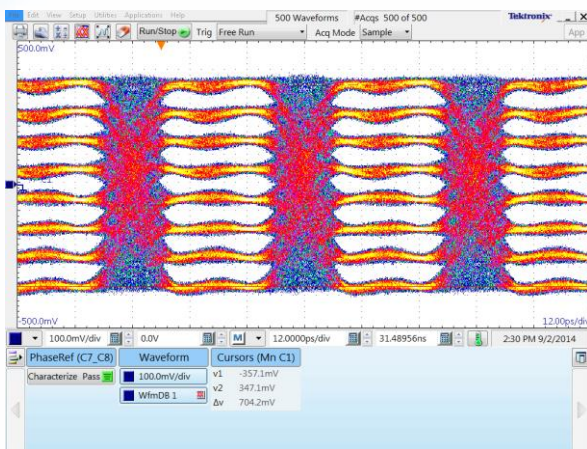




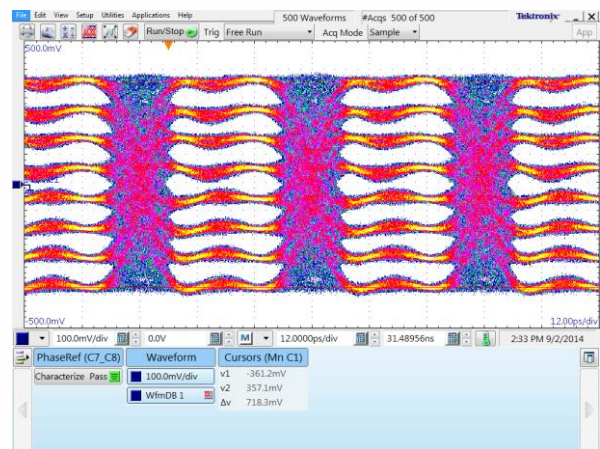
**Out @ 32 GBaud**



**Out! @ 32 GBaud**



**Out @ 28 GBaud**



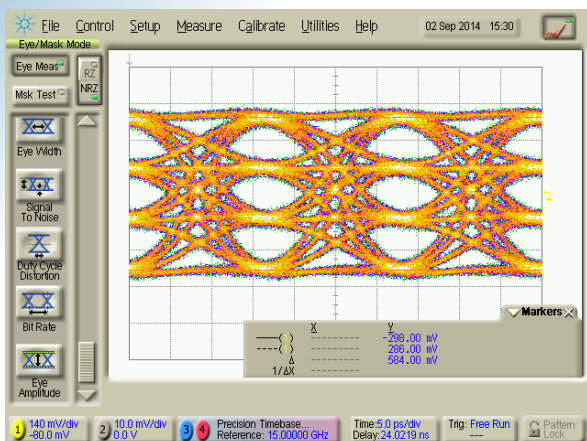
**Out! @ 28 GBaud**



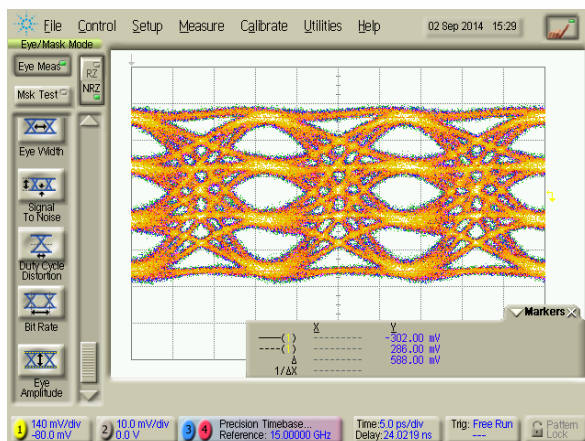
## Typical Output Eye Diagrams

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2<sup>31</sup>-1) and an Agilent Digital Communication Analyzer (DCA) with Precision Timebase Module (86107A) and 70 GHz Sampling Module (86118A). The outputs of the DAC module had been connected directly to the DCA input with a 6 dB attenuator.

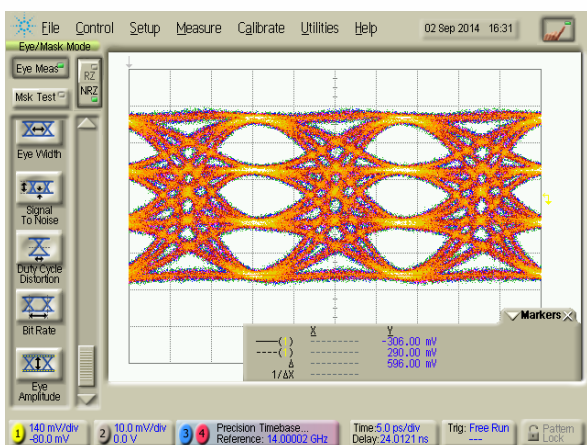
### 4-Level Output Signal Measurement



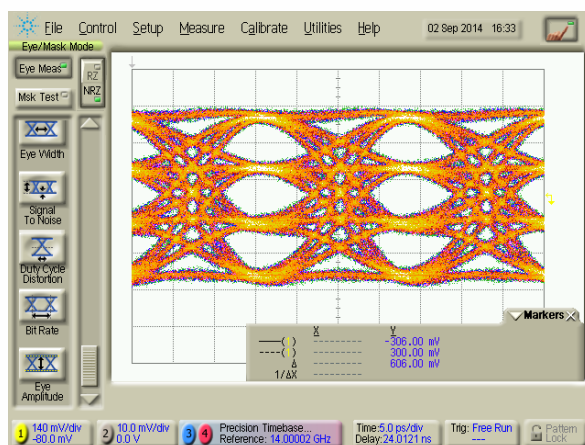
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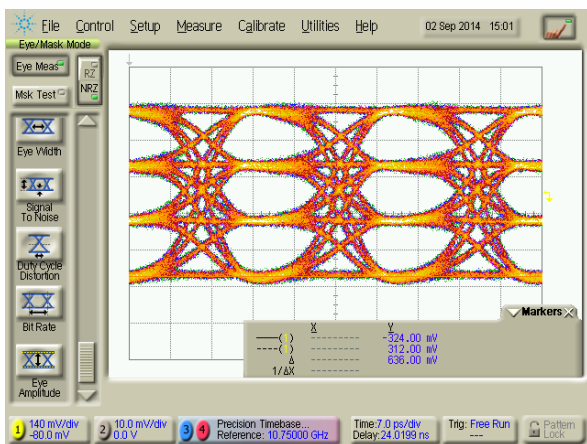
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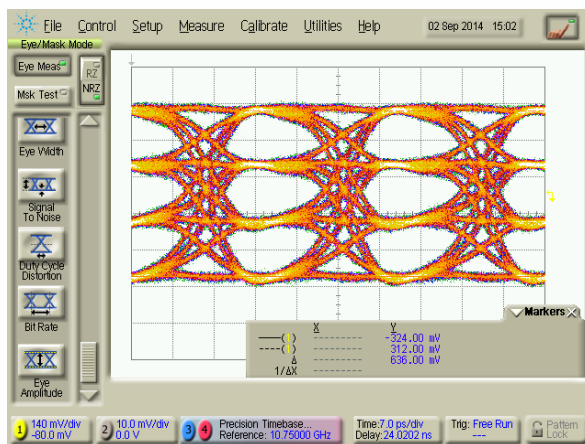
Out @ 56 GBaud



Out! @ 56 GBaud

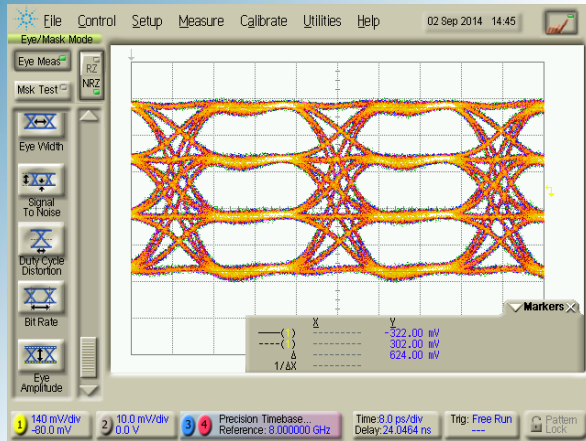


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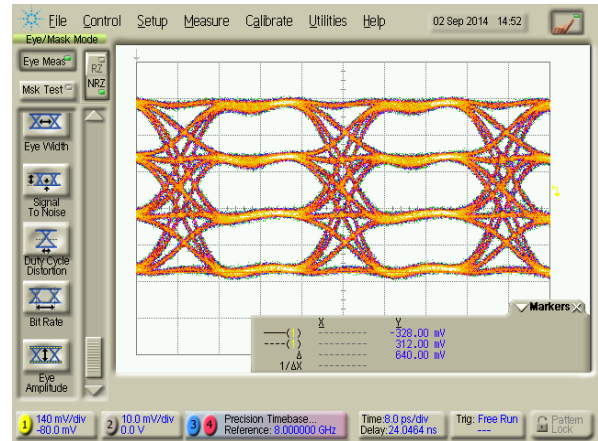


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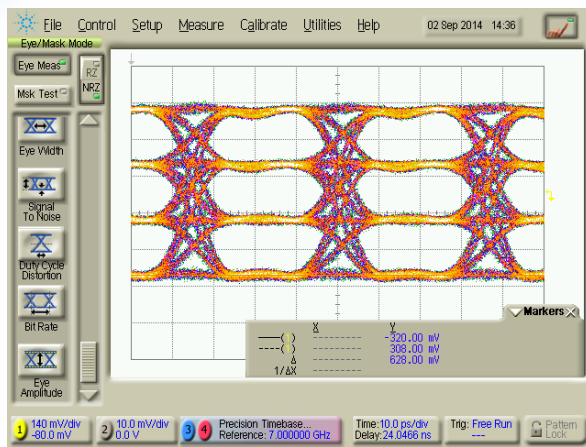




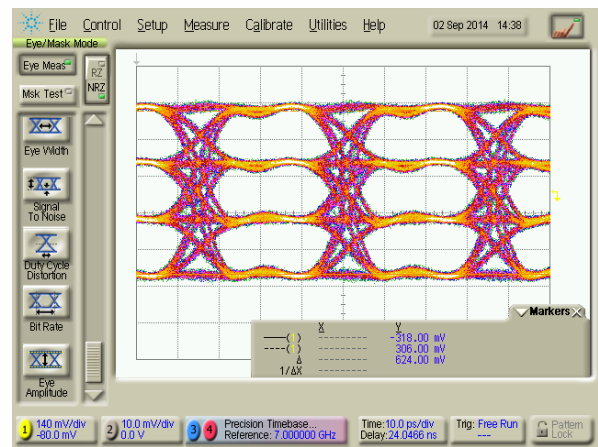
**Out @ 32 GBaud**



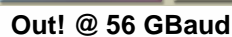
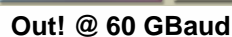
**Out! @ 32 GBaud**



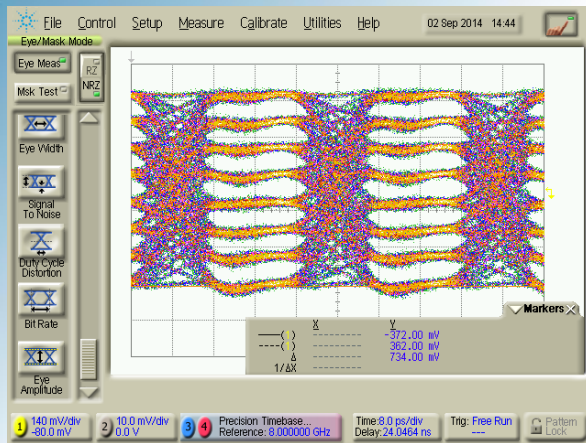
**Out @ 28 GBaud**



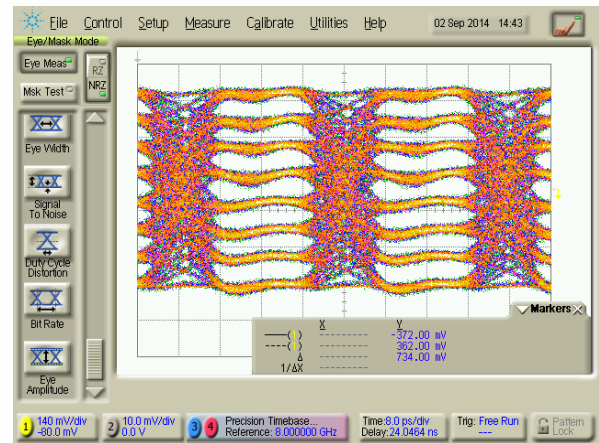
**Out! @ 28 GBaud**



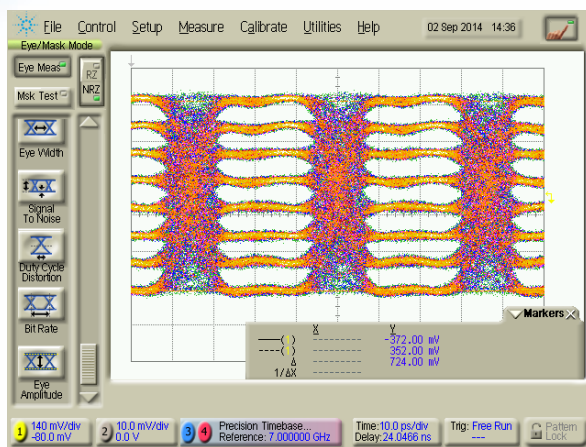




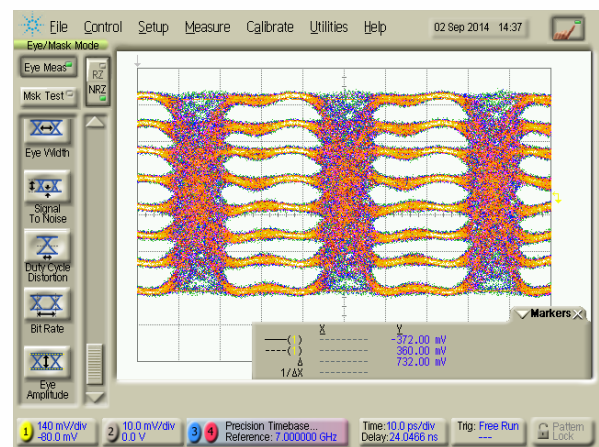
**Out @ 32 GBaud**



**Out! @ 32 GBaud**



**Out @ 28 GBaud**

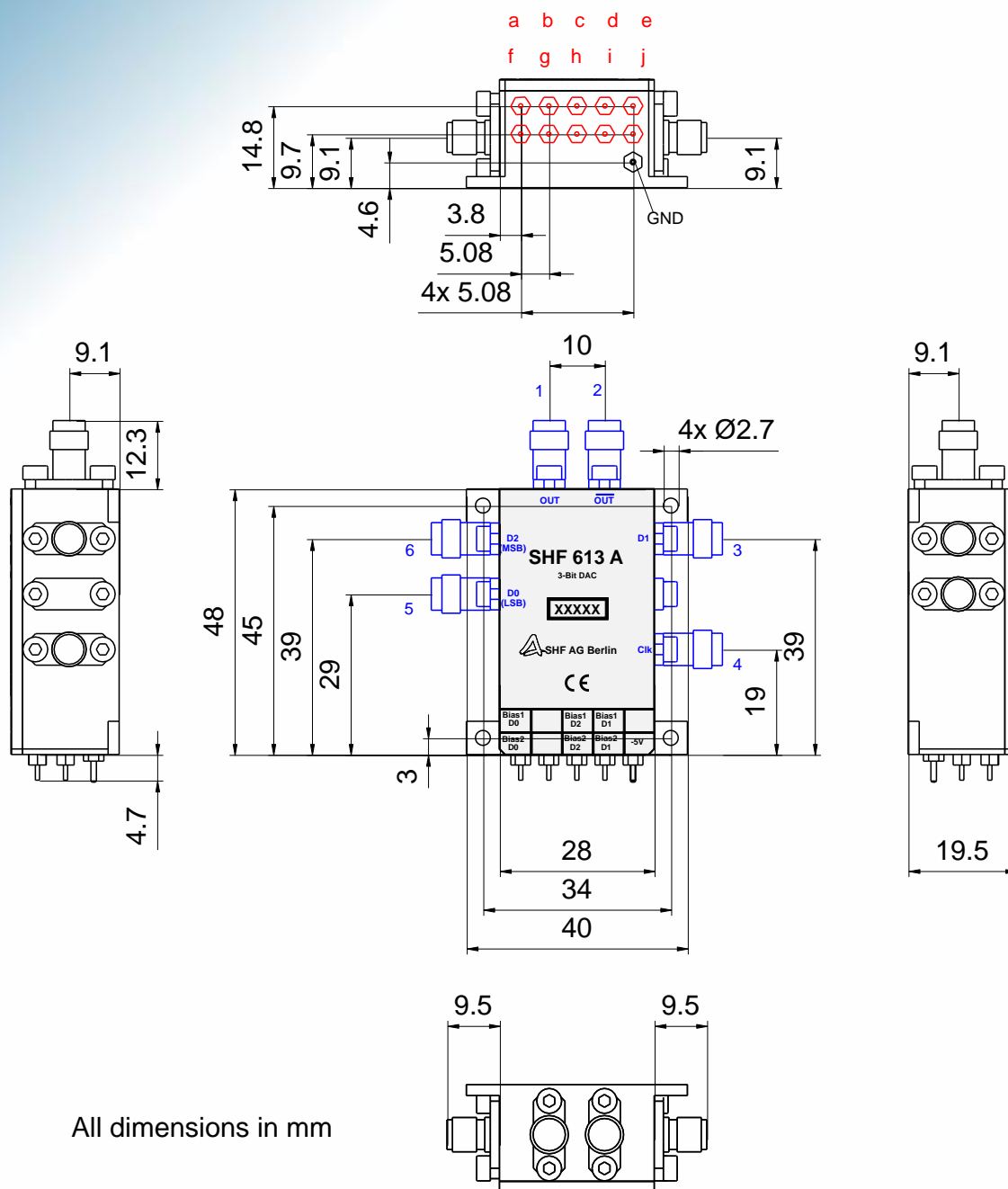


**Out! @ 28 GBaud**





## Outline Drawing - Module



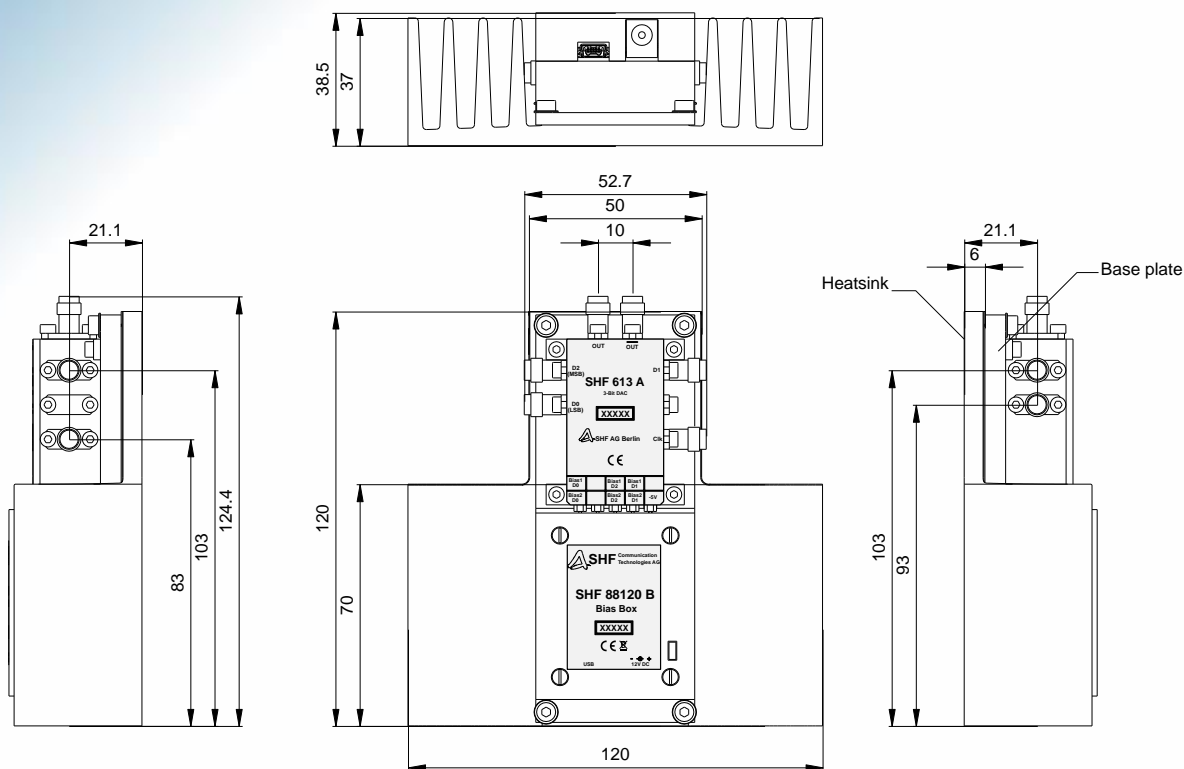
Port	a	b	c	d	e	f	g	h	i	j
Designation	Bias 1 DO		Bias 1 D2	Bias 1 D1		Bias 2 DO		Bias 2 D2	Bias 2 D1	-5V

Port	1	2	3	4	5	6
Designation	Out	Out	D1	Clk	D0 (LSB)	D2 (MSB)
Connector	1.85mm (V) Female					





## Outline Drawing – “Module + Bias Box”- Assembly with Heat Sink



All dimensions in mm





## Outline Drawing – SHF 613 A with Option Case

