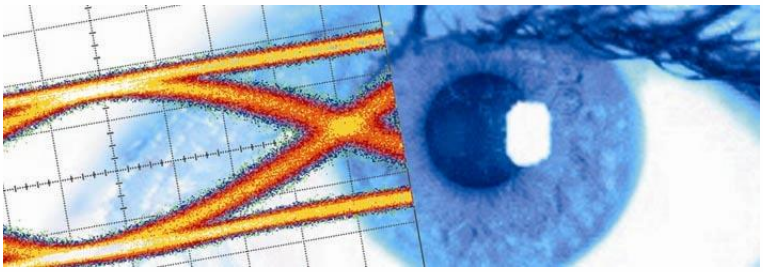
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany

Phone +49 30 772051-0 • Fax +49 30 7531078

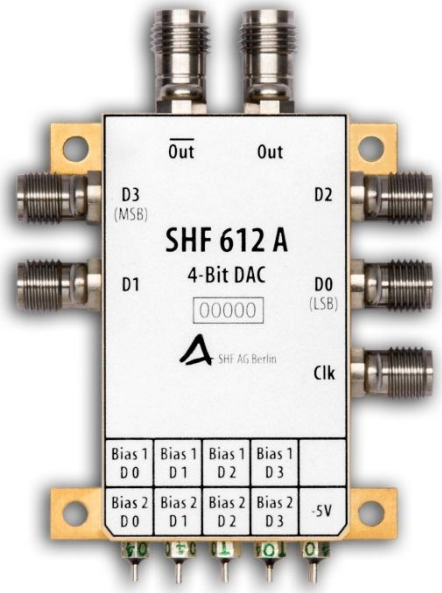
E-Mail: sales@shf.de • Web: http://www.shf.de



Datasheet

SHF 612 A

32 GBaud 4-Bit DAC



Description

The SHF 612 A is a 4-Bit Digital-to-Analog Converter (DAC) operating at data rates up to 32 GBaud for use in broadband test setups and telecom transmission systems. Four 32 Gbps single ended serial data streams are converted into one differential 16-Level data signal at an output data rate of 32 GBaud. By using less input ports it is possible to convert two or three single ended input data serial data streams into an 8-level or 4-Level output signal. A single ended clock signal with the same frequency as the output data rate drives the SHF 612 A.

For data regeneration purposes all input data signals are re-timed by the clock signal. All RF input and output ports are AC-coupled. Unused in- and output ports should be terminated.

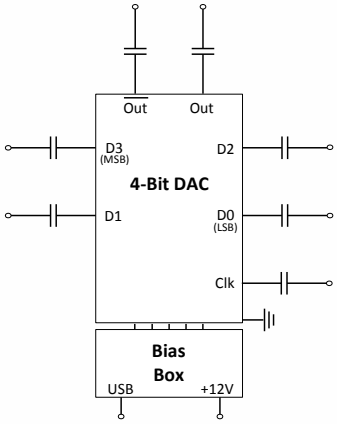
Features

- Broadband operation up to 32 GBaud
- Differential data output, 630 mV single ended output swing
- Single ended clock and data inputs
- Latched input ports
- Output level control
- USB controlled Bias Box

Applications

- 100G Ethernet development and prototyping
- 200G and 400G systems
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block Diagram



® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Bias Box

At delivery, the bias box SHF 88120 A is mounted on a common base plate, together with the SHF 612 A 4-Bit DAC (Fig.1). All bias voltages are provided by this bias box which is controlled by a PC via a USB interface. The easy to use software package is a complementary part of each delivery. For system applications it is possible to remove the bias box. In that case the operating voltages have to be supplied by the customer's circuitry. The Bias Box can only be used with the delivered power supply. Using other power supplies can damage the Bias Box. At delivery, the software package including a 1.5m USB cable will be provided.

Fig. 1: "SHF 612 A + Bias Box"-Assembly

SHF 600 Series Control - Software

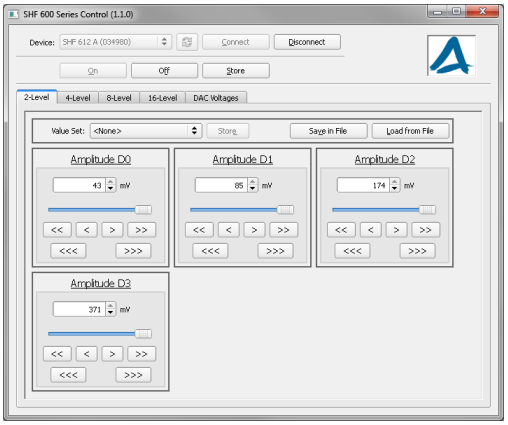


Fig. 2: "SHF 600 Series Control" – GUI

Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$	400	500	1000	Clock input amplitude = 500mV
Clock Input Frequency	GHz	f_{in}	1		32	
Clock Input Voltage	mV_{pp}	$V_{clk\ in}$	400	500	1000	Data input amplitude = 500mV
Output Parameters						
Minimum Output Data Rate	GBaud	$R_{in,min}$			1	
Maximum Output Data Rate	GBaud	$R_{in,max}$	32			
Maximum Output Amplitude (16-Level Signal)	mV	V_{out}	560	630	710	Single ended, full scale, adjustable up to -15dB, see table 1 on page 5
Analog Output Bandwidth	GHz	B		19		-3dB bandwidth @ full scale, see Fig.3 on page 5
Power Requirements (incl. Bias Box)						
Supply Voltage	V	V_{ee}	+11.75	+12	+12.25	
Supply Current	mA	I_{ee}		310	330	
Power Dissipation	W	P_d		3.7		
Power Requirements (DAC-Module only)						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		600	620	
Power Dissipation	W	P_d		3		@ V_{EE} = -5V
Bias Voltages						
Bias Adjust 1 for D0,D1,D2,D3	V	V_{Bias1}	-3.3		0	
Bias Adjust 2 for D0,D1,D2,D3	V	V_{Bias2}	-3.3		0	
Conditions						
Case Temperature	°C	T_{case}			45	

Typical Output Amplitude

Signal Type	Input D3 (MSB)	Input D2	Input D1	Input D0 (LSB)	Typical Output Amplitude [mV] (Spread = ±1dB)	Comment
Binary	-	-	-	On	**43**	-
Binary	-	-	On	-	**85**	-
Binary	-	On	-	-	**175**	-
Binary	On	-	-	-	**371**	-
4-Level	-	-	On	On	**126**	achievable output amplitudes using the 4/8/16-level presets for equal output eye heights
4-Level	-	On	On	-	**245**	
4-Level	On	On	-	-	**520**	
8-Level	-	On	On	On	**295**	
8-Level	On	On	On	-	**595**	
16-Level	On	On	On	On	**630**	

Table 1: Typical Output Amplitude

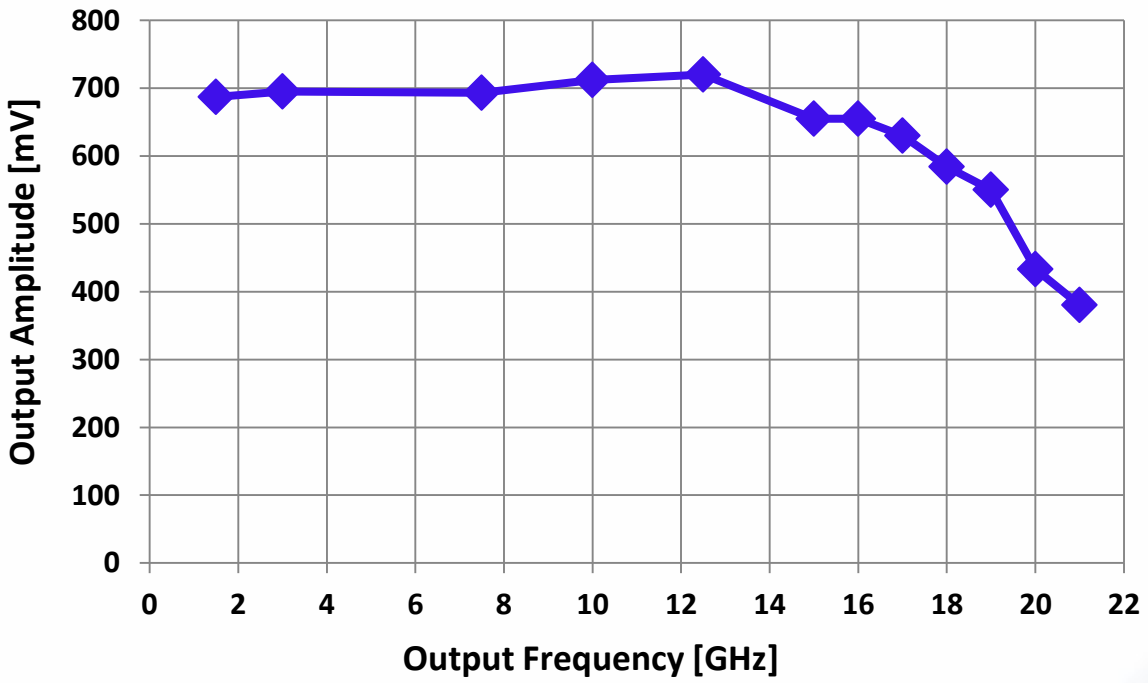


Fig. 3: Analog Output Amplitude – measured at full scale with 0-1-Output-Pattern

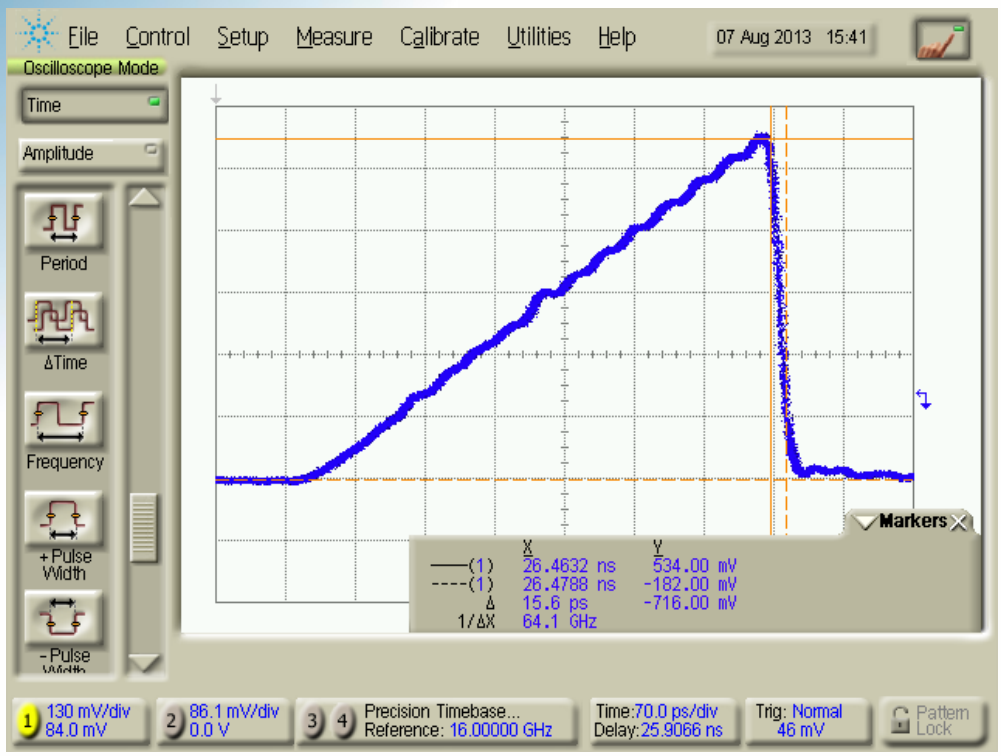
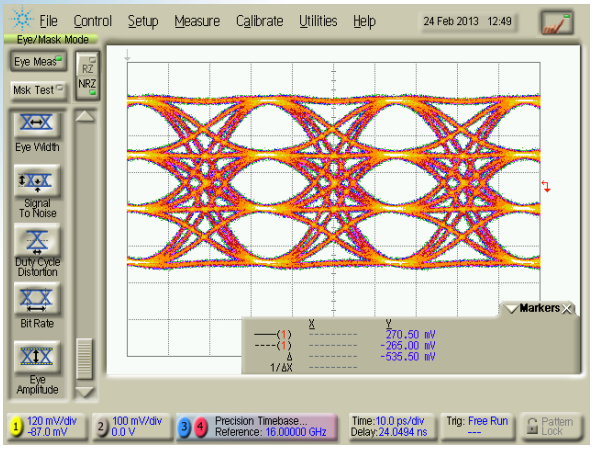


Fig. 4: 16-step ramp @ 32GS/s

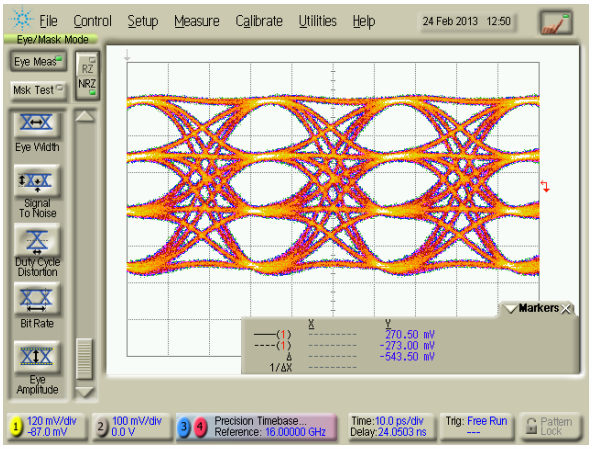
Typical Output Eye Diagrams

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2^{31}-1) and an Agilent 86100A Digital Communication Analyzer (DCA) with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the DAC module had been connected directly to the DCA input.

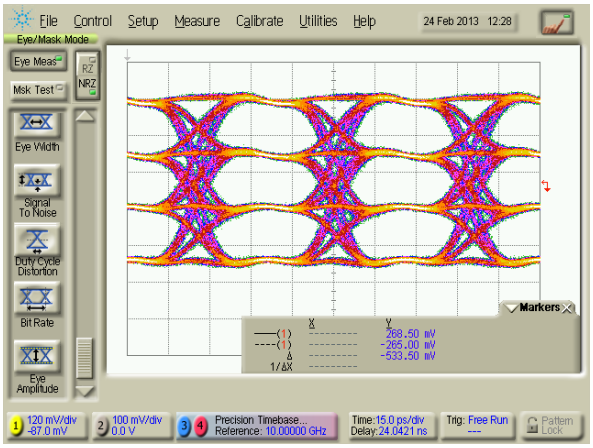
4-Level Output Signals



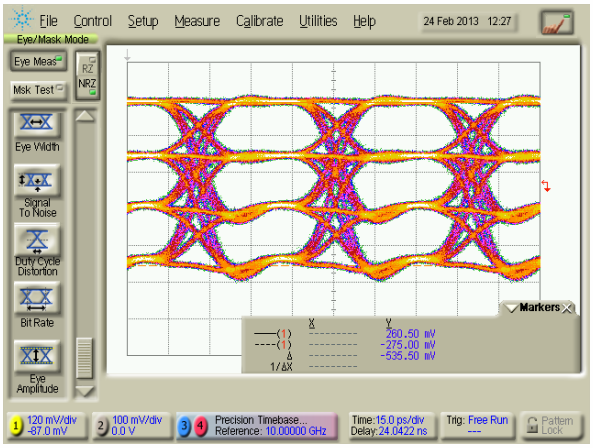
Out @ 32 GBaud



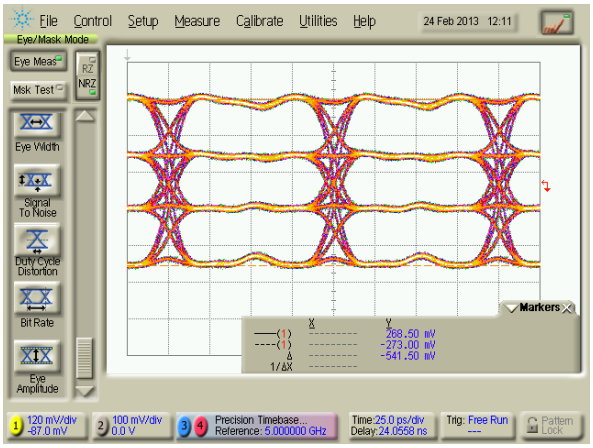
Out! @ 32 GBaud



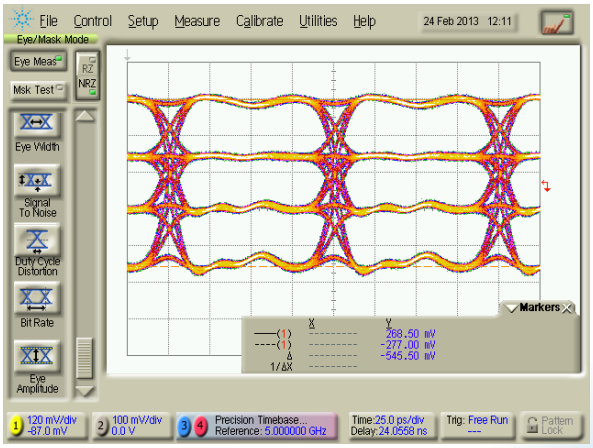
Out @ 20 GBaud



Out! @ 20 GBaud



Out @ 10 GBaud



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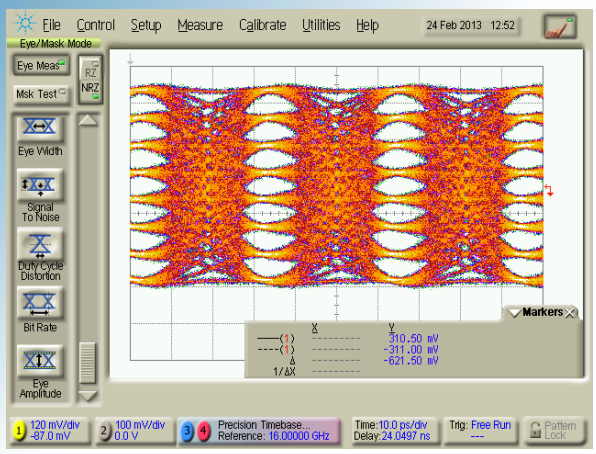
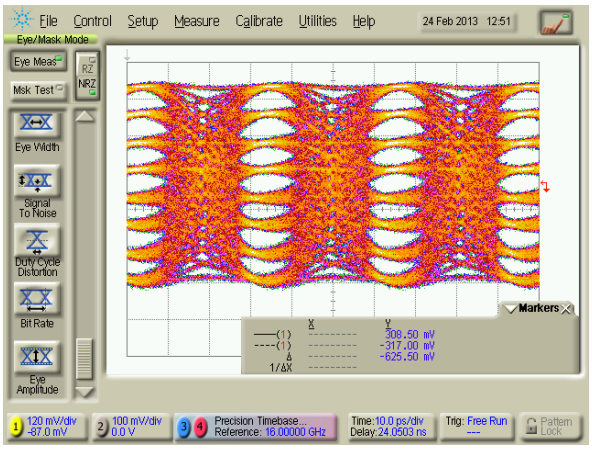
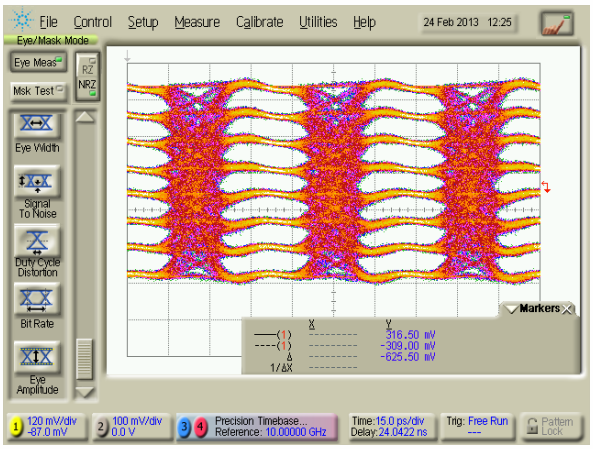
8-Level Output Signals



Out @ 32 GBaud



Out! @ 32 GBaud



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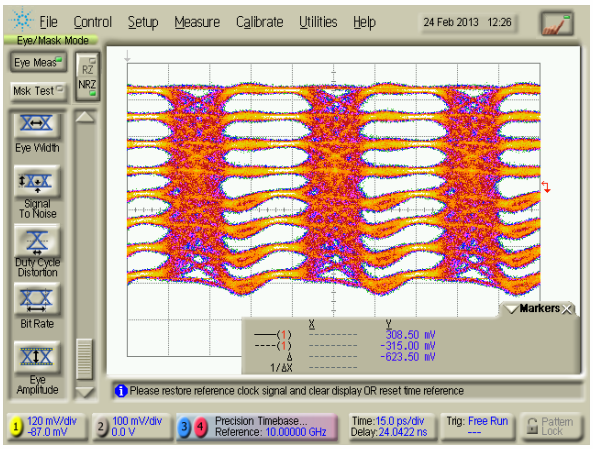

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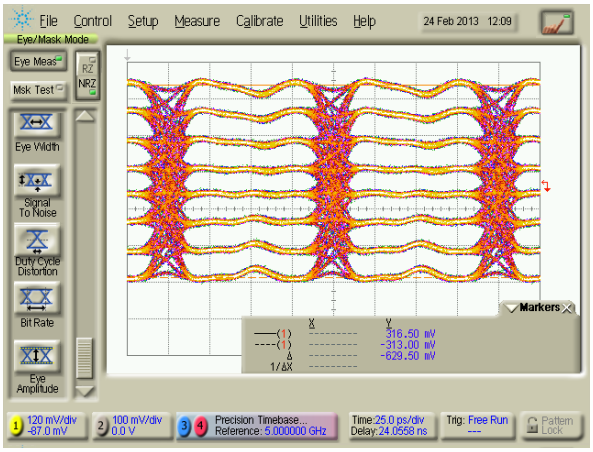

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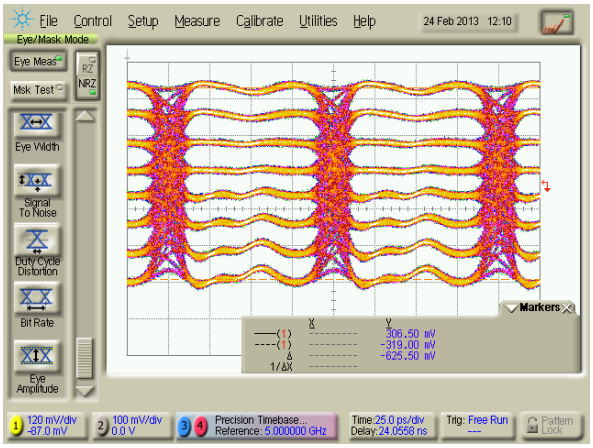

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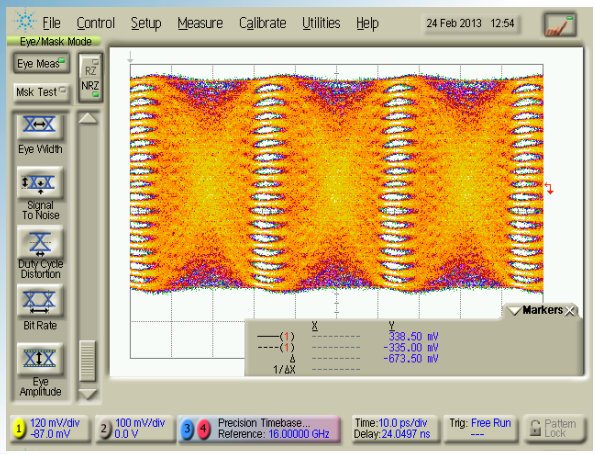
16-Level Output Signals



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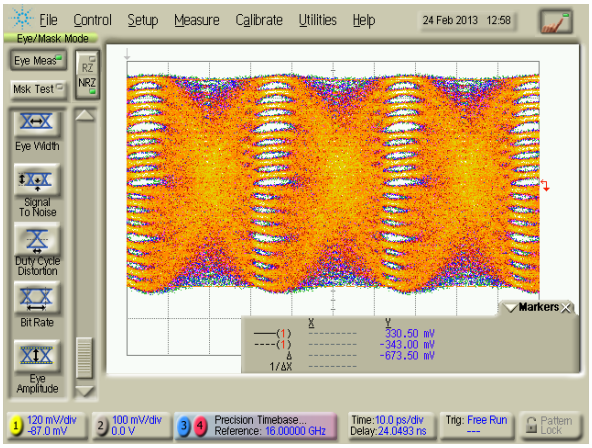

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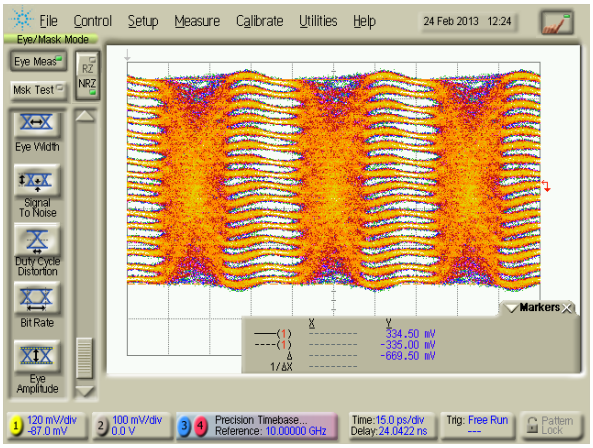

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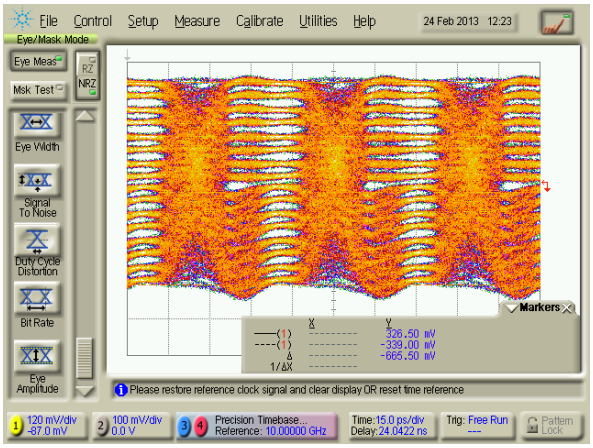

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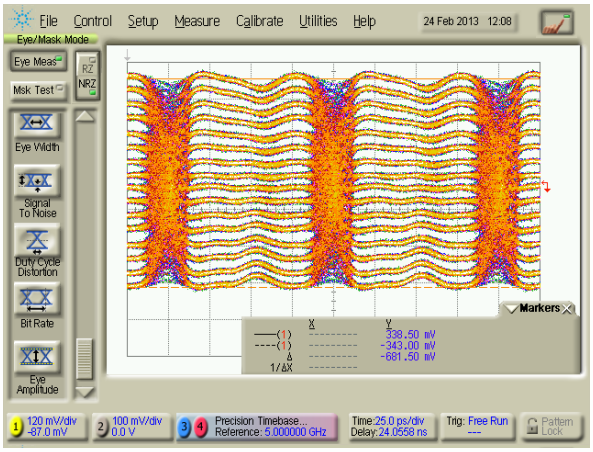

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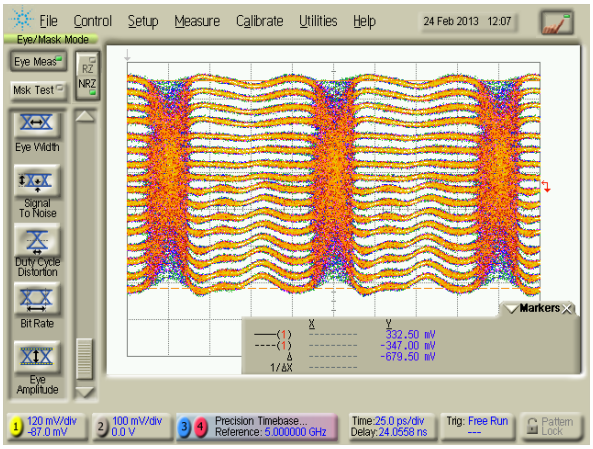

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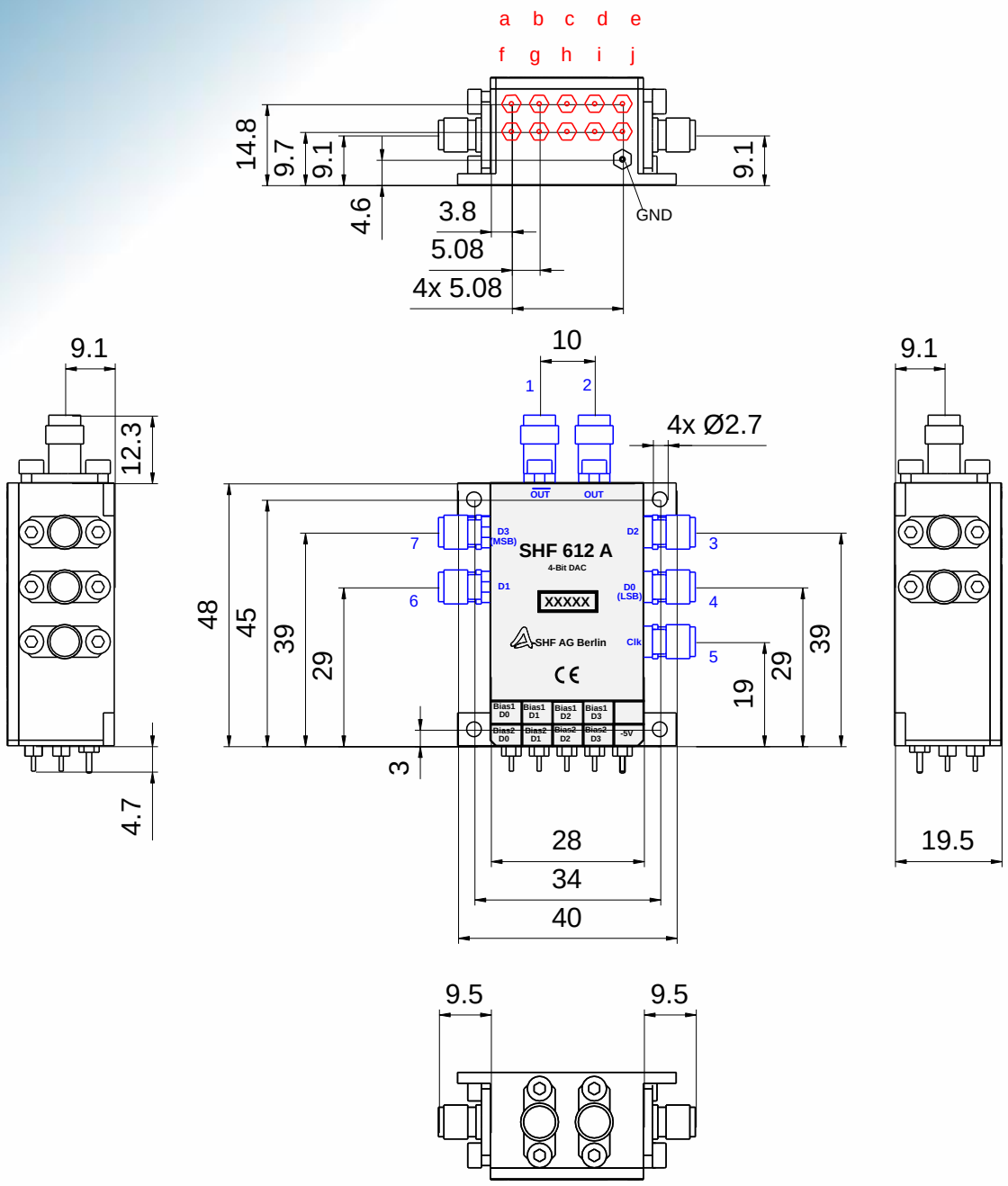
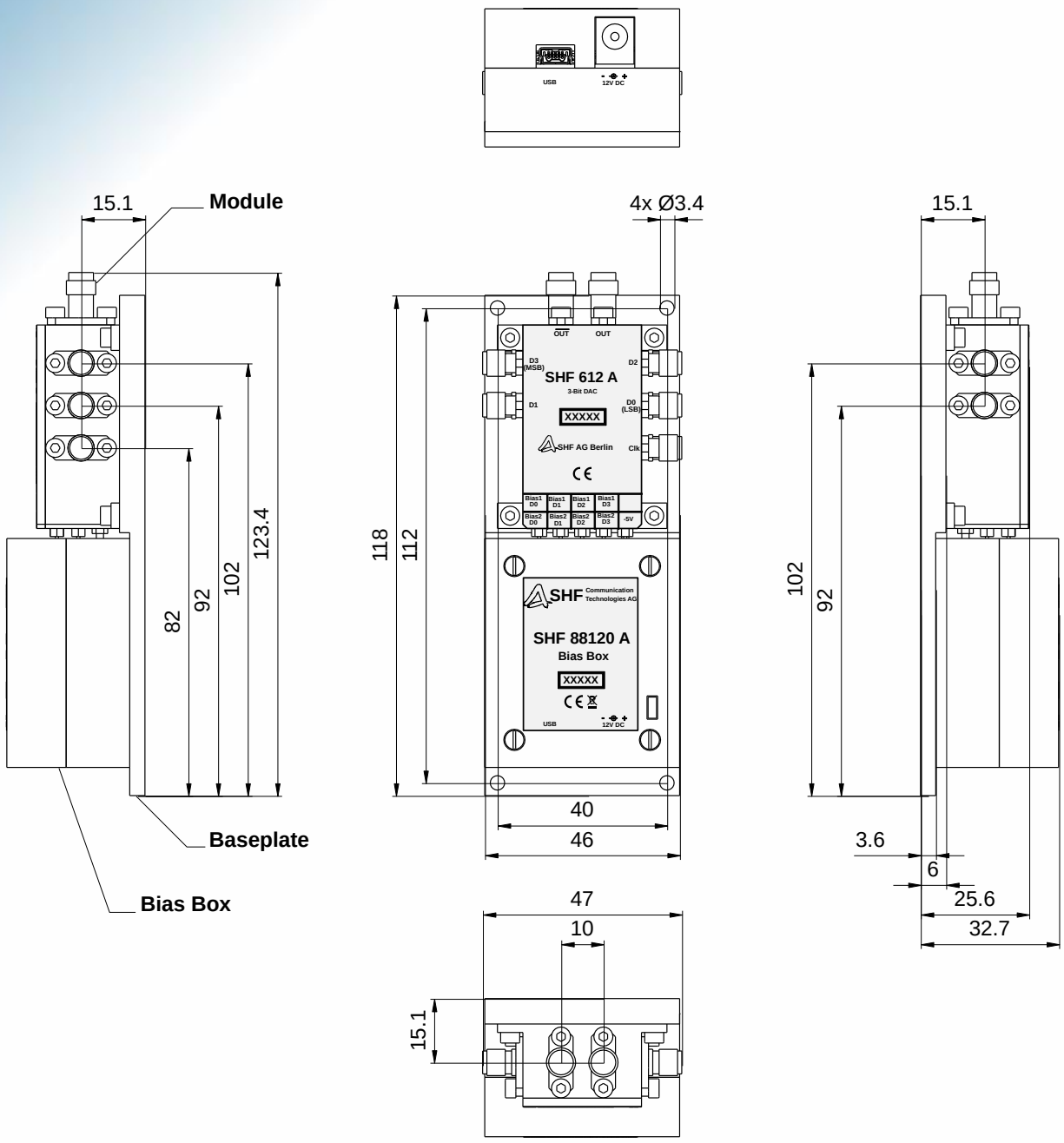
Outline Drawing – Module



Port	a	b	c	d	e	f	g	h	i	j
Designation	Bias 1 DO	Bias 1 D1	Bias 1 D2	Bias 1 D3		Bias 2 DO	Bias 2 D1	Bias 2 D2	Bias 2 D3	-5V

Port	1	2	3	4	5	6	7
Designation	$\overline{\text{Out}}$	Out	D2	D0 (LSB)	Clk	D1	D3 (MSB)
Connector	1.85mm (V) Female		2.92mm (K) Female				

Outline Drawing – “Module + Bias Box”- Assembly



SHF Communication Technologies AG
the bandwidth company