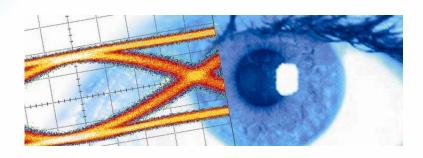


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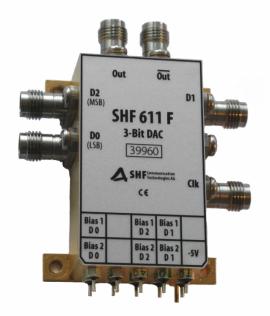
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Datasheet SHF 611 F 32 GBaud 3-Bit DAC







Description

The SHF 611 F is a 3-Bit Digital-to-Analog Converter (DAC) operating at symbol rates up to 32 GBaud for use in broadband test setups and telecom transmission systems. Three single ended serial data streams of up to 32 Gbps are accepted by the DAC and converted into one differential 8-level data signal of up to 32 GBaud. By using two input ports only it is possible to generate 4-level output signals. A single ended clock signal with the same frequency as the data rate drives the SHF 611 F. Thus the baud rate of the resulting PAM signal is as fast as the sample rate of the system.

For data regeneration purposes all input data signals are re-sampled to mitigate any signal impairments resulting e.g. from long cables. Therefore, it becomes possible to place the DAC very close to the DUT.

All RF input and output ports are AC-coupled.

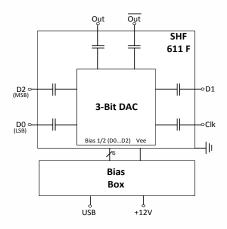
Features

- Broadband operation up to 32 GBaud
- Output baud rate = sample rate
- Differential data output, 600 mV single ended output swing
- · Single ended clock and data inputs
- · Latched input ports
- Output level control
- Bias Box

Applications

- 100G, 200G and 400G system evaluation & development
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel[®]
- Broadband test and measurement equipment

Block Diagram



[®] Fibre Channel is a registered trademark of the Fibre Channel Industry Association





Bias Box

At delivery, the Bias Box SHF 88120 B is mounted on a common base plate, together with the SHF 611 F 3-Bit DAC (Fig.1). All bias voltages are provided by this Bias Box which is controlled by a PC via a USB interface. The easy to use software package is a complementary part of each delivery. For system applications it is possible to remove the Bias Box. In that case the operating voltages have to be supplied by the customer's circuitry.

It is recommended to use the Bias Box only with the delivered power supply. Using other power supplies can damage the Bias Box.



Fig. 1: "SHF 611 F + Bias Box"- Assembly

SHF 600 Series Control - Software

At delivery, the software package for a MS Windows installation including a 1.5m USB cable will be provided. Control software for other operating systems is available on request.

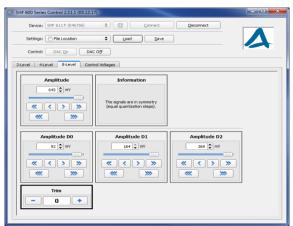
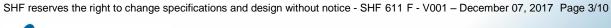


Fig. 2: "SHF 600 Series Control" - GUI

Heat Sink

The provided heat sink can be disassembled by the customer. In this case it is required to provide other cooling measures to ensure that the maximum case temperature specified on page 4 will not be exceeded.







Specifications

Parameter	Unit	Symbol	Min.	Тур.	Max.	Comment
Input Parameters						
Data Input Voltage	mV_{pp}	V _{data in}	300	500	800	Clock input amplitude = 500mV
Clock Input Frequency	GHz	f _{in}				Equates to the output data rate
Clock Input Voltage	mV_{pp}	V _{clk in}	300	500	800	Data input amplitude = 500mV
Output Parameters						
Minimum Output Data Rate	GBaud	R _{out,min}			1	
Maximum Output Data Rate	GBaud	R _{out,max}	32			
Output Amplitude	mV	V _{out}	525	630	805	Single ended, full scale, adjustable up to -6dB, see table on page 5
Rise- / Fall Time	ps	t _r /t _f		8	10	20%80%, deconvolved ¹
Equivalent Output Bandwidth	GHz	BW	22	27		Derived from Rise Time using formula ² , -3 dB bandwidth
Power Requirements (incl. E	Bias Box)					
Supply Voltage	V	V _{ee}	+11.5	+12	+12.5	
Supply Current	mA	l _{ee}		520	540	
Power Dissipation	W	P _d		6.2		@ V _{EE} = +12V
Power Requirements (DAC-I	Module or	nly)				
Supply Voltage	V	V _{ee}	-5.2	-5	-4.8	
Supply Current	mA	l _{ee}		1000	1100	
Power Dissipation	W	P_{d}		5		@ V _{EE} = -5V
Bias Voltages						
Bias Adjust 1 for D0, D1 & D2	V	V _{Bias1}	-3.3		0	
Bias Adjust 2 for D0, D1 & D2	V	V _{Bias2}	-3.3		0	
Conditions						
Case Temperature ³	°C	T _{case}	10		45	

¹ Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\,deconvolved} = \sqrt{(t_{r\,measured})^2 - (t_{r\,oscilloscope})^2} = \sqrt{(t_{r\,meas})^2 - (3.68\,ps)^2}$

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² Calculation based on formula: $BW = \frac{0.22}{Tr}$

 $^{^3}$ tr / tf of the output data signal can be slightly decreased by applying additional cooling measures like heat sinks or cooling fans.



Typical Output Amplitudes

Below mentioned values assume no attenuation to be set in the control software. The output amplitude of the DAC can be reduced by 0 to -6 dB by making the appropriate setting in the control software.

Output Amplitude								
Input D2 (MSB)	Input D1	Input D0 (LSB)	Minimum Output Amplitude [mV]	Maximum Output Amplitude [mV]				
-	-	On	75	115				
-	On	-	150	230				
On	-	-	300	460				

The typical output amplitude of a multilevel signal can be calculated by accumulating the typical output amplitudes of all applied input ports of the DAC as shown in the table above. Thus the full scale output swing (all inputs active) accumulates as follows:

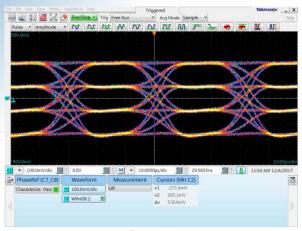
On	On	On	525	805

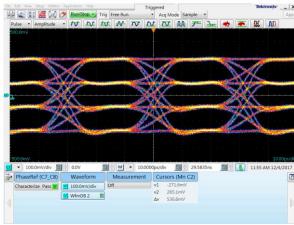


Typical Output Eye Diagrams

The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2³¹-1) and a Tektronix DSA 8300 Digital Serial Analyzer (DSA) with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Module (80E11). The outputs of the DAC module had been connected directly to the DSA input with a 6 dB attenuator.

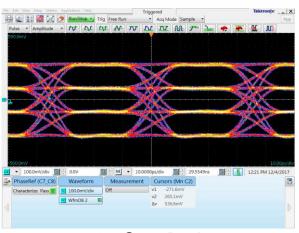
4-Level Output Signal Measurement



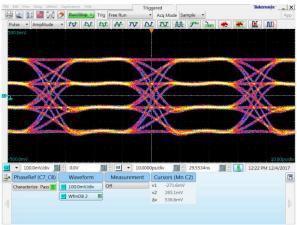


Out @ 32 GBaud

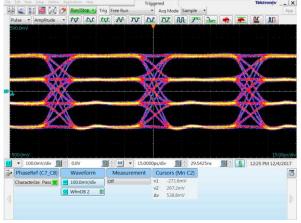
Out! @ 32 GBaud



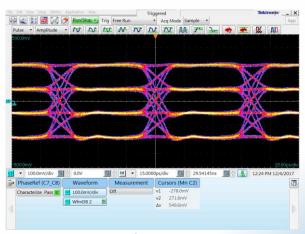




Out! @ 28 GBaud



Out @ 20 GBaud



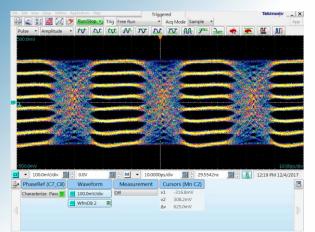
Out! @ 20 GBaud

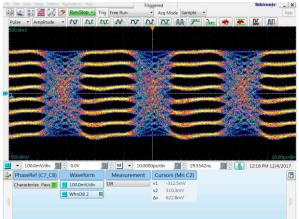
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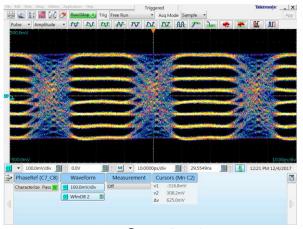
8-Level Output Signal Measurement

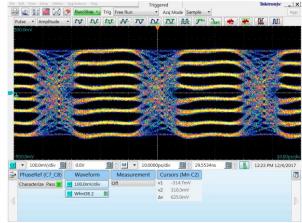




Out @ 32 GBaud

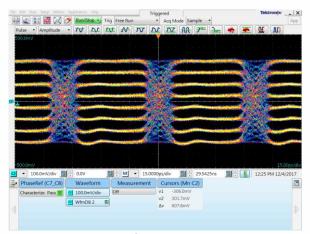
Out! @ 32 GBaud

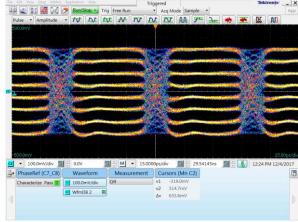




Out @ 28 GBaud

Out! @ 28 GBaud



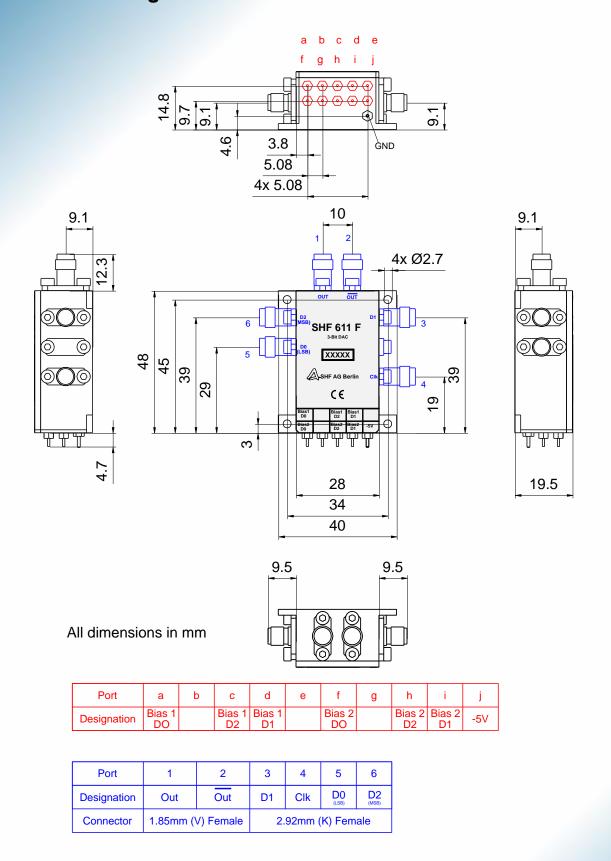


Out @ 20 GBaud

Out! @ 20 GBaud

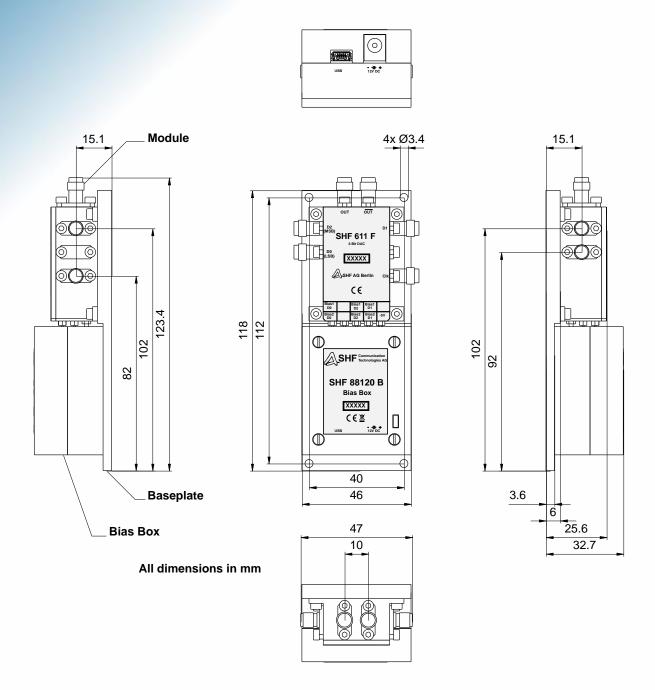


Outline Drawing - Module





Outline Drawing - "Module + Bias Box"- Assembly





Outline Drawing – "Module + Bias Box"- Assembly with Heat Sink

