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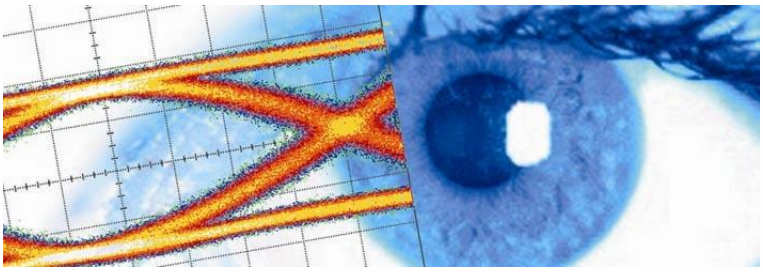


Datasheet

SHF 603 A

120 Gbps

2:1 Multiplexer

Description

The SHF 603 A is a 2:1 Multiplexer operating at data rates up to 120 Gbps for use in broadband test setups and telecom transmission systems. Two single ended serial data streams of up to 60 Gbps are accepted by the multiplexer and converted into one differential data signal of up to 120 Gbps. A single ended clock signal with a frequency half of the output data rate drives the SHF 603 A. All RF in- and output ports are AC-coupled and internally terminated with 50 Ohm to GND. Unused in- or output ports should be terminated with 50 Ohm.

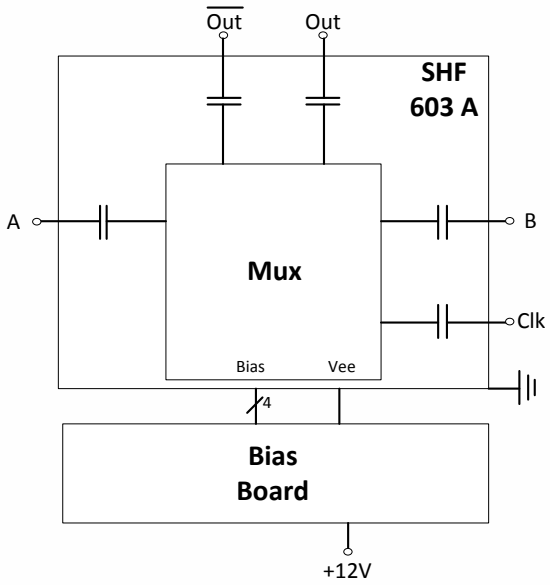
Features

- Broadband operation up to 120 Gbps
- Differential data output, 400mV single ended output swing
- Single ended clock and data inputs
- Output Level Control
- Bias Board

Applications

- 100G, 200G and 400G system evaluation & development
- Telecom transmission
- Broadband test and measurement equipment

Block Diagram



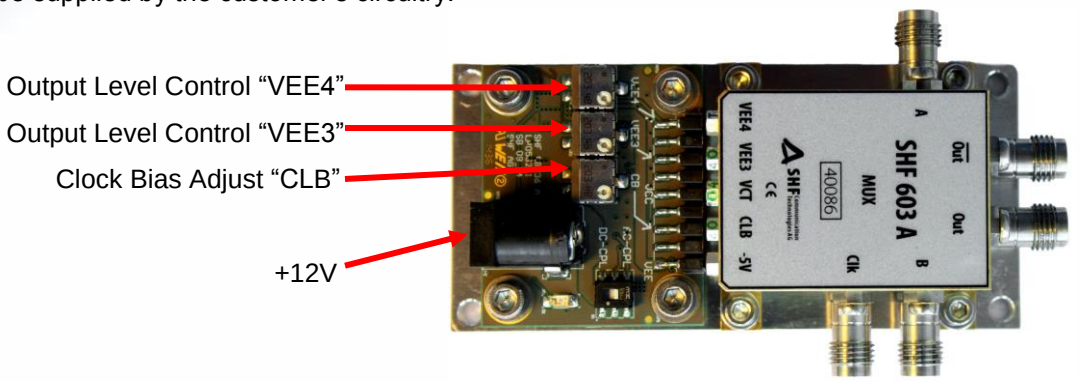
Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 603 A MUX. When using the bias board only one supply voltage of +12V needs to be applied. All operating voltages will be provided by the bias board.

It is recommended to use the Bias Board only with the delivered power supply. Using other power supplies can damage the Bias Board.

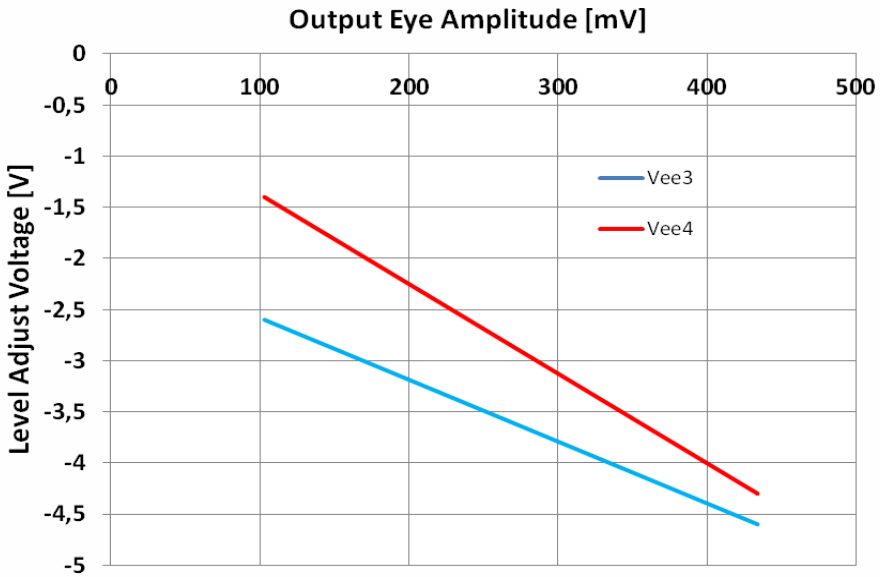
With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level “VEE3/4” and the clock bias voltage “CLB” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



Output Level Adjustment

Output signal amplitude can be reduced by adjusting VEE3 and VEE4 as shown below.



Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$			900	Peak-to-Peak
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on RF Input Ports	V	V_{DCin}	-6		+6	AC coupled input
External DC Voltage on RF Output Ports	V	V_{DCout}	-6		+6	AC coupled output
DC Supply Voltage	V	V_{cc}	0		+13	

Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$	300		800	
Clock Input Frequency	GHz	f_{in}	2		60	
Clock Input Voltage	mV_{pp}	$V_{clk\ in}$	300		800	
Output Parameters						
Minimum Output Data Rate	Gbps	$R_{in,min}$		2	4	@ 500mV_{pp} clock input
Maximum Output Data Rate	Gbps	$R_{in,max}$	120			@ 500mV_{pp} clock input
Maximum Output Amplitude	mV	V_{out}	350	400	500	single ended, adjustable
Rise / Fall time	ps	t_r/t_f		5	6	20% / 80%
Output Jitter, RMS value[1]	fs	J_{rms}		350 450	550 650	≤ 100Gbps ≥ 100Gbps

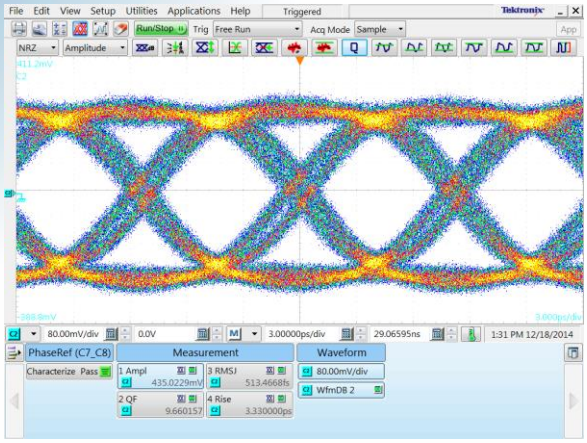
[1] Test condition: Clock Input Signal $Jitter_{RMS}$ <150 fs

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Power Requirements (incl. Bias Board)						
Supply Voltage	V	V_{CC}	+9.0	+12	+12.5	
Supply Current	mA	Icc		420		
Power Dissipation	W	P_d		5.0		@ V_{CC} = +12V
Power Requirements (Mux-Module only)						
Supply Voltage	V	V_{ee}	-5.1	-5.0	-4.9	
Supply Current	mA	I_{ee}		680		
Power Dissipation	W	P_d		3.4		@ V_{EE} = -5V
Bias Voltages						
Output Level Adjust Voltage	V	$V_{EE3/4}$	-4.6		-1.0	adjusts output level, see page 3, $I_{EE3/4}$ ~ 27/30 mA
Output Coupling Ctrl. Voltage	V	V_{CT}	+0.5	+0.7	+1.0	I_{CT} ~ 26 mA
Clock Bias	V	CLB	-2.0	-2.15	-2.3	
Conditions						
Case Temperature[2]	°C	T_{case}	10		45	

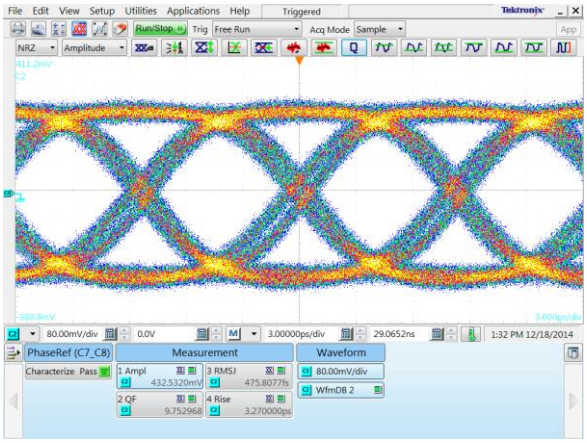
[2] Tr / Tf of the output data signal can be slightly decreased by applying additional cooling measures like heat sinks or cooling fans.

Typical Output Eye Diagrams

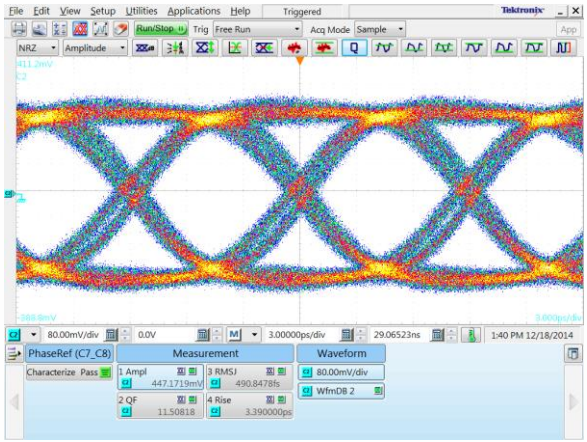
The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2^{31}-1) and a Tektronix DSA 8300 Digital Serial Analyzer (DSA) with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Module (80E11). The outputs of the MUX module had been connected directly to the DSA input.



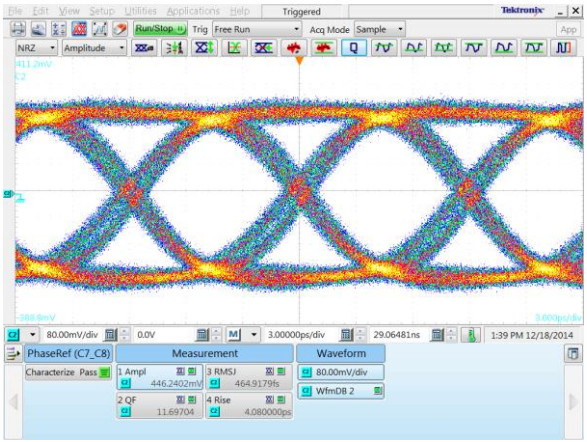
Out @ 120 Gbps



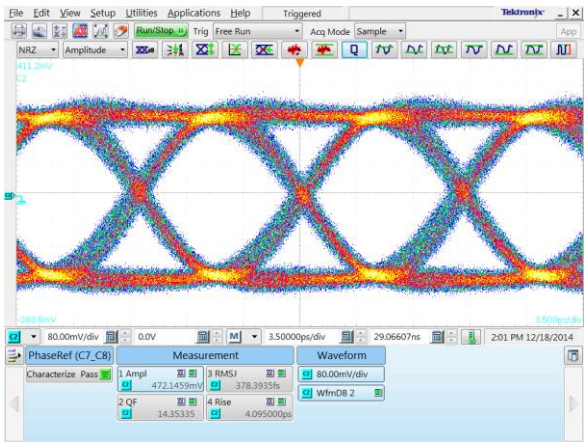
Out inv. @ 120 Gbps



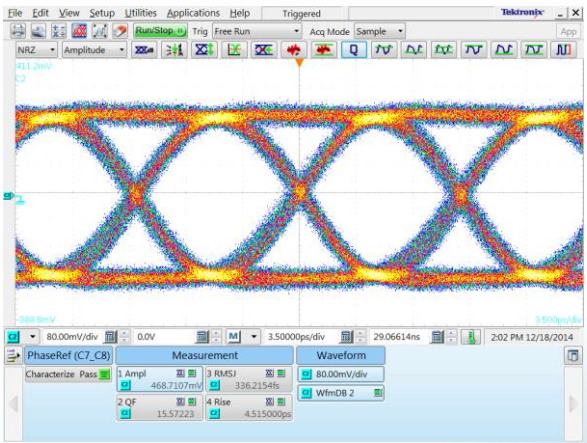
Out @ 112 Gbps



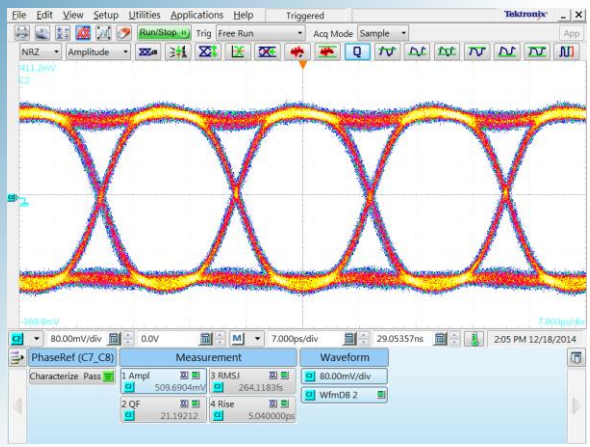
Out inv. @ 112 Gbps



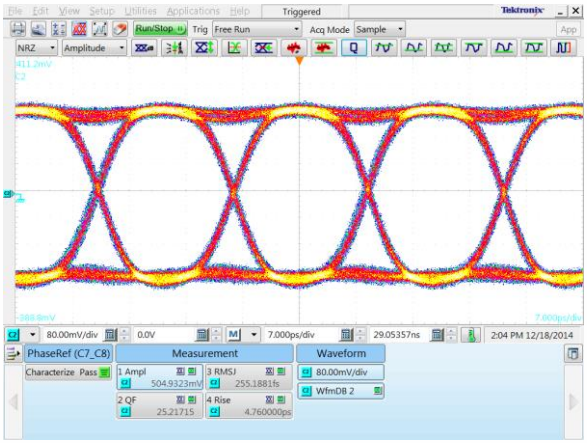
Out @ 100 Gbps



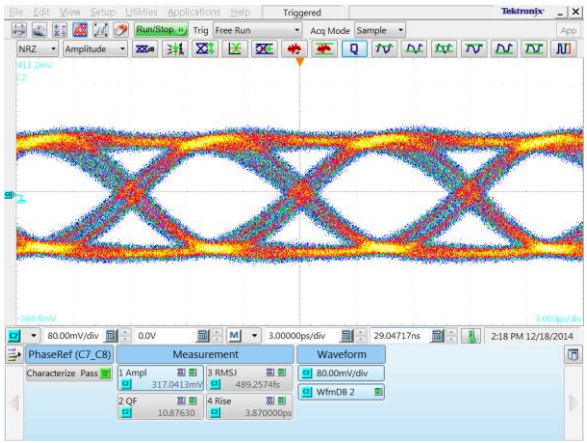
Out inv. @ 100 Gbps



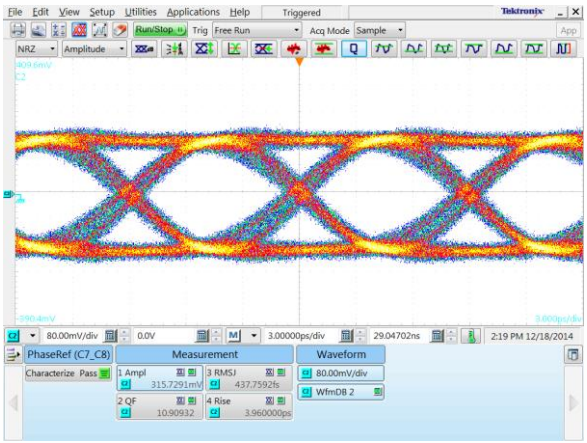
Out @ 60 Gbps



Out inv. @ 60 Gbps



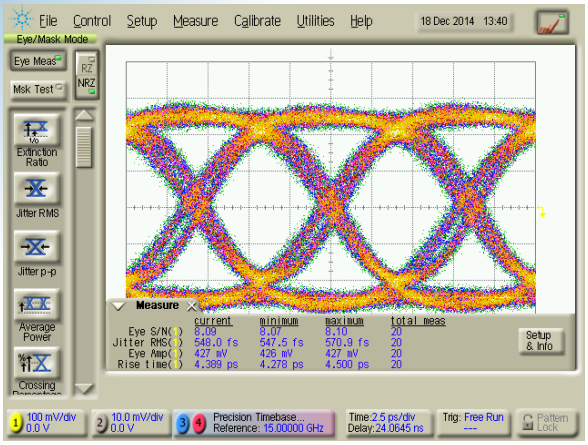
Out @ 112 Gbps, Level = -3dB



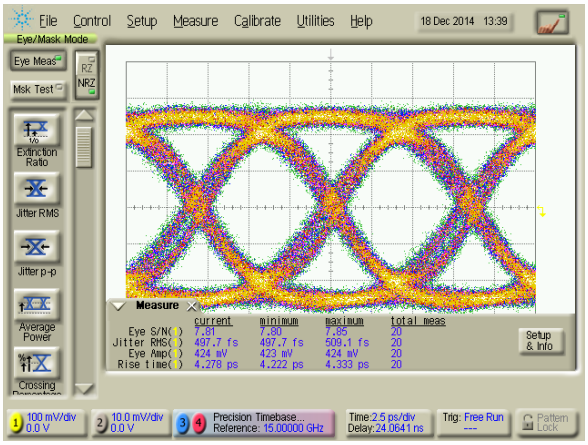
Out! @ 112 Gbps, Level = -3dB

Typical Output Eye Diagrams

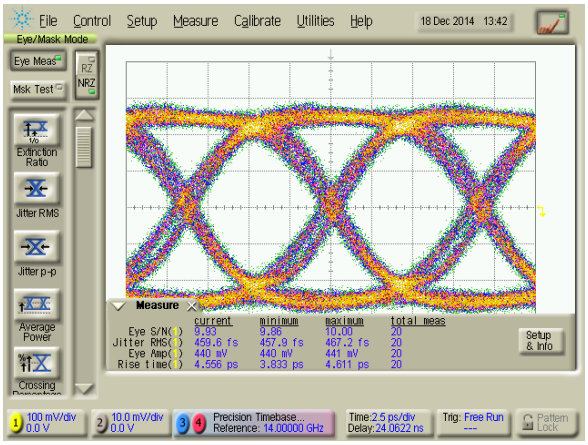
The measurements below had been performed using a SHF 12104 A Bit Pattern Generator (PRBS 2^{31}-1) and an Agilent Digital Communication Analyzer (DCA) with a Precision Timebase Module (86107A) and a 70 GHz Sampling Module (86118A). The outputs of the MUX module had been connected directly to the DCA input.



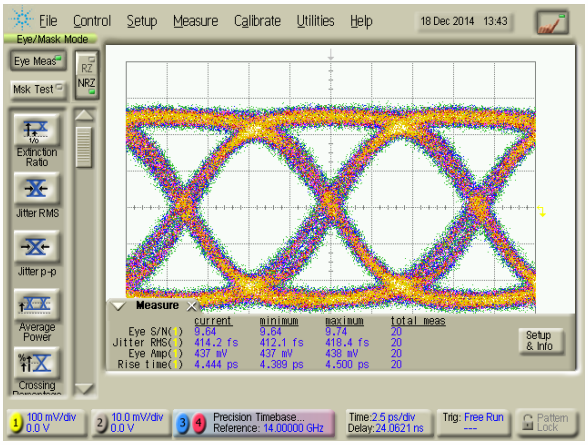
Out @ 120 Gbps



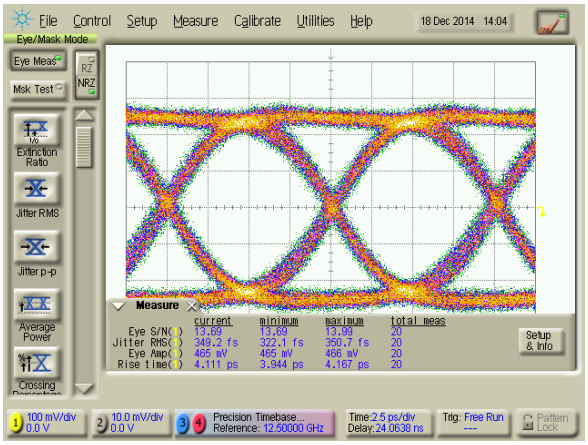
Out inv. @ 120 Gbps



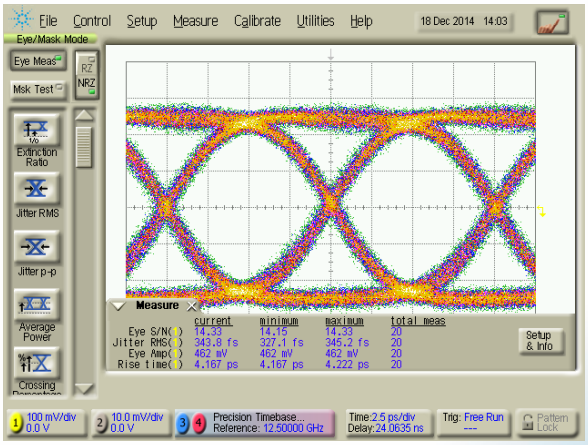
Out @ 112 Gbps



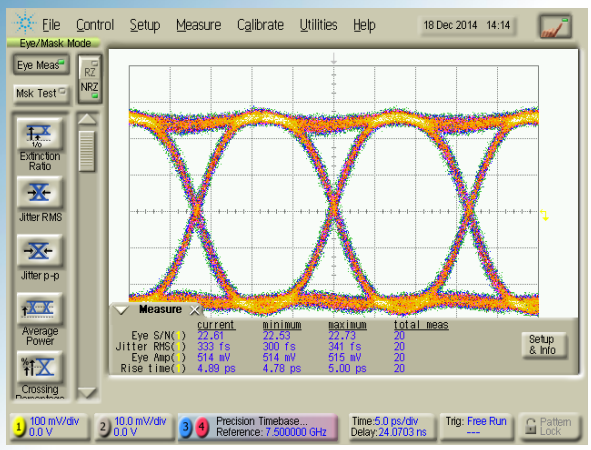
Out inv. @ 112 Gbps



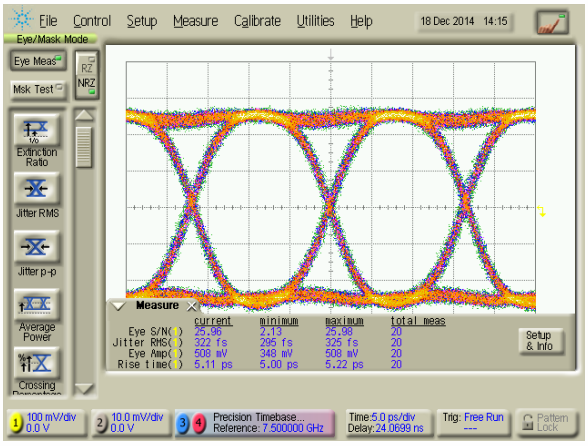
Out @ 100 Gbps



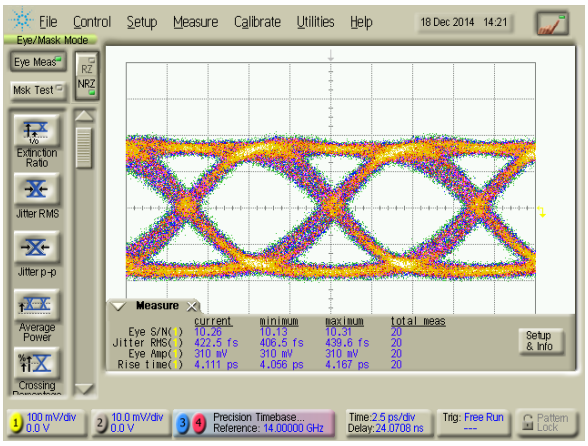
Out inv. @ 100 Gbps



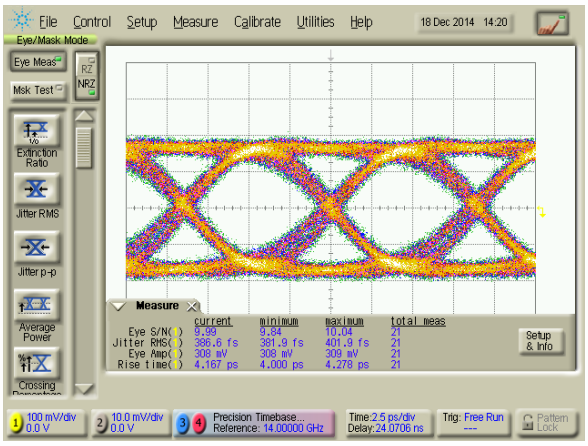
Out @ 60 Gbps



Out inv. @ 60 Gbps

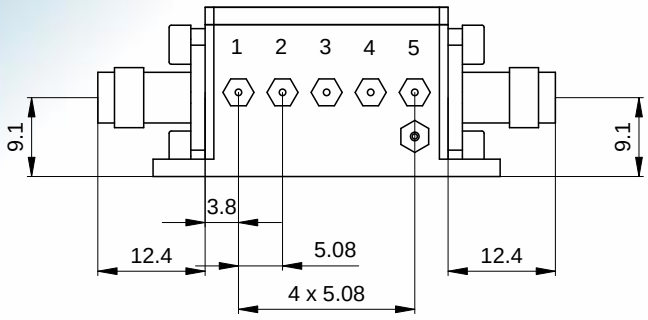


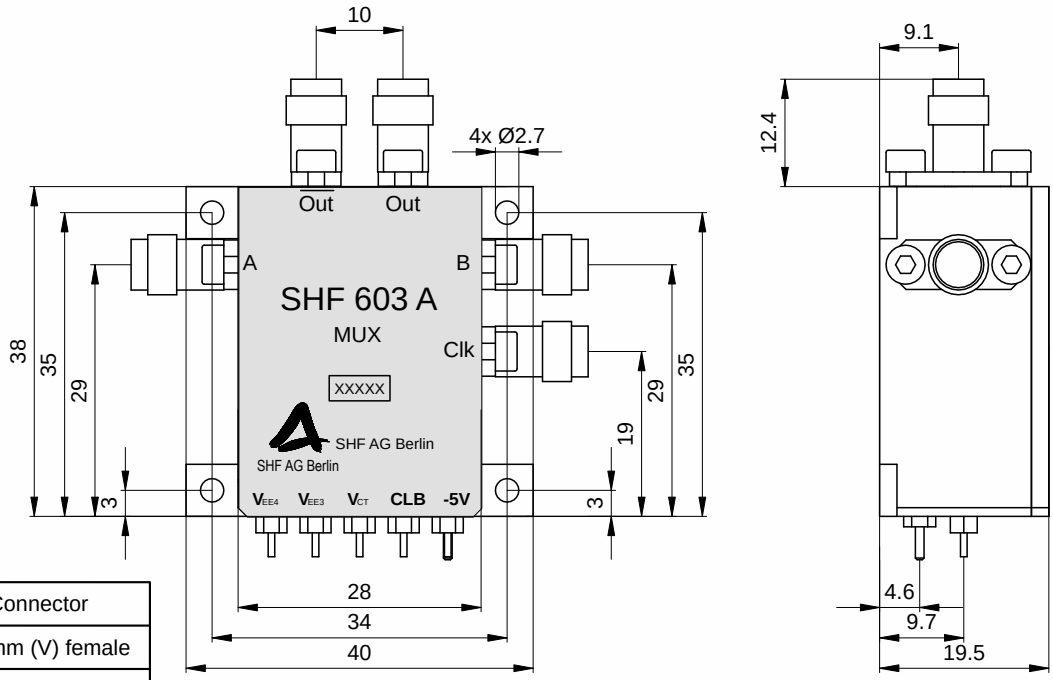
Out @ 112 Gbps, Level = -3dB



Out! @ 112 Gbps, Level = -3dB

Outline Drawing – Module



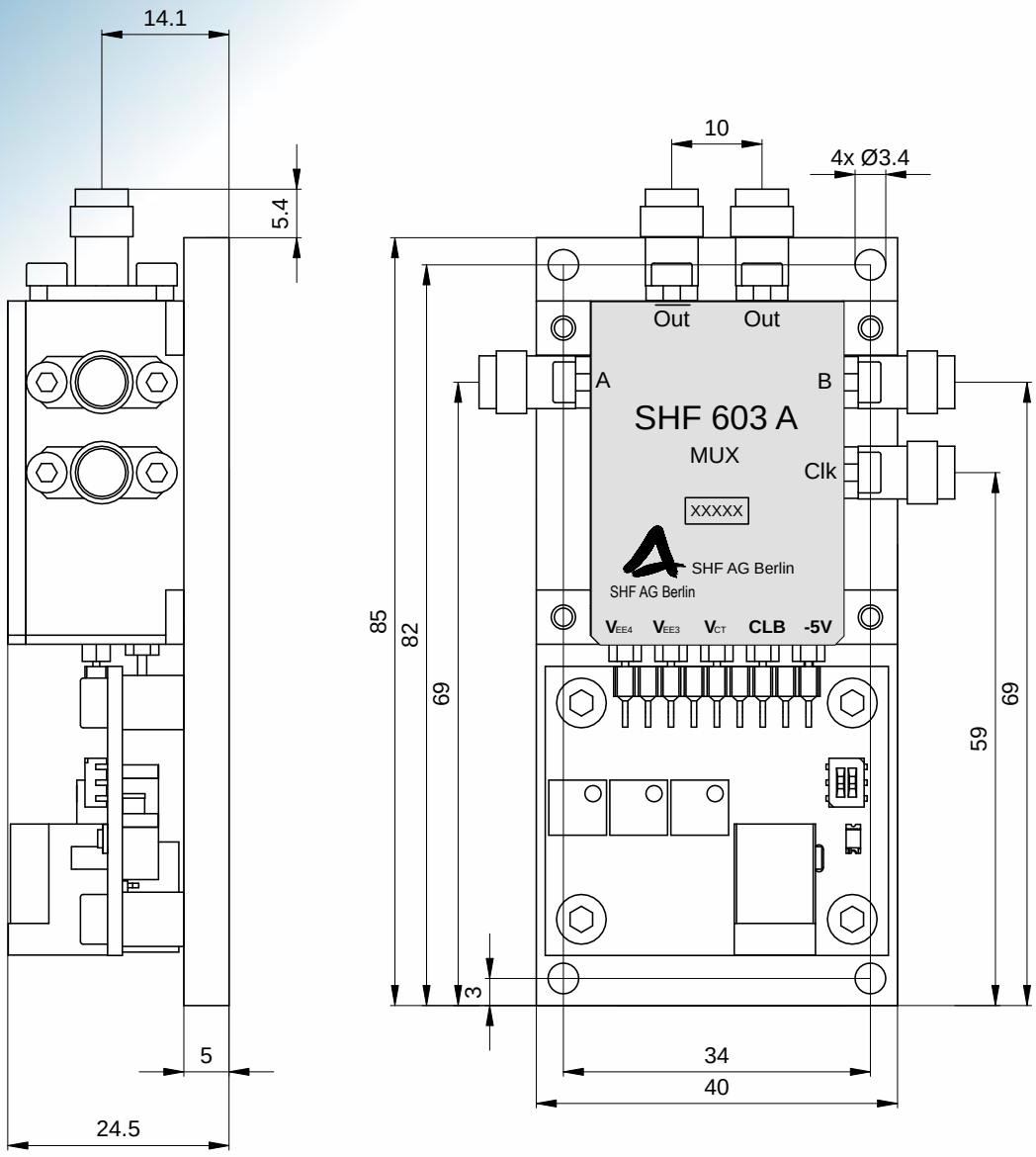


Port	Connector
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female

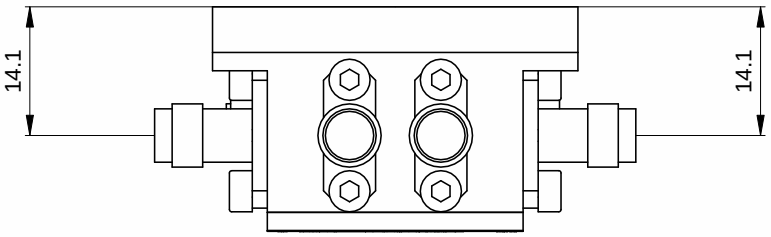
Pin	Designation
1	Level (V_{EE4})
2	Level (V_{EE3})
3	V_{CT}
4	Clock Bias (CLB)
5	-5V

All dimensions in mm

Outline Drawing – “Module + Bias Board”- Assembly

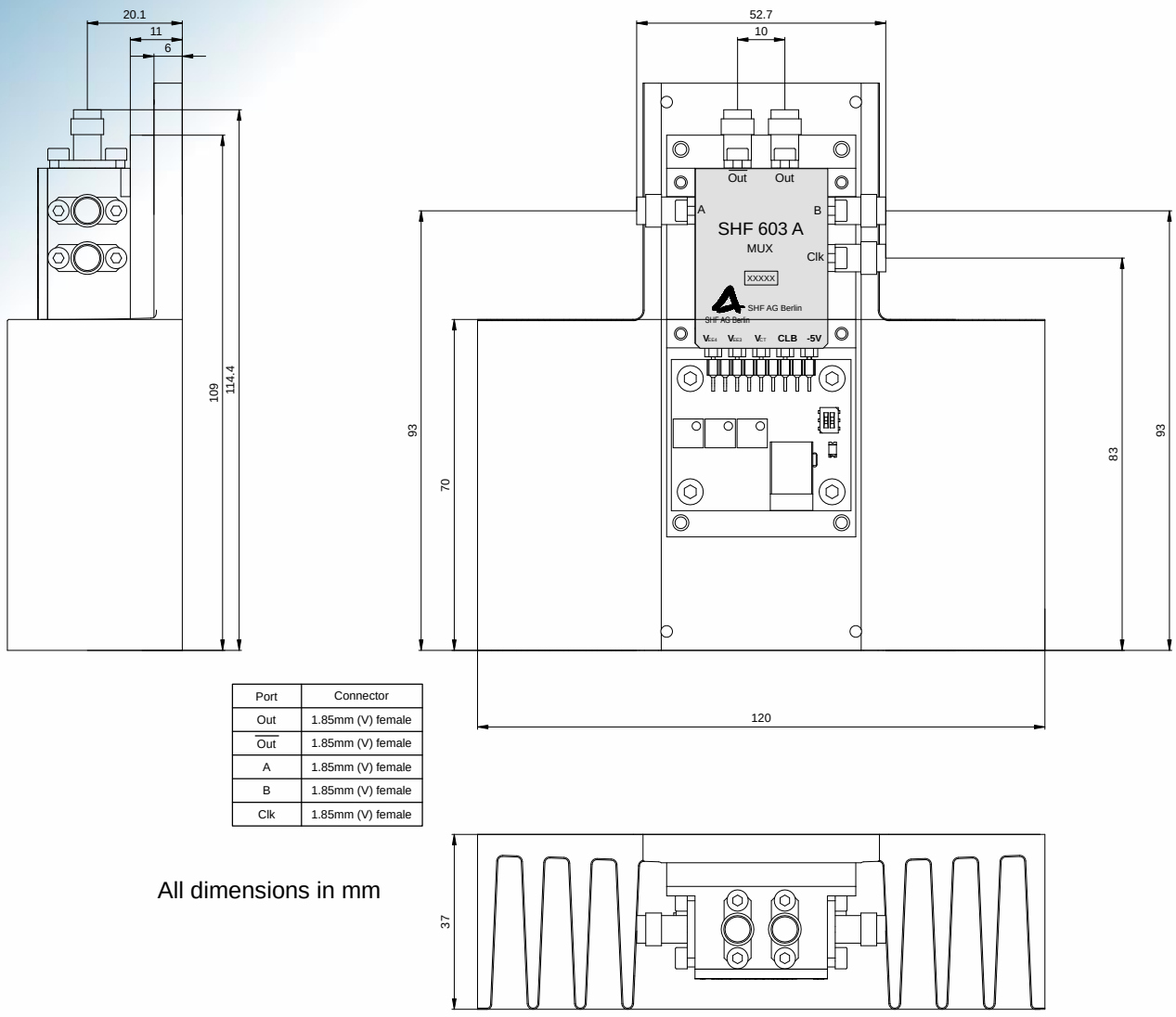


Port	Connector
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female



All dimensions in mm

Outline Drawing – “Module + Bias Board”- Assembly with Heat Sink



Port	Connector
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
A	1.85mm (V) female
B	1.85mm (V) female
Clk	1.85mm (V) female

All dimensions in mm