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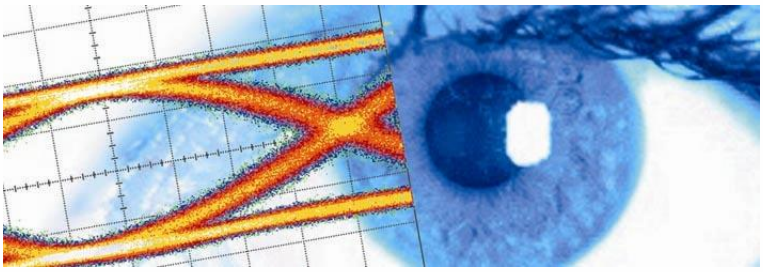
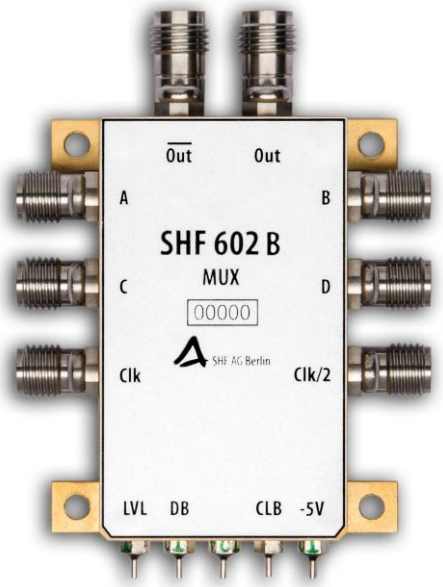


Datasheet

SHF 602 B

60 Gbps 4:1 Multiplexer



Description

The SHF 602 B is a 4:1 Multiplexer operating at data rates up to 60 Gbps for use in broadband test setups and telecom transmission systems. Four ≤15 Gbps single ended serial data streams are accepted by the multiplexer and converted into one differential data signal at an output data rate up to 60 Gbps. A single ended clock signal with a frequency half of the output data rate drives the SHF 602 B. All RF in- and output ports are AC-coupled. Unused in- or output ports should be terminated.

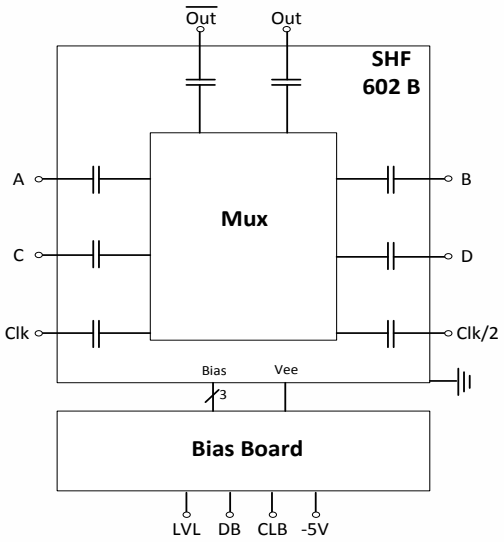
Features

- Broadband operation up to 60 Gbps
- Differential data output, 550 mV single ended output swing
- Single ended clock and data inputs
- Divide-by-2 clock output
- Output Level Control
- Bias Board

Applications

- 100G Ethernet development and prototyping
- 25G/28G CEI applications
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block Diagram



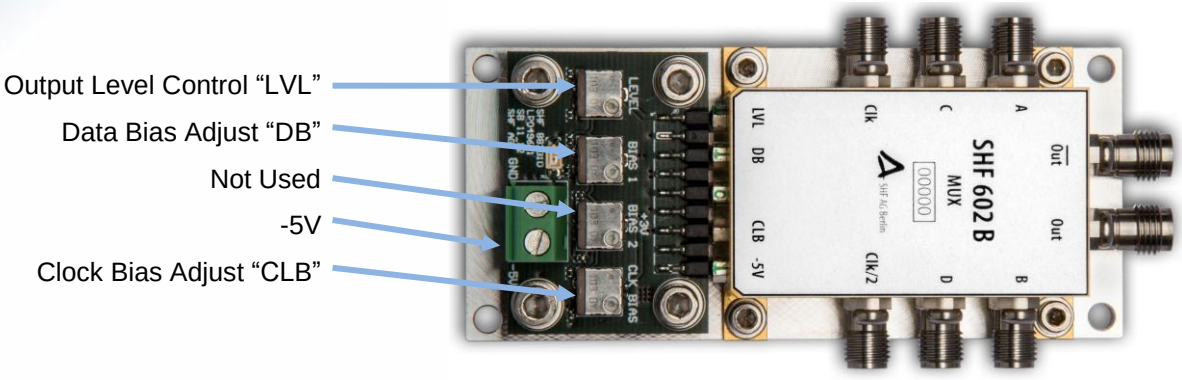
® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 602 B MUX. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level “LVL”, the input data bias voltage “DB” and the clock bias voltage “CLB” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



Specifications

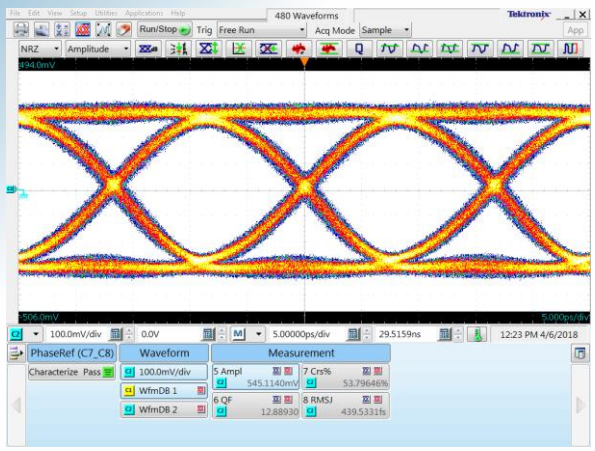
Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$	200		1000	
Clock Input Frequency	GHz	f_{in}	3		30	
Clock Input Voltage	mV_{pp}	$V_{clk\ in}$	300		1000	
Minimum Input Data Rate	Gbps	$R_{in,min}$		0.25[1]	1.5	
Maximum Input Data Rate	Gbps	$R_{in,max}$	15			
Output Parameters						
Minimum Output Data Rate	Gbps	$R_{out,min}$		1[1]	6	@ $500mV_{pp}$ clock input
Maximum Output Data Rate	Gbps	$R_{out,max}$	60			@ $500mV_{pp}$ clock input
Data Output Amplitude	mV	V_{out}	450	550	700	Single ended, adjustable up to -6dB
Rise / Fall time	ps	t_r/t_f		8	10	20% / 80%
Output Jitter, RMS value[2]	fs	J_{rms}		400	550	
Clock Output Frequency	GHz	f_{out}	1.5		15	
Clock Output Amplitude	mV	$V_{clk\ out}$	180	250	320	@ $500mV_{pp}$ clock input
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		720	750	
Power Dissipation	mW	P_d		3600		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Output Level Adjust	V	V_{LVL}	-3.3		0	if not used, connect to gnd
Input Data Bias	V	V_{DB}	-3.3	-1,65	0	common voltage for data inputs A,B,C and D
Clock Bias	V	V_{CLB}	-3.3	-1,65	0	
Conditions						
Case Temperature	°C	T_{case}		40	45	

[1] For operation below 6Gbps it is necessary to apply a clock input signal with a slew rate ≥3V/ns

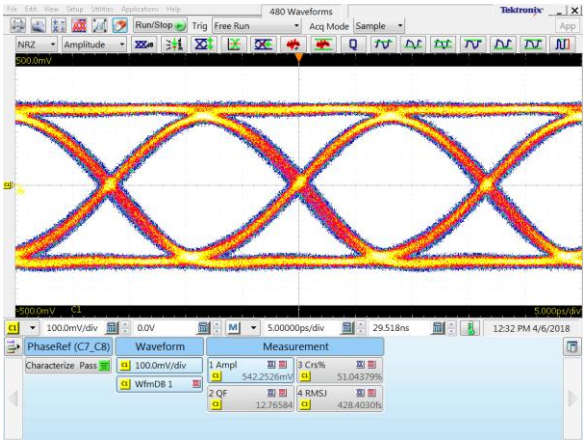
[2] Test condition: Clock Input Signal $Jitter_{RMS}$ = 230 fs

Typical Output Eye Diagrams

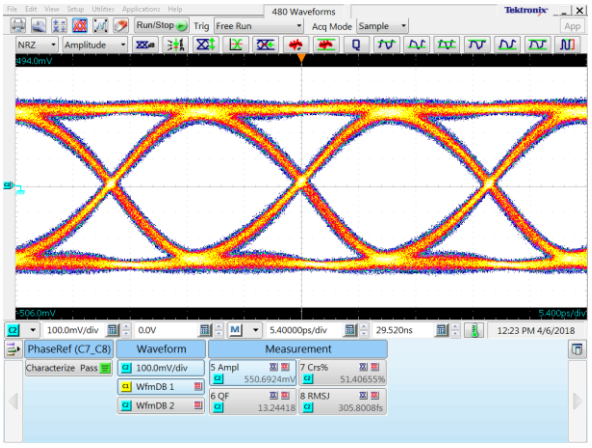
The measurements below had been performed using a SHF 12104 A BPG (PRBS 2^{31}-1), Tektronix 8300 DSA with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Head (80E11). The clock/2 outputs of the SHF 602 A MUX had been connected to the DCA inputs with a 6 dB Anritsu V-Attenuator.



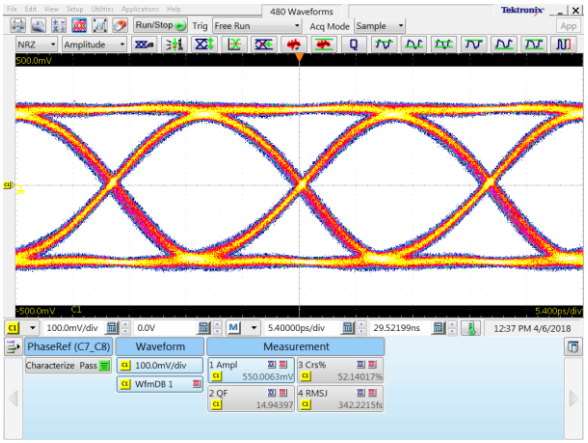
Out @ 60 Gbps



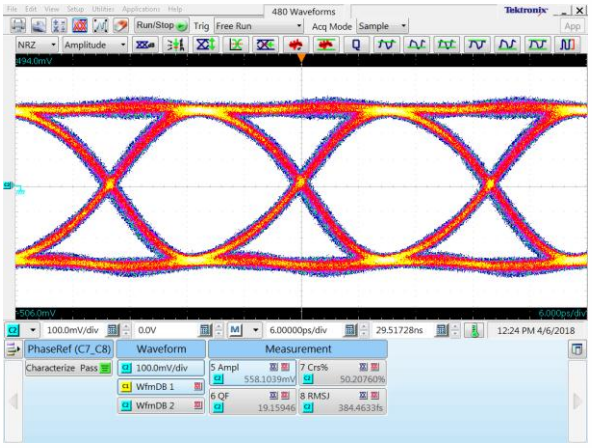
Out! @ 60 Gbps



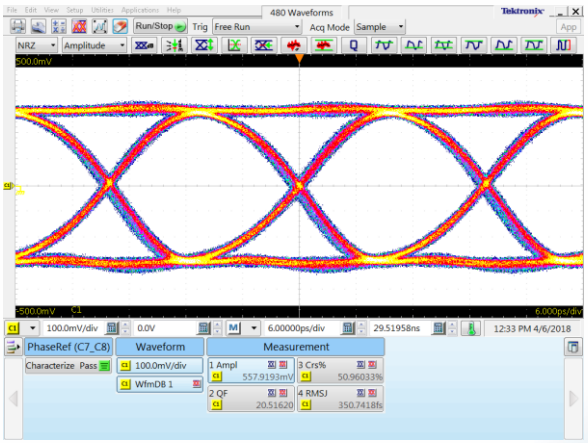
Out @ 56 Gbps



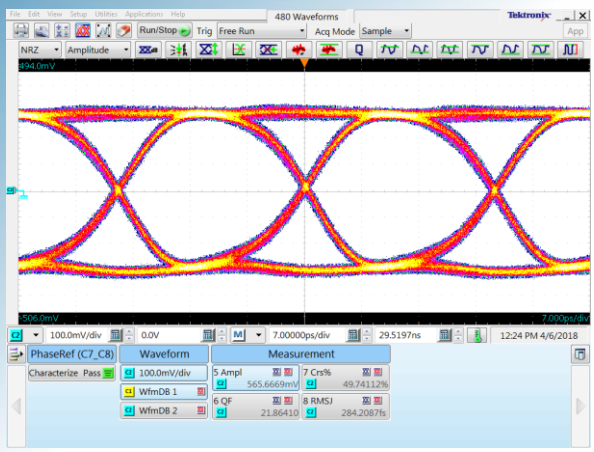
Out! @ 56 Gbps



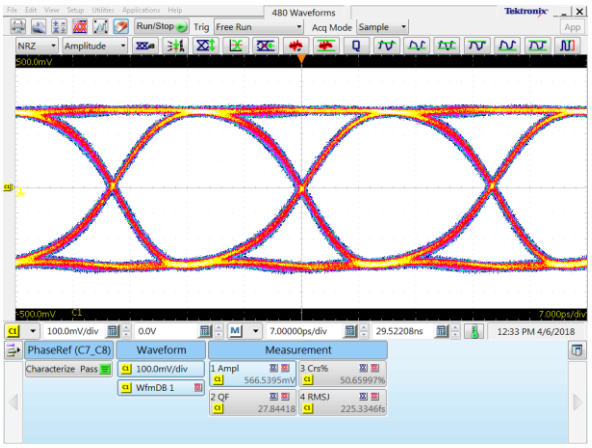
Out @ 50 Gbps



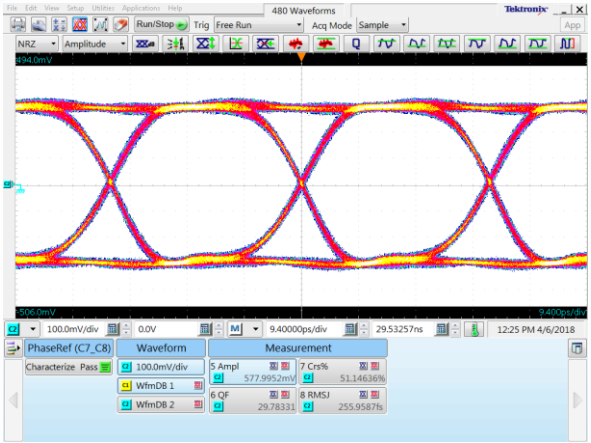
Out! @ 50 Gbps



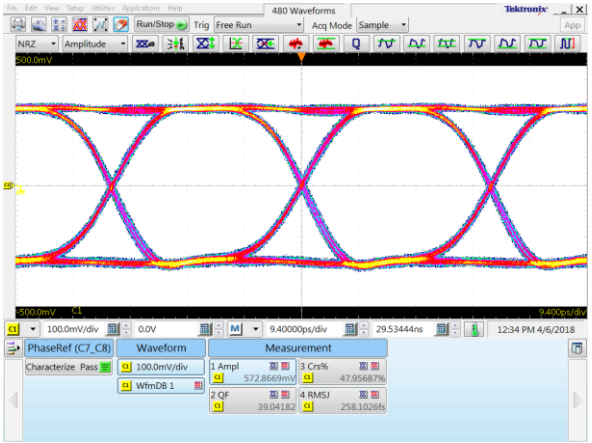
Out @ 43 Gbps



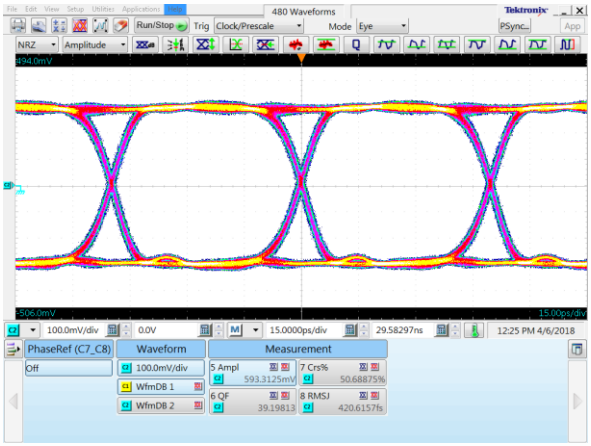
Out! @ 43 Gbps



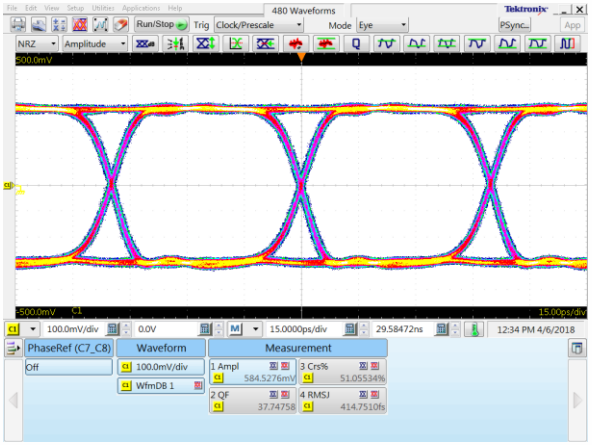
Out @ 32 Gbps



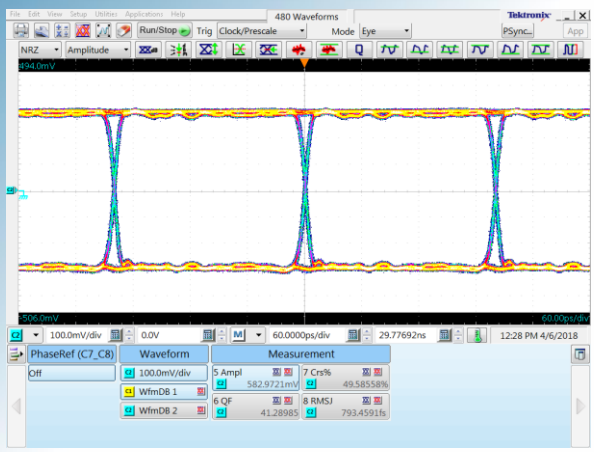
Out! @ 32 Gbps



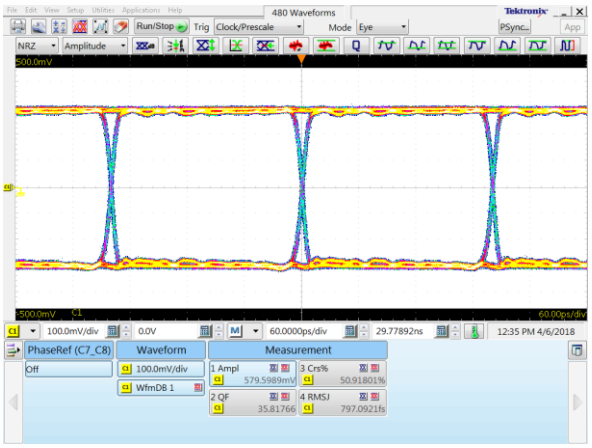
Out @ 20 Gbps



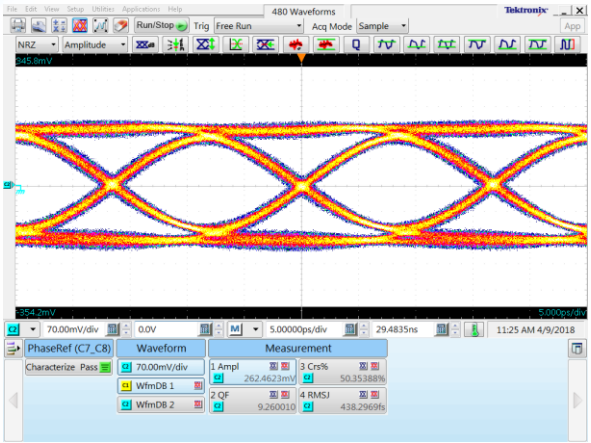
Out! @ 20 Gbps



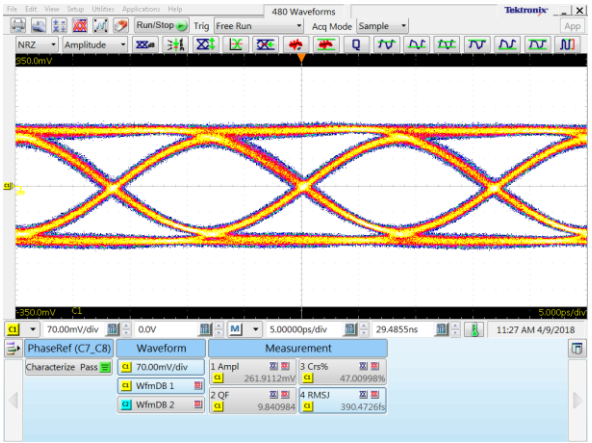
Out @ 5 Gbps



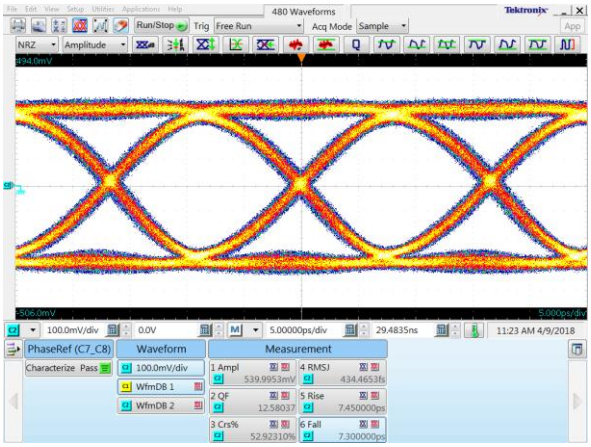
Out! @ 5 Gbps



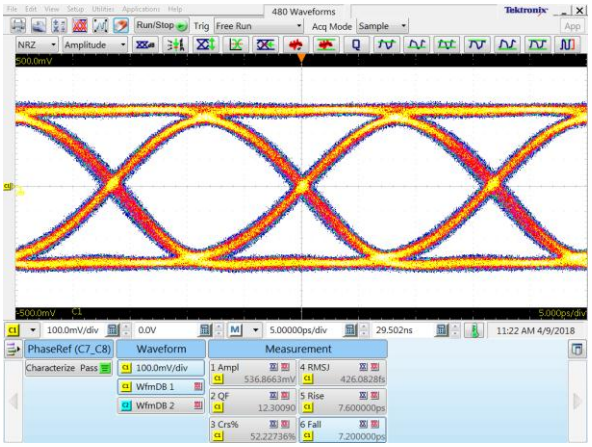
Out @ 60 Gbps, Level = -6dB



Out! @ 60 Gbps, Level = -6dB



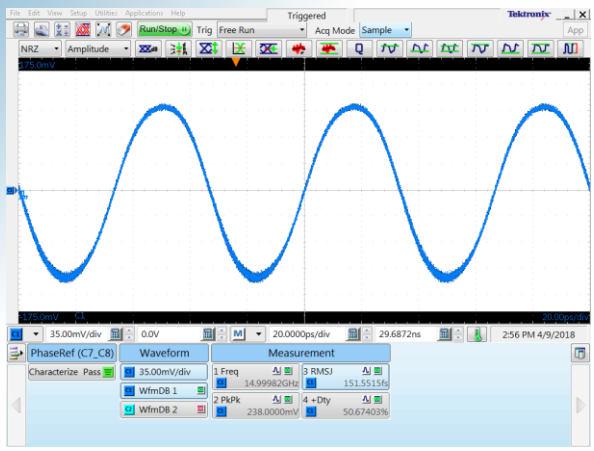
Out @ 60 Gbps, t_r/t_f



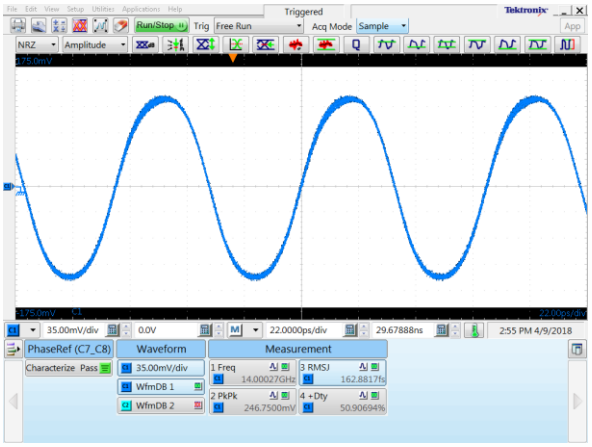
Out! @ 60 Gbps, t_r/t_f

Typical Clock/2 Output Signal Waveforms

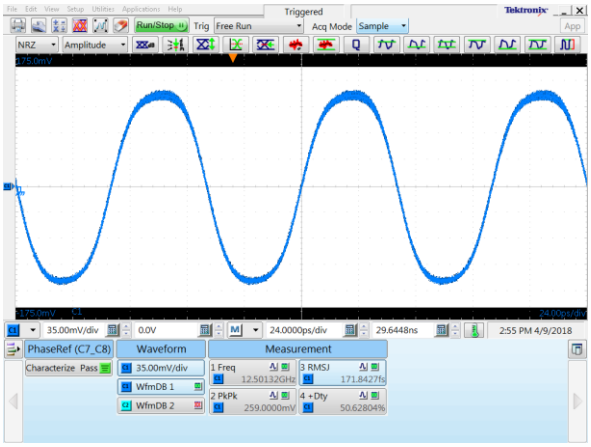
The measurements below had been performed using a Tektronix 8300 DSA with Phase Reference Module (82A04B-60G) and 70 GHz Sampling Head (80E11). The clock/2 output of the SHF 602 A MUX has been connected to the DCA input directly.



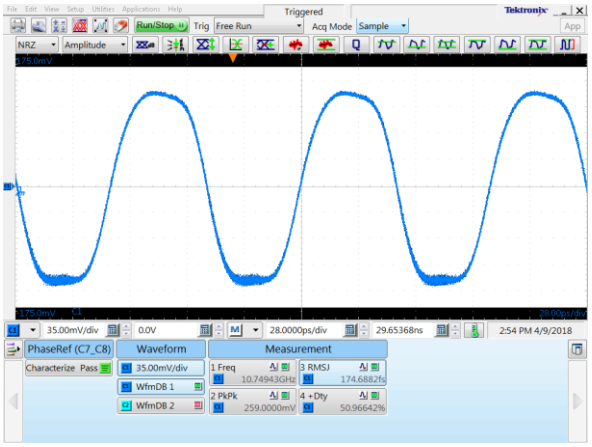
Clk/2 @ 15 GHz



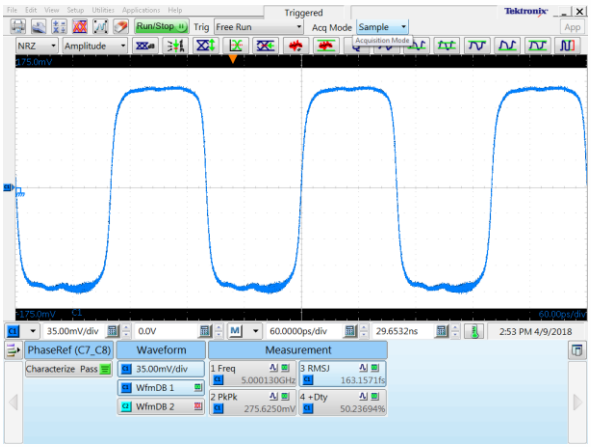
Clk/2 @ 14 GHz



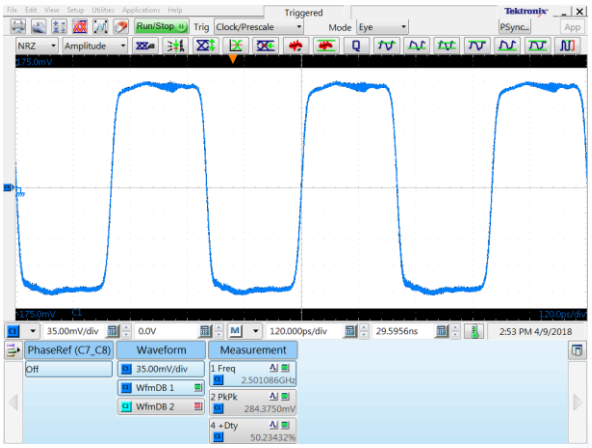
Clk/2 @ 12.5 GHz



Clk/2 @ 10.75 GHz

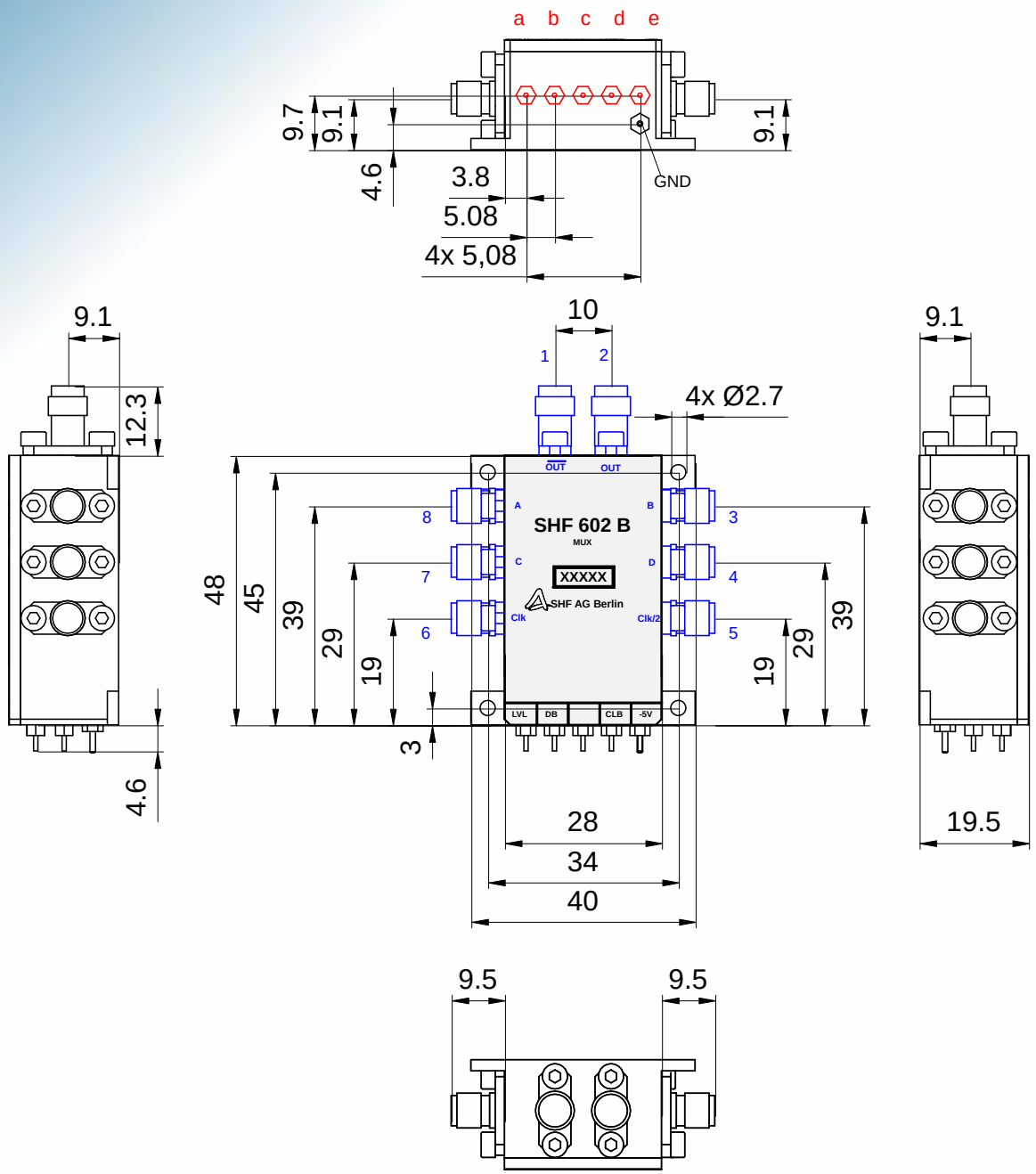


Clk/2 @ 5 GHz



Clk/2 @ 2.5 GHz

Outline Drawing

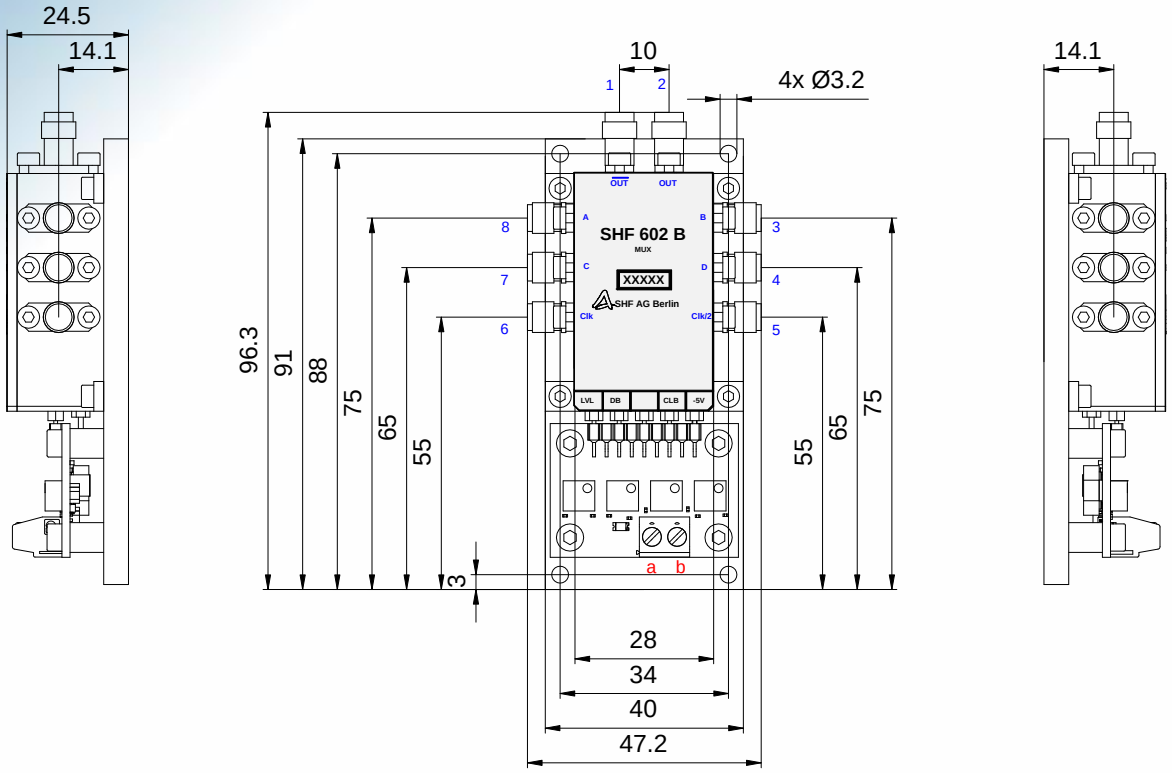


Port	a	b	c	d	e
Designation	LVL	DB		CLB	-5V

All dimensions are in mm.

Port	1	2	3	4	5	6	7	8
Designation	Out	$\overline{\text{Out}}$	B	D	Clk/2	Clk	C	A
Connector	1.85mm (V) Female		2.92mm (K) Female					

Outline Drawing – “Module + Bias Board”- Assembly

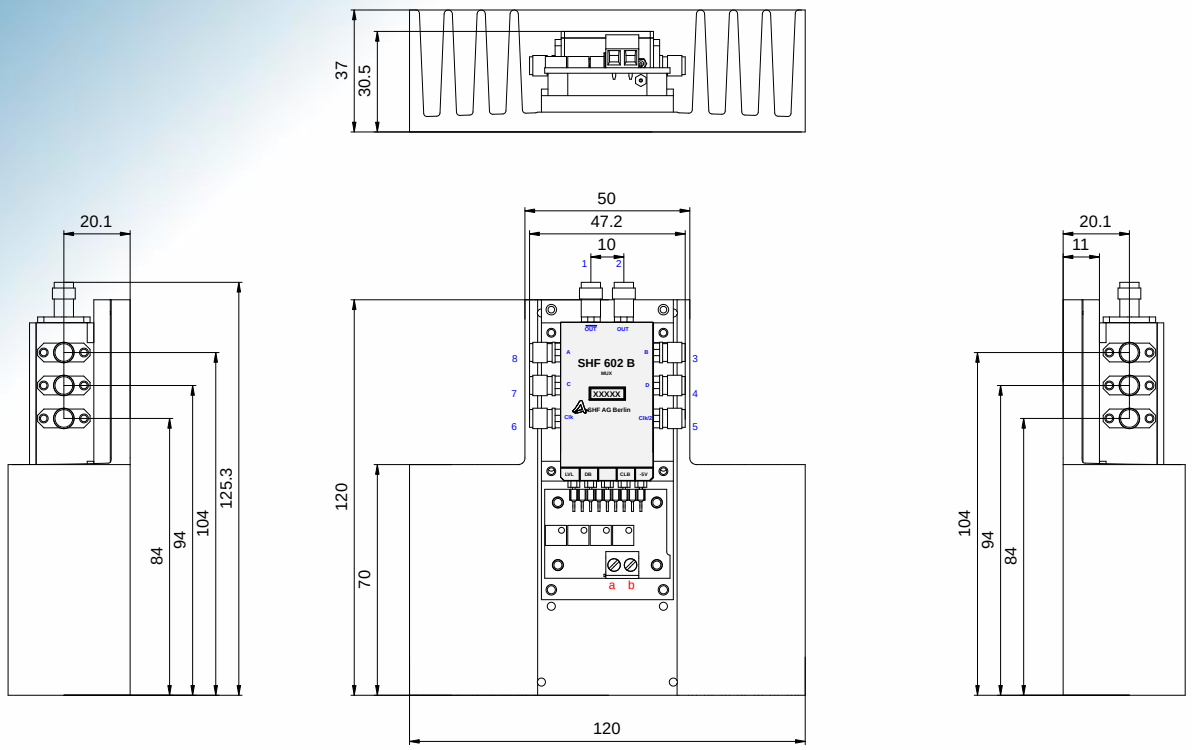


Port	a	b
Designation	GND	-5V

All dimensions are in mm.

Port	1	2	3	4	5	6	7	8
Designation	Out	$\overline{\text{Out}}$	B	D	Clk/2	Clk	C	A
Connector	1.85mm (V) Female		2.92mm (K) Female					

Outline Drawing – “Module + Bias Board”- Assembly with Heat Sink



Port	a	b
Designation	GND	-5V

All dimensions are in mm.

Port	1	2	3	4	5	6	7	8
Designation	Out	$\overline{\text{Out}}$	B	D	Clk/2	Clk	C	A
Connector	1.85mm (V) Female		2.92mm (K) Female					