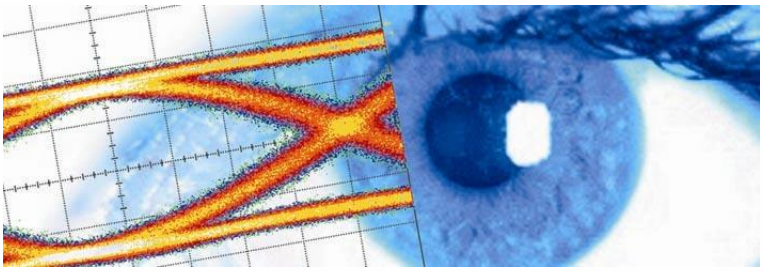
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany

Phone +49 30 772051-0 • Fax +49 30 7531078

E-Mail: sales@shf.de • Web: http://www.shf.de

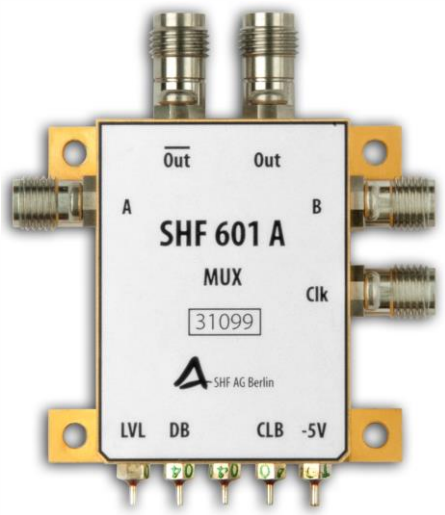


Datasheet

SHF 601 A

60 Gbps

2:1 Multiplexer



Description

The SHF 601 A is a 2:1 Multiplexer operating at data rates up to 60 Gbps for use in broadband test setups and telecom transmission systems. Two 30 Gbps single ended serial data streams are accepted by the multiplexer and converted into one differential data signal at a nominal output data rate of 60 Gbps. A single ended clock signal (nominally 30 GHz) with a frequency half of the output data rate drives the SHF 601 A. All RF in- and output ports are AC-coupled. Unused in- or output ports should be terminated.

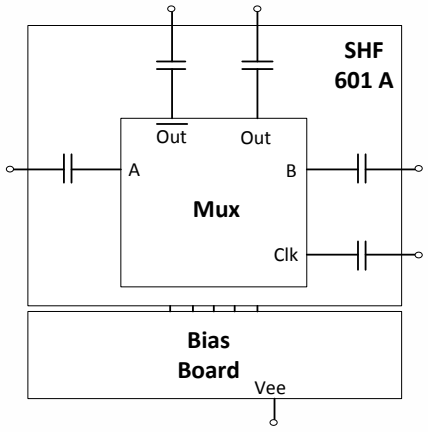
Features

- Broadband operation up to 60 Gbps
- Differential data output, 650mV single ended output swing
- Single ended clock and data inputs
- Output Level Control
- Bias Board

Applications

- 100G Ethernet development and prototyping
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel®
- Broadband test and measurement equipment

Block Diagram

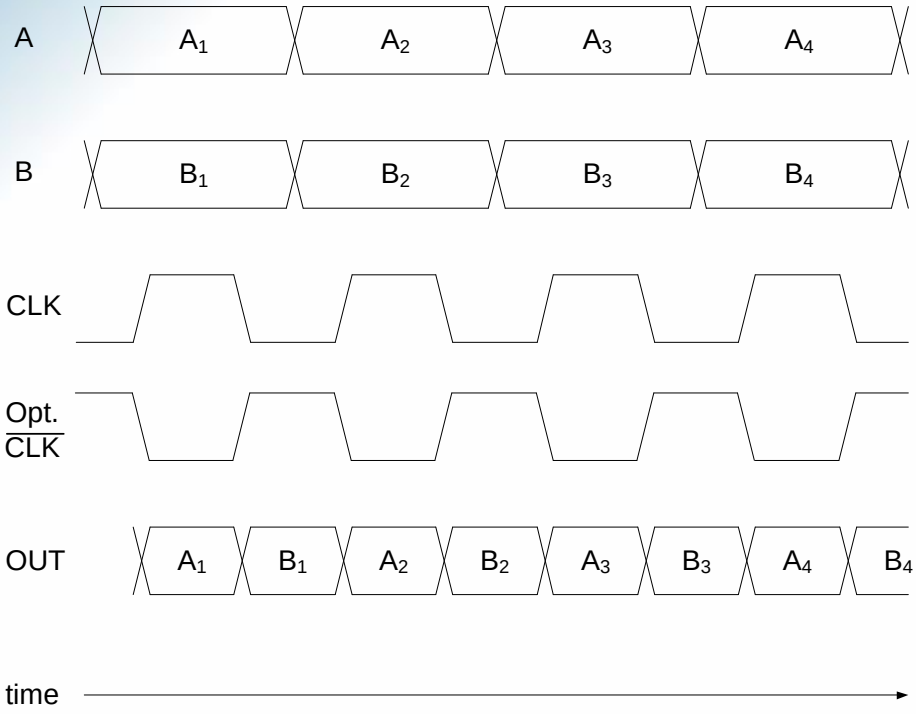


Options

- Option Inverted Clock – Phase of the clock input port is shifted by 180°

® Fibre Channel is a registered trademark of the Fibre Channel Industry Association

Timing Diagram

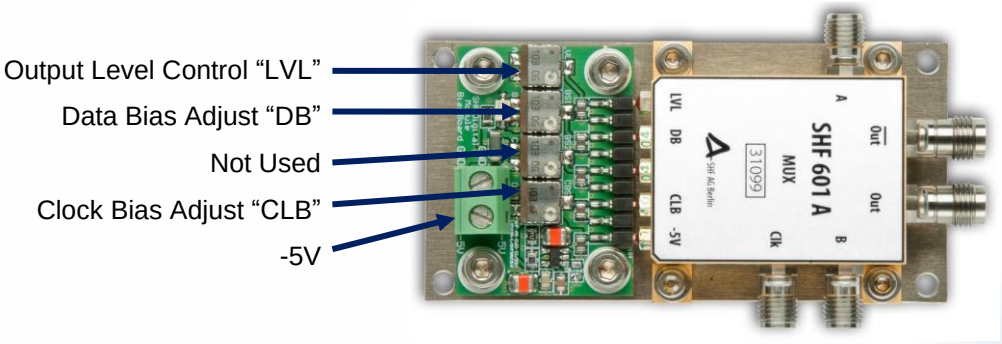


Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 601 A MUX. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level “LVL”, the input data bias voltage “DB” and the clock bias voltage “CLB” with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer’s circuitry.



Absolute Maximum Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	mV	$V_{data\ in}$			900	Peak-to-Peak
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on RF Input Ports	V	V_{DCin}	-10		+10	AC coupled inputs
External DC Voltage on RF Output Ports	V	V_{DCout}	-10		+10	AC coupled outputs
DC Supply Voltage	V	V_{ee}	-5.5		0	

Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Minimum Input Data Rate	Gbps	$R_{in,min}$			1	
Maximum Input Data Rate	Gbps	$R_{in,max}$	30			
Data Input Voltage	mV	$V_{data\ in}$	200		800	Eye Amplitude; 500 mV recommended;
External DC Voltage on RF Data Input Ports	V	V_{DCin}	-9		+9	AC coupled inputs
Min. Clock Input Frequency	GHz	$f_{in,min}$			1[1]	
Max. Clock Input Frequency	GHz	$f_{in,max}$	30			
Clock Input Voltage	mV_{pp}	$V_{clk\ in}$	300		800	Peak-to-Peak; 500 mV recommended
External DC Voltage on RF Clock Input Port	V	V_{DCin}	-9		+9	AC coupled input

[1] For clock input frequencies between 1…3 GHz a clock input signal slew rate of ~10 V/ns is required

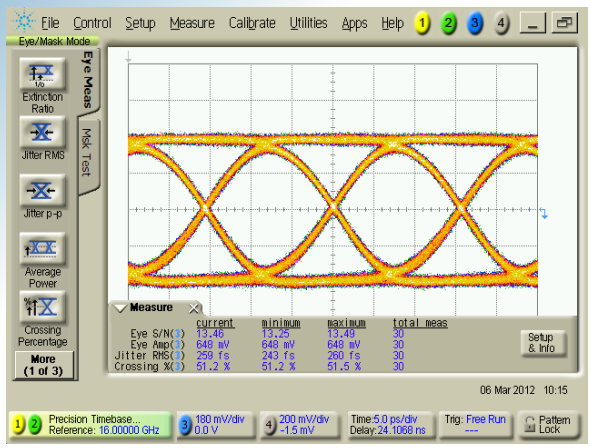
Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Output Parameters						
Minimum Output Data Rate	Gbps	$R_{in,min}$		1	2[2]	@ 500mV$_{pp}$ clock input
Maximum Output Data Rate	Gbps	$R_{in,max}$	60	64		@ 500mV$_{pp}$ clock input
Output Voltage	mV	V_{out}	550	630	800	Eye Amplitude; Single ended; Adjustable up to -3dB
Rise / Fall time	ps	t_r/t_f		8	10	20%...80%
Output Jitter, RMS value[3]	fs	J_{rms}		350	500	
Power Requirements						
Supply Voltage	V	V_{ee}	-5.2	-5	-4.8	
Supply Current	mA	I_{ee}		430	460	
Power Dissipation	mW	P_d		2150		@ V_{EE} = -5V; incl. Bias Board
Bias Voltages						
Output Level Adjust	V	LVL	-3.3		0	if not used, connect to gnd
Input Data Bias	V	DB	-3.3	-1,65	0	
Clock Bias	V	CLB	-3.3	-1,65	0	
Conditions						
Operating Temperature	°C	$T_{ambient}$	15		35	

[2] For output data rates between 2…6 Gbps a clock input signal slew rate of ~10 V/ns is required

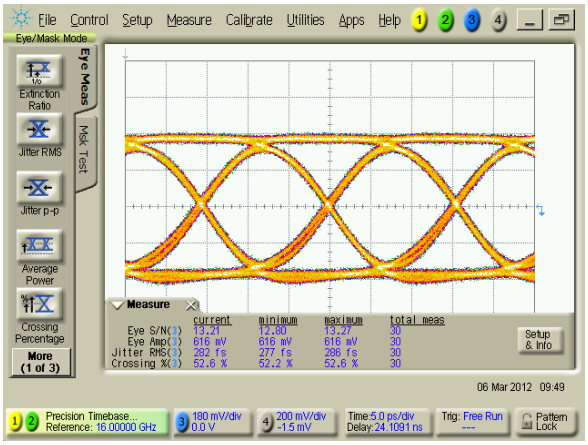
[3] Test condition: Input Signal Jitter$_{RMS}$ = 230 fs

Typical Output Eye Diagrams

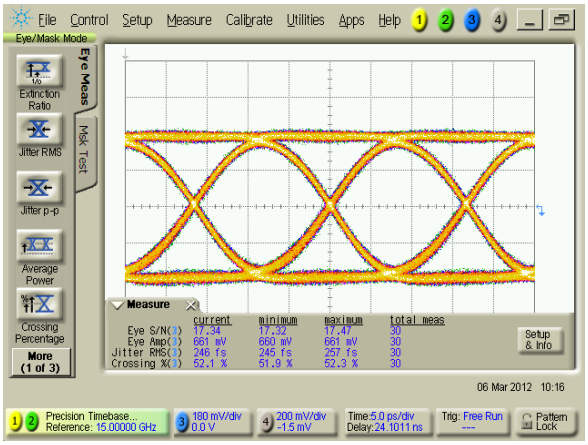
The measurements below had been performed using a SHF 12103 A BPG (PRBS 2^{31}-1) and an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the multiplexer module had been connected directly to the DCA input.



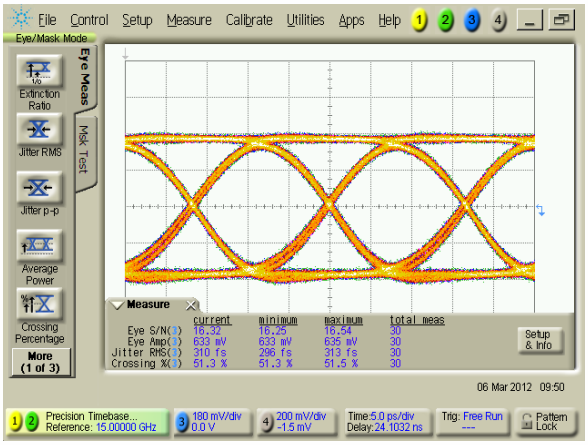
Out @ 64 Gbps



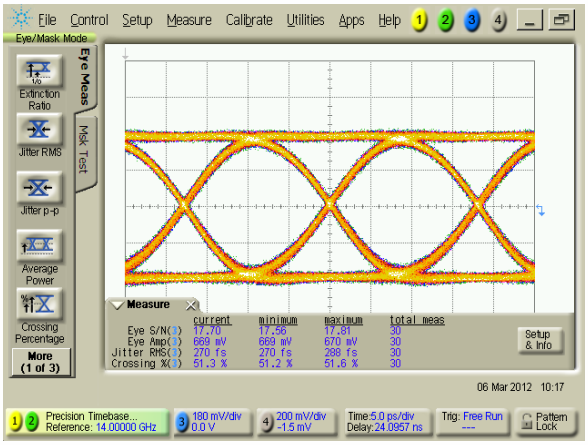
Out inv. @ 64 Gbps



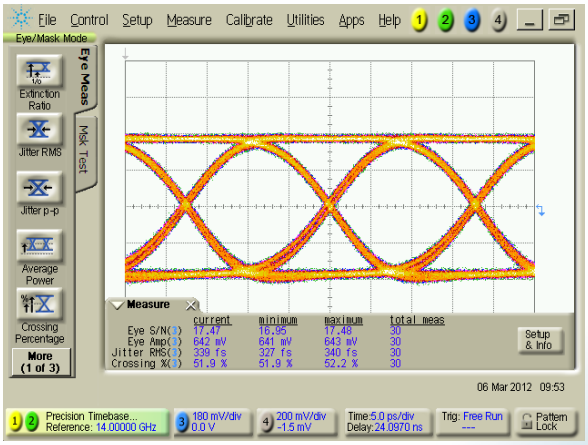
Out @ 60 Gbps



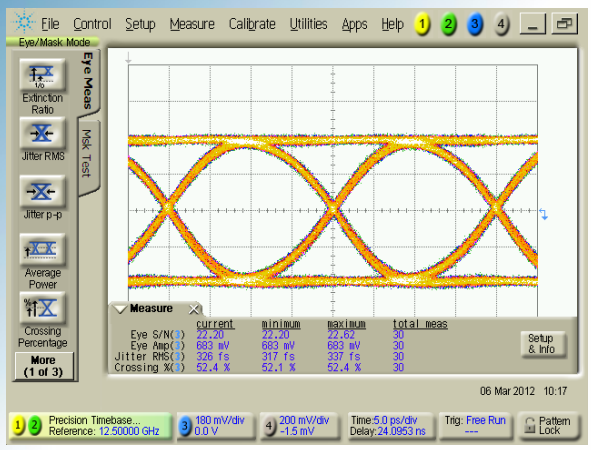
Out inv. @ 60 Gbps



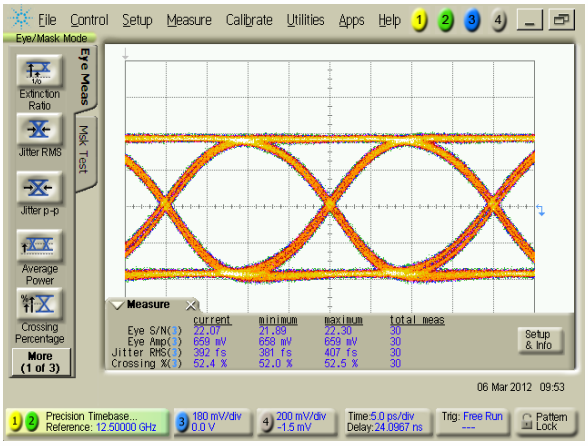
Out @ 56 Gbps



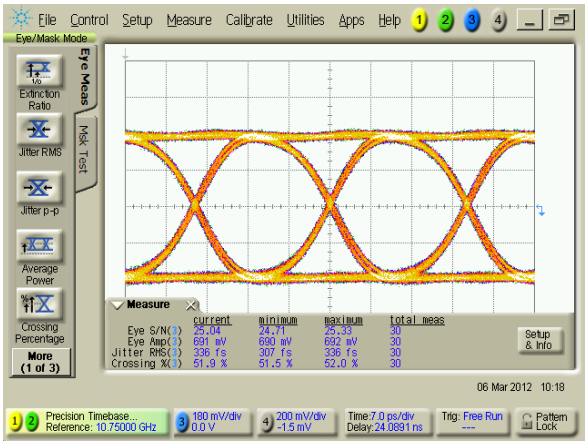
Out inv. @ 56 Gbps



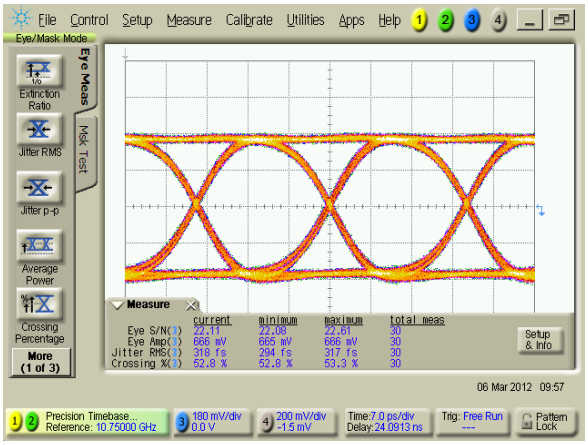
Out @ 50 Gbps



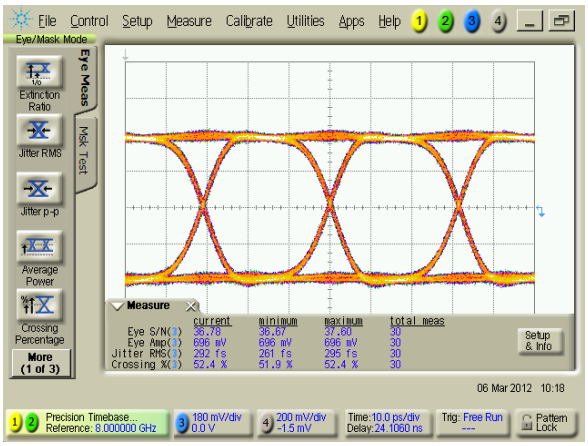
Out inv. @ 50 Gbps



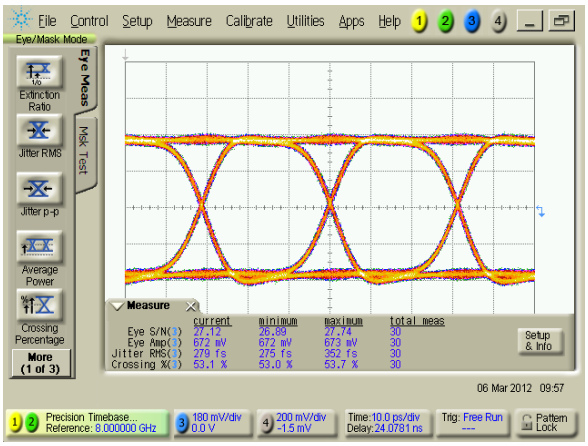
Out @ 43 Gbps



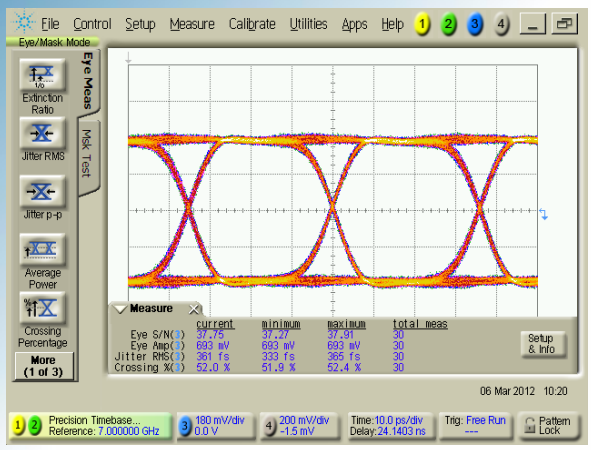
Out inv. @ 43 Gbps



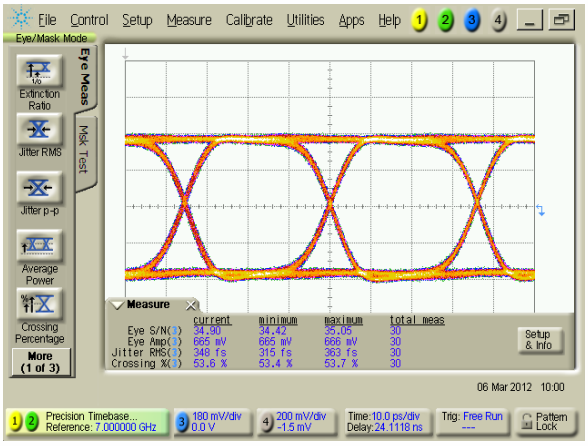
Out @ 32 Gbps



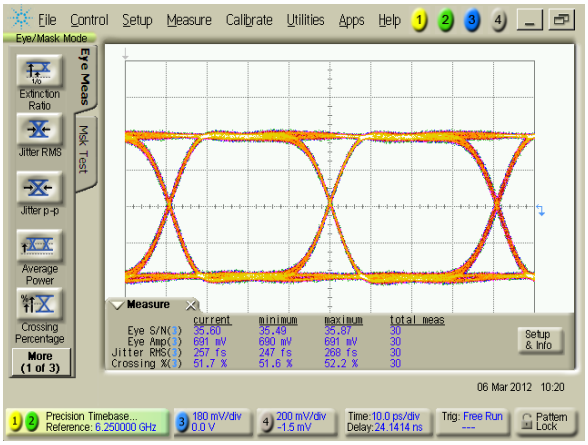
Out inv. @ 32 Gbps



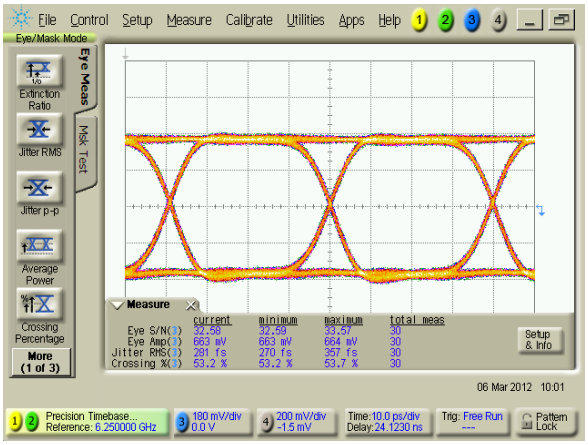
Out @ 28 Gbps



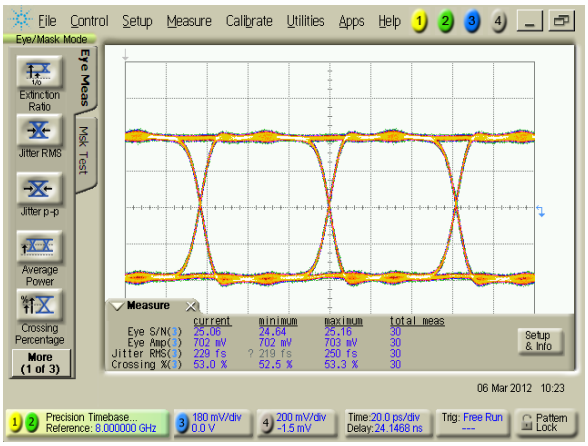
Out inv. @ 28 Gbps



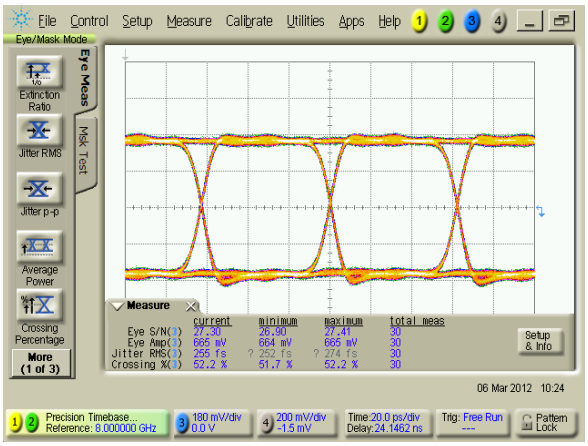
Out @ 25 Gbps



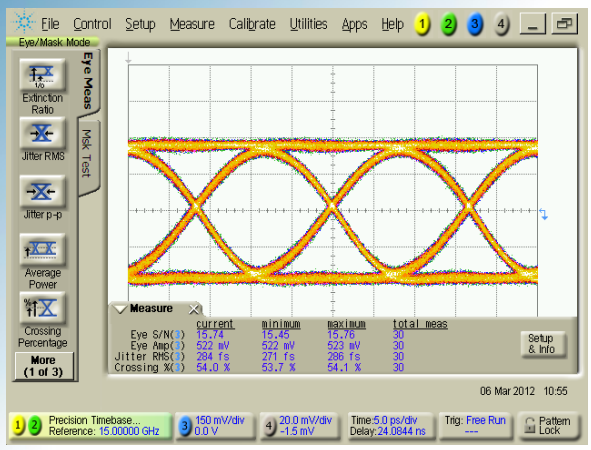
Out inv. @ 25 Gbps



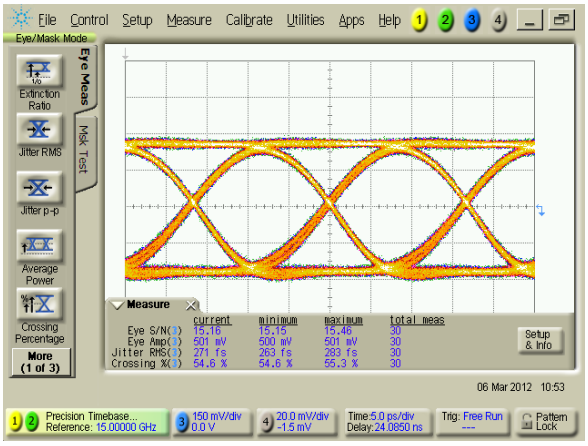
Out @ 16 Gbps



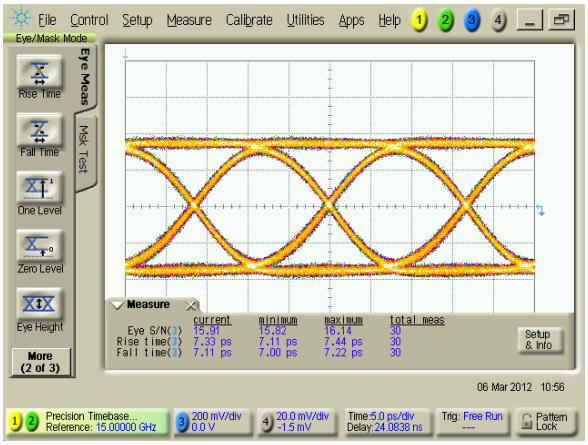
Out inv. @ 16 Gbps



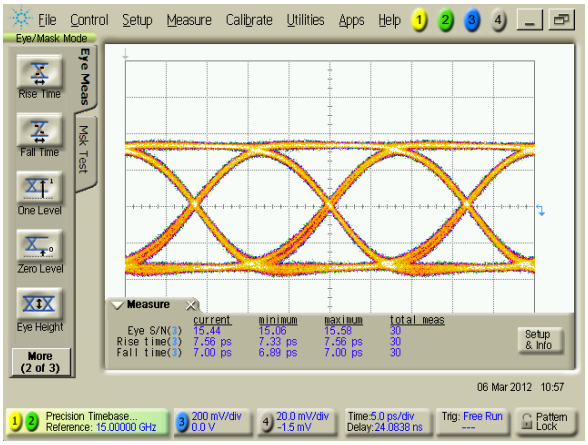
Out @ 60 Gbps, Level = -3dB



Out! @ 60 Gbps, Level = -3dB

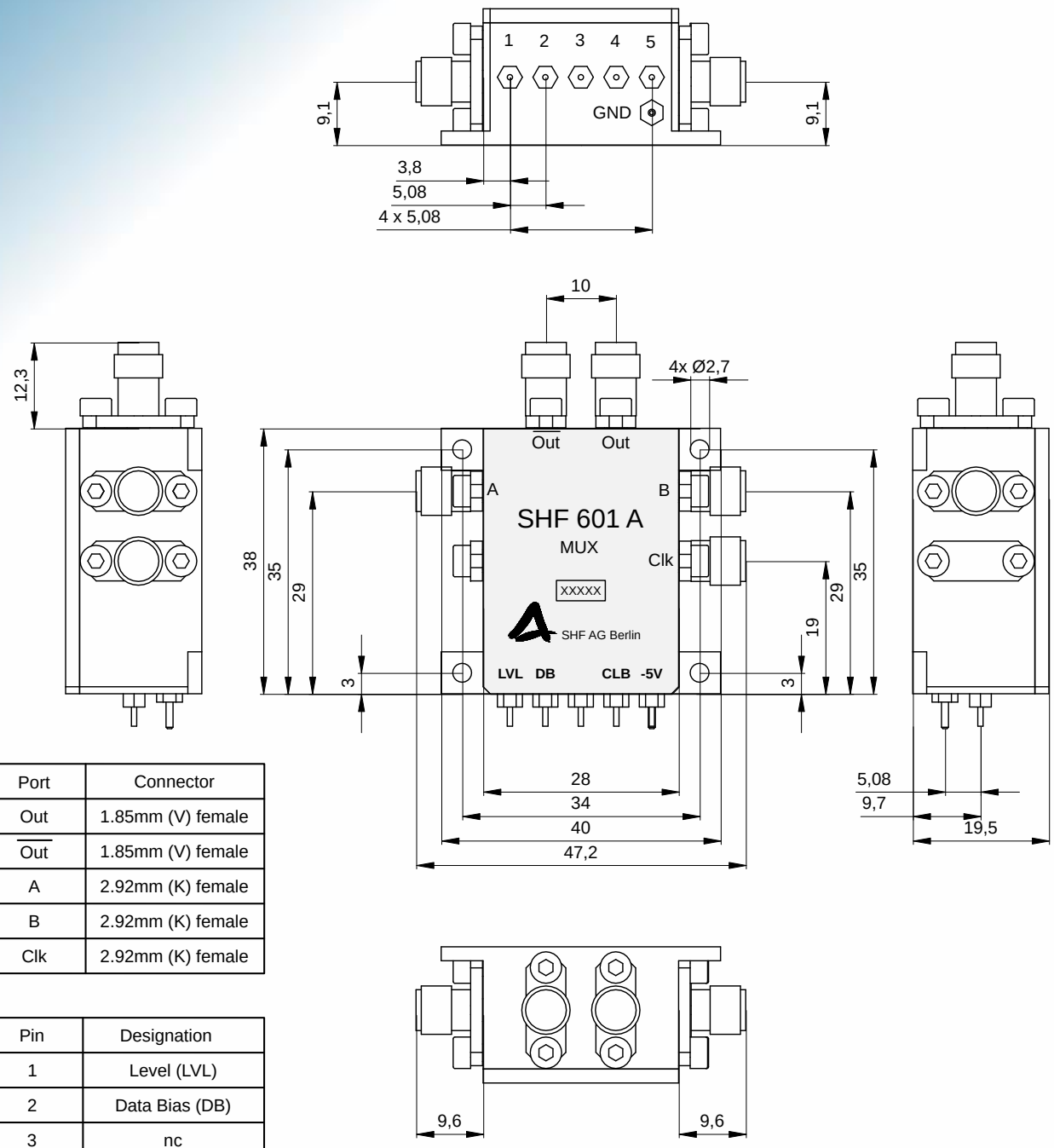


Out @ 60 Gbps, t_r/t_f



Out! @ 60 Gbps, t_r/t_f

Outline Drawing



Port	Connector
Out	1.85mm (V) female
$\overline{\text{Out}}$	1.85mm (V) female
A	2.92mm (K) female
B	2.92mm (K) female
Clk	2.92mm (K) female

Pin	Designation
1	Level (LVL)
2	Data Bias (DB)
3	nc
4	Clock Bias (CLB)
5	-5V

All dimensions in mm.