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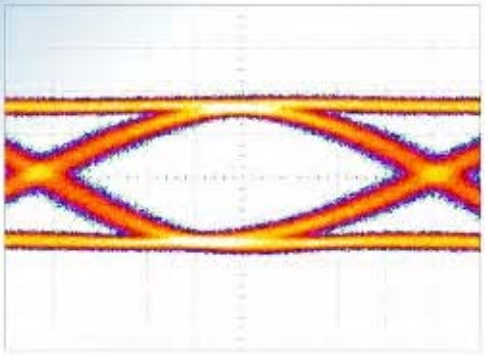


Datasheet

SHF 5002 A

60 Gbps 1:4 Demultiplexer

Description

The SHF 5002 A demultiplexer extracts four output data streams from a 60 GBit/s input signal at a rate of a quarter of the input signal data rate.

All features of the demultiplexer are controlled by push button using a menu system on the front panel. The half clock (1/4 Bit rate) output allows perfect sychronization of a 15 GBit/s error analyzer to the individual four output signals.

A high output signal level of over 2.5 V_{amp} allows resistive splitting, leaving enough signal to drive multiple digital circuits. Very high sensitivity and a clock phase margin of more than 200° make this instrument suitable for measurements of the highest precision.

The SHF 5002 A demultiplexer is a result of SHFs many years experience in the development and production of ultra high speed components and their assembly to more complex systems.

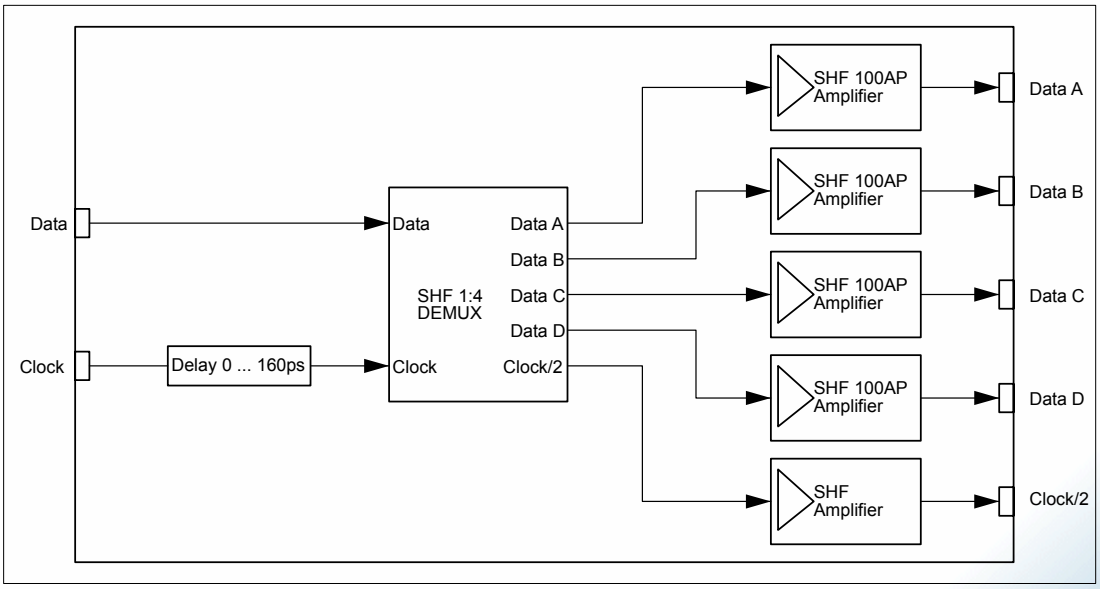
Features

- High amplitude data output @ 15 GBit/s
- Ruggedized 1.85 mm male input connectors for data input
- External master clock input at half of the bitrate
- Clock output at half the input frequency
- High precision computer controlled delay line to adjust the clock phase
- External GPIB control
- Very high sensitivity
- Large angle clock phase margin
- Wide band operation up to more than 60 GBit/s
- High amplitude data output @ 15 GBit/s

Option

- Option DS: Internal 4:1 data selector – allows each output signal to be selected and sent to a single output.

Functional Block Diagram



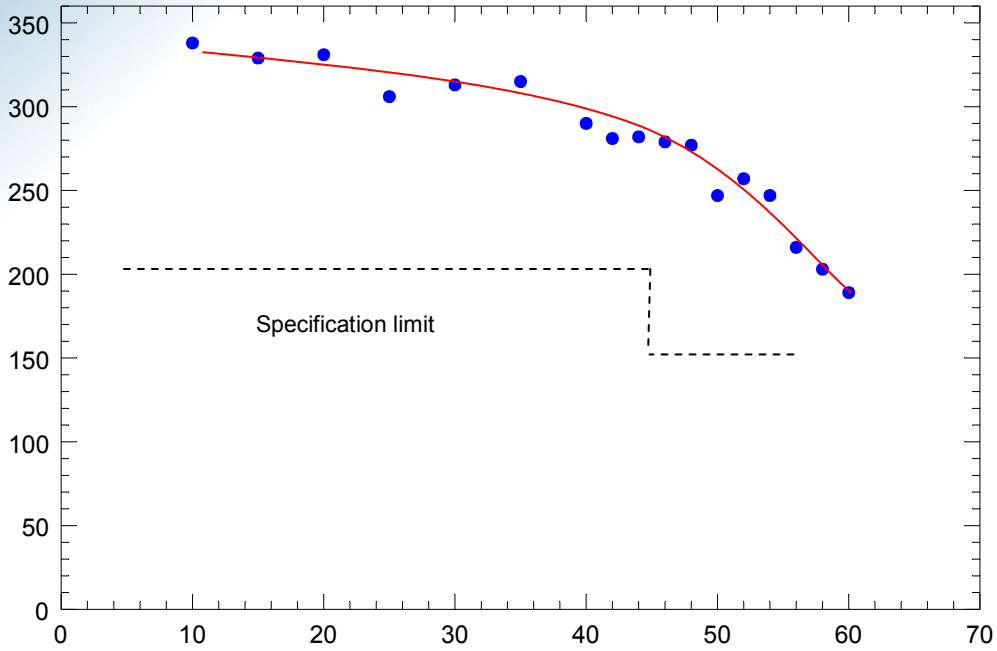
Specifications

Parameter	Unit	Min.	Typ.	Max.	Conditions
Clock input [1]					AC coupled
Frequency range	GHz	1		30	half bit rate
S11	dB			-10	
Input level	V_{pp}	0.4		0.8	
Clock delay range	ps	0		160	in 1ps steps
Max. AC input	V_{pp} (dBm)			1 (4)	
Data inputs [2]					AC coupled
Bit rate	Gbps	2		60	<0.1 V_{pp}
S11	dB			-10	
Sensitivity	mV			60 100	<50 Gbps <60 Gbps
Clock phase margin	°	200 150			<50 Gbps <60 Gbps see page 4
Max. AC input	V_{pp}			1	
Max. DC input	V_{pp} (dBm)			1 (4)	
Clock output [1]					AC coupled
Output level	V_{pp}	0.4		0.8	
S22	dB			-10	
Electrical data outputs [3]					AC coupled
Frequency range	GHz	0.5		15	
Output level	V_{amp}	1.5	2	2.5	
Rise/fall time	ps			30	20%...80%
Power supply	V	90 180	110 230	135 270	47…63 Hz
Power consumption	W		100		
Weight	kg		15		
Dimensions (WxHxD)	mm				472x110x365
Operating temperature	°C	10		35	
Storage temperature	°C	-20		70	

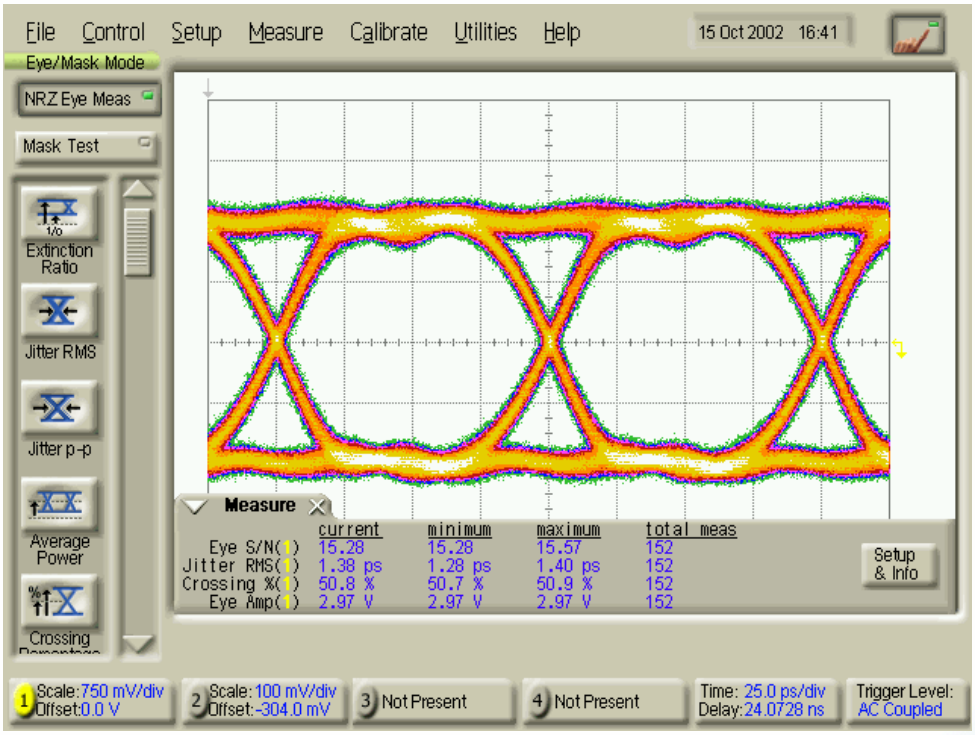
[1] 50 Ω ruggedized 2.9 mm precision female connector.
[2] 50 Ω ruggedized 1.85 mm precision male connector
[3] 50 Ω SMA female connector

Output Waveforms

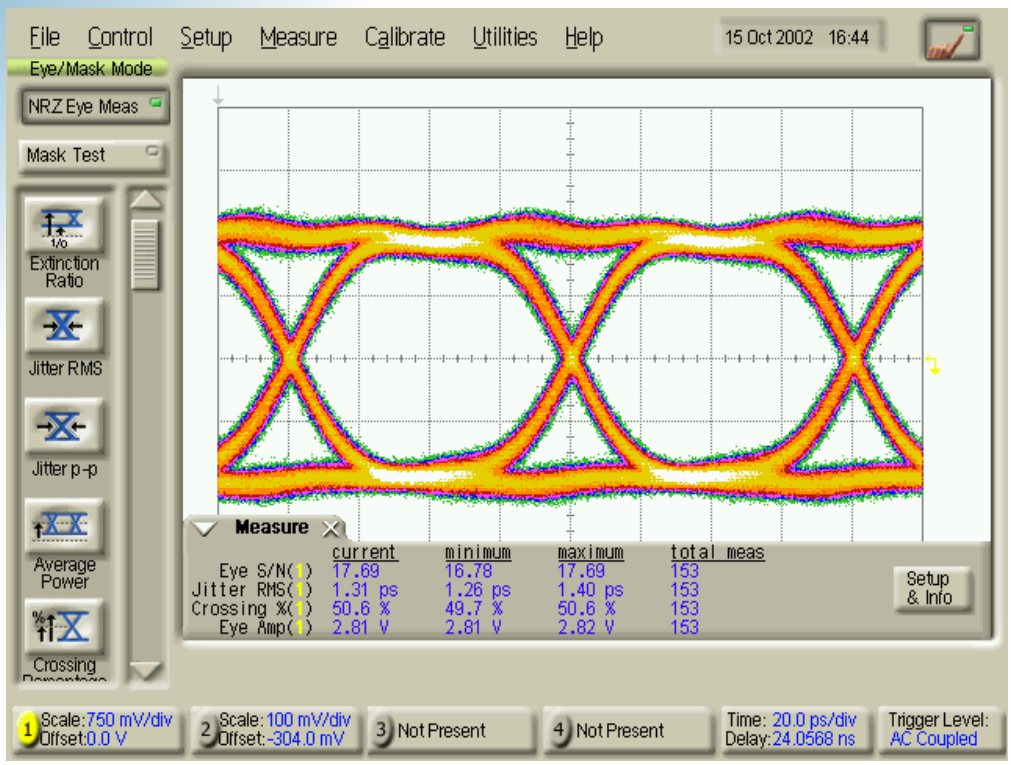
Clock Phase Margin Measurement
BER Limit 10^{-9}, PRBS 2^{31}-1, Eye Height 100 mV, Input Data Jitter[1] 5 ps_{pp}
Input Signal provided by SHF BPG 44



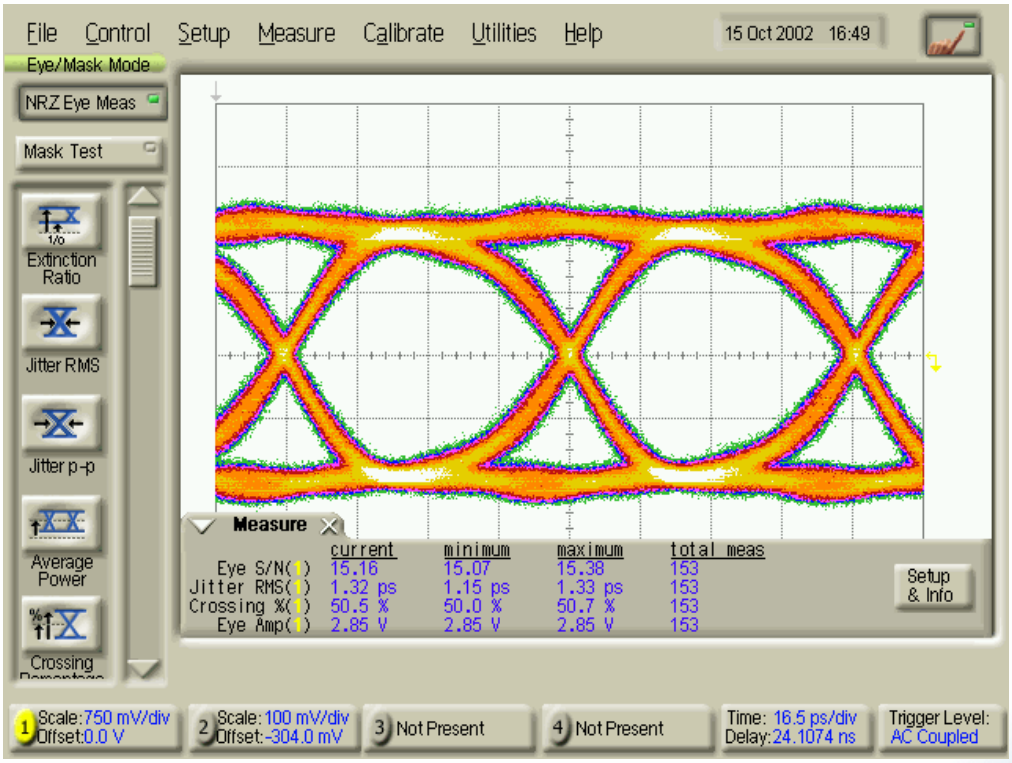
Subrate output at 10 GBit/s from a 40 GBit/s 100 mV input signal



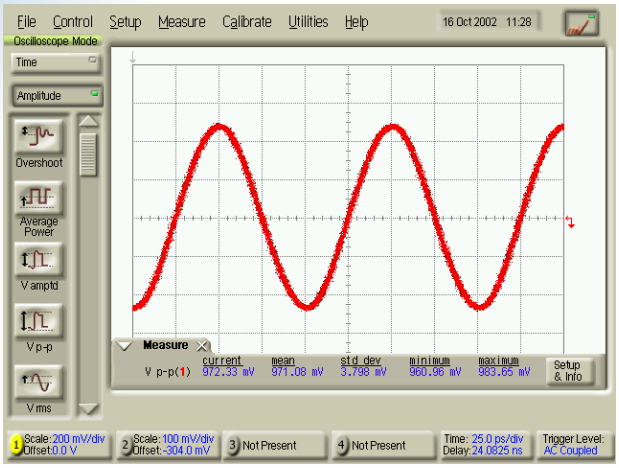
Subrate output at 12.5 GBit/s from a 50 GBit/s 100 mV input signal



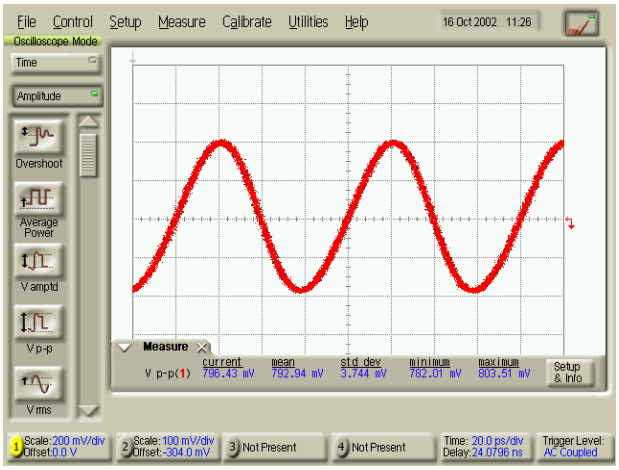
Subrate output at 15 GBit/s from a 60 GBit/s 100 mV input signal



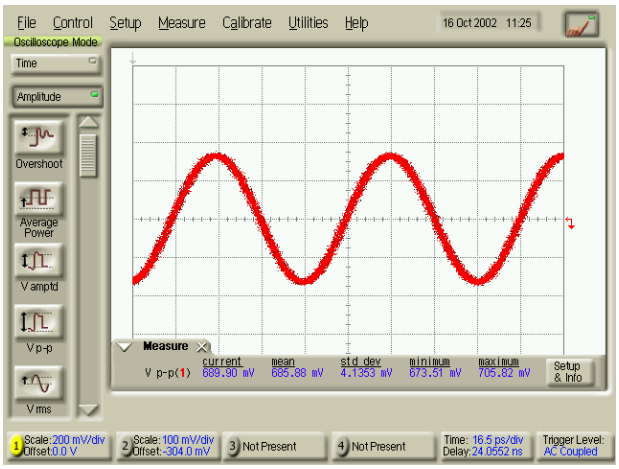
Clock outputs



10 GHz



12.5 GHz



15 GHz