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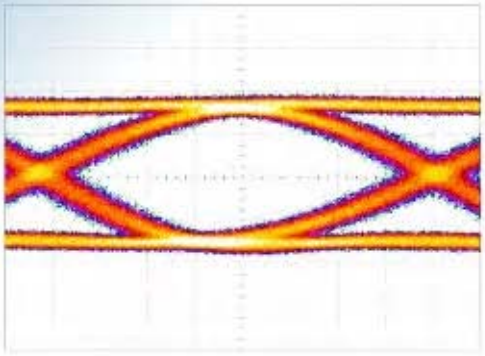


Datasheet

SHF 423 Demux

60 Gbps Demultiplexer Module

Description

The SHF 423 is a 1:4 demultiplexer operating at data rates up to 60 Gbps for use in SONET OC-768 and SDH STM-256 applications, broadband test setups, and telecom transmission systems. A 60 Gbps single ended serial data stream is accepted by the demultiplexer and converted into four single ended data signals at a nominal output data rate of 15 Gbps. A single ended clock signal (nominally 30 GHz) with a frequency half of the input data rate drives the SHF 423, and a copy of the divided input clock (with a nominal frequency of 15 GHz) is provided as an output signal to drive succeeding circuits or an error analyzer. Data and clock outputs are DC-coupled ground referenced CML signals with on-chip 50 Ω terminations. The data and clock inputs are AC-coupled and also include 50 Ω terminations.

Features

SiGe HBT technology
Supports input data rates from 2 Gbps up to 60 Gbps
Low power consumption: 3.5 W typ.
Dual power supply with internal voltage regulator ±5 V
V-type connectors for the 60 Gbps data input
K-type connectors for the data outputs and clock in-/outputs
SMB-type connectors for the clock/data bias inputs

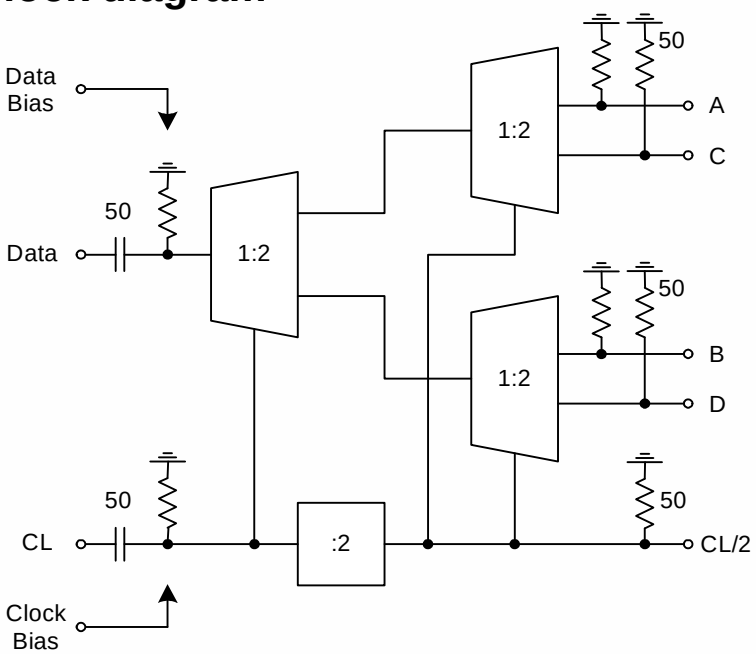
Applications

SONET OC-768 and SDH STM-256 applications
Broadband test setups
Telecom transmission systems and transponder prototyping

Option

Option BA: two potentiometers to allow data bias and clock bias to be adjusted without the need for additional power supplies.

Functional block diagram

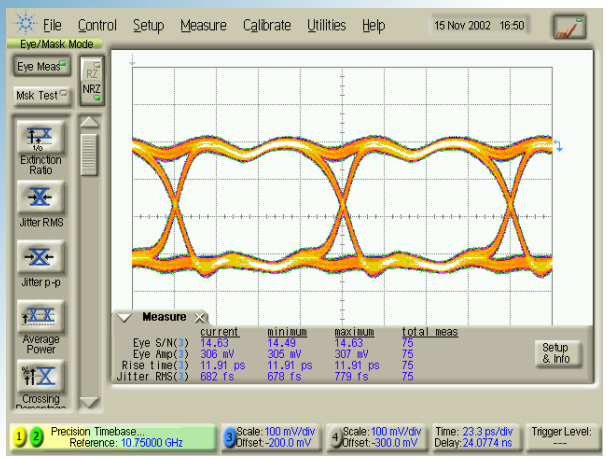


Specifications – SHF 423 DEMUX

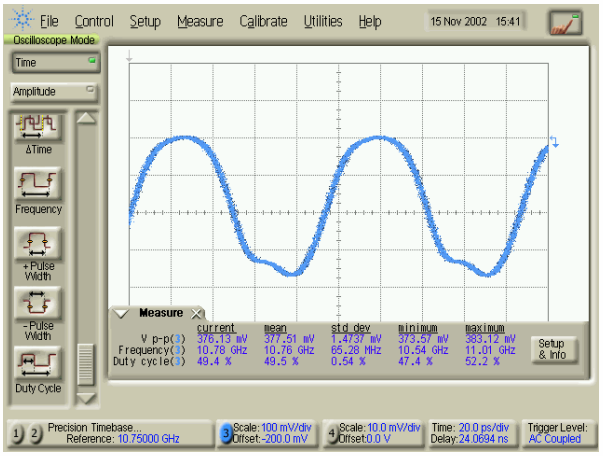
Parameter	Unit	Min.	Typ.	Max.	Conditions
Input parameters					
Data bit rate	Gbps	2		60	
Data eye amplitude	mV			1000	
Sensitivity	mV		50 150		<55 Gbps <60 Gbps
Return loss	dB			-10	
Output parameters					
Data bit rate	Gbps	0.5		15	
Voltage high level	mV		0		single ended
Voltage low level	mV		-300	-250	single ended
Eye amplitude	mV	250	300		single ended
Rise time	ps		15	20	(20%...80%)
Fall time	ps		15	20	(20%...80%)
RMS jitter	ps		1		
Return loss	dB			-10	
Clock parameters					
Input level	mV	400		1000	
Clock phase margin	deg	200 160			<50 Gbps <60 Gbps
Input return loss	dB			-10	
Clock/2 output level	mV	300	350		
Clock/2 output return loss	dB			-10	
Power requirements					
Negative supply voltage	V	-6.5		-5.0	
Negative supply current	mA	600	650	700	
Positive supply voltage	V	+5.0		+6.5	
Positive supply current	mA		20		
Total power dissipation	W		3.5		

Note: SHF also supplies adjustable delay lines for clock-data alignment purpose. See SHF application note AN423-1 for 1:4 demultiplexing operation setup.

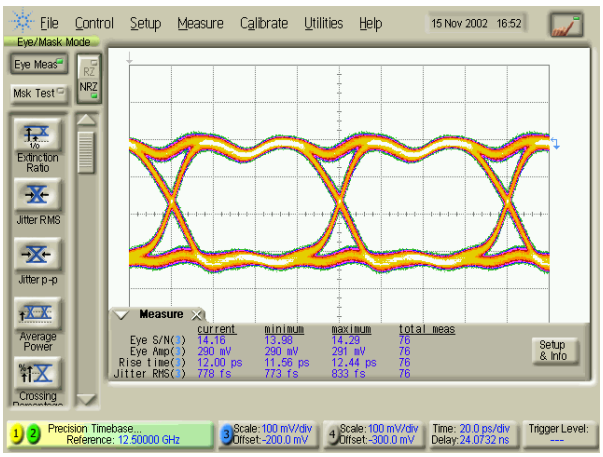
Output waveforms



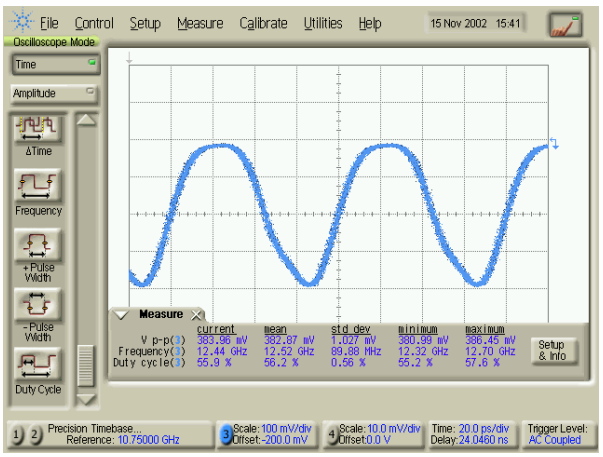
Eye Diagram at 10.75 Gbps
(43 Gbps input data rate), PRBS 2^{31}-1



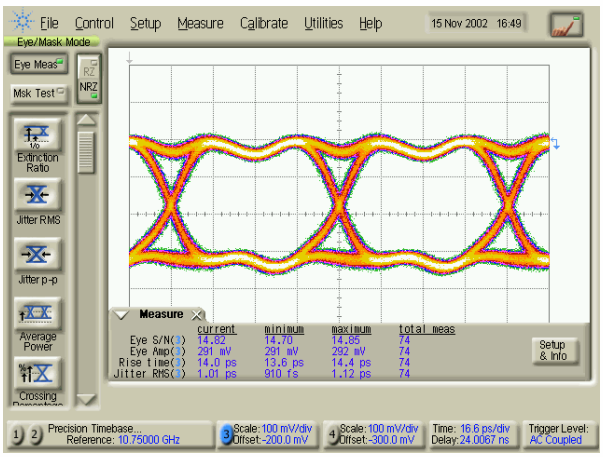
Clock/2 Output at 43 Gbps input data rate



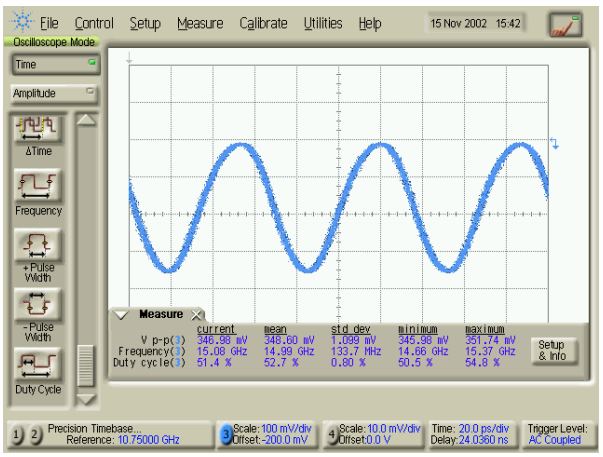
Eye Diagram at 12.5 Gbps
(50 Gbps input data rate), PRBS 2^{31}-1



Clock/2 Output at 50 Gbps input data rate



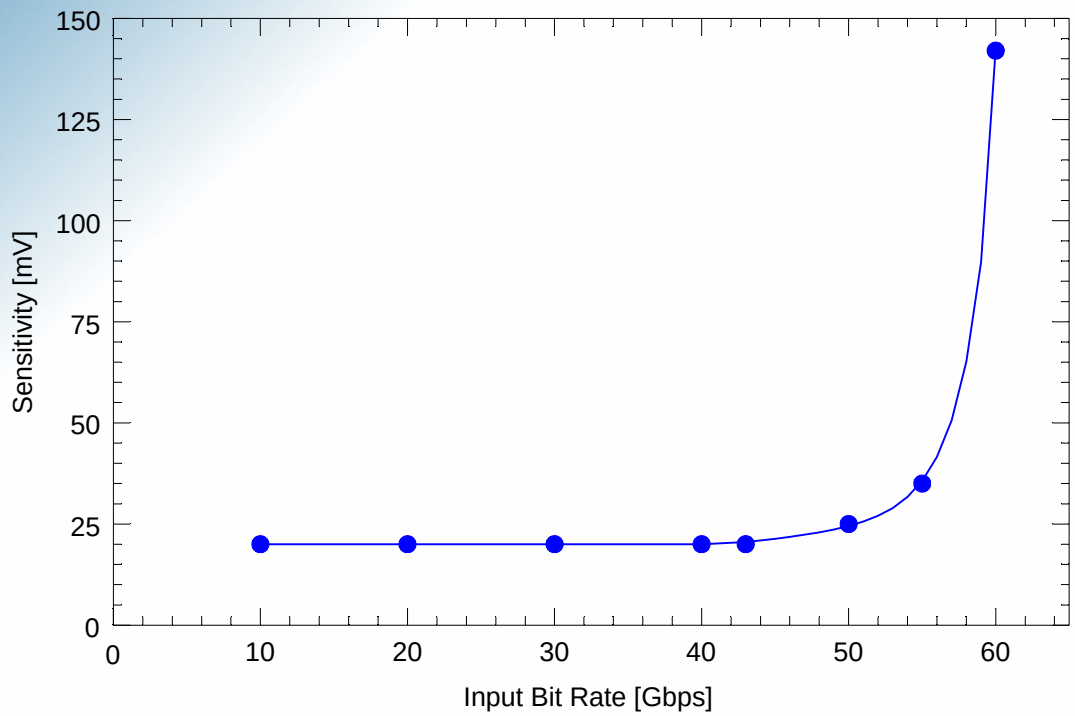
Eye Diagram at 15 Gbps
(60 Gbps input data rate), PRBS 231-1



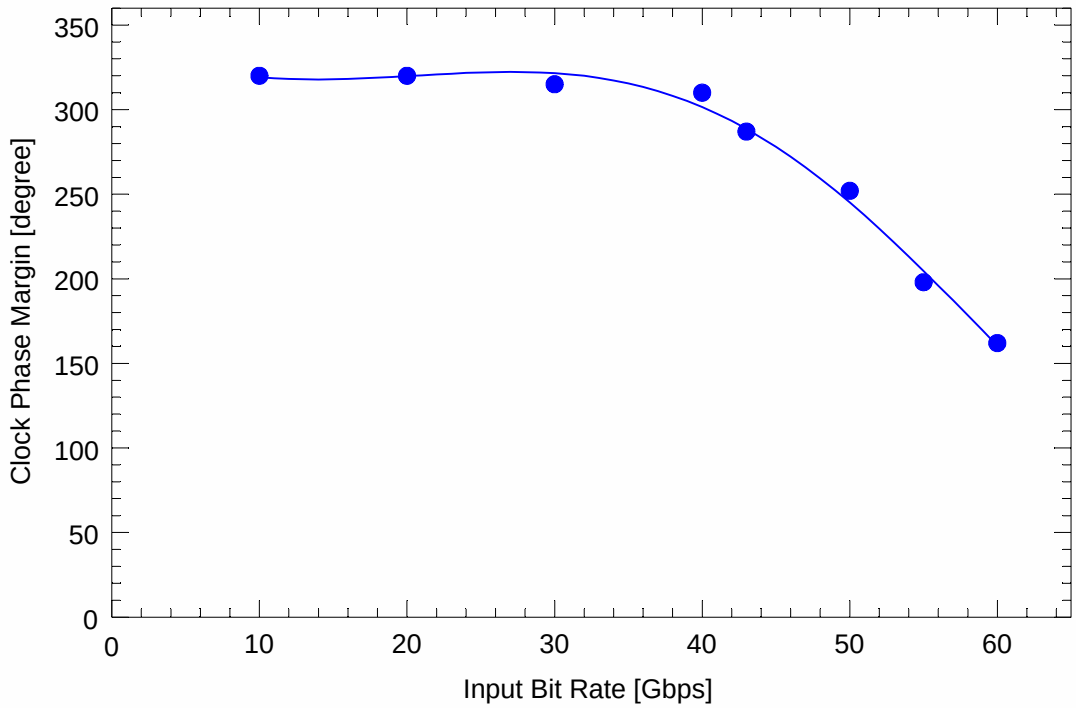
Clock/2 Output at 60 Gbps input data rate

Measured using Agilent DCA 86100B, sampling module 83484A [50 GHz], precision timebase module 86107A, 0.5 m microwave cable assembly, 10 dB attenuator

Sensitivity

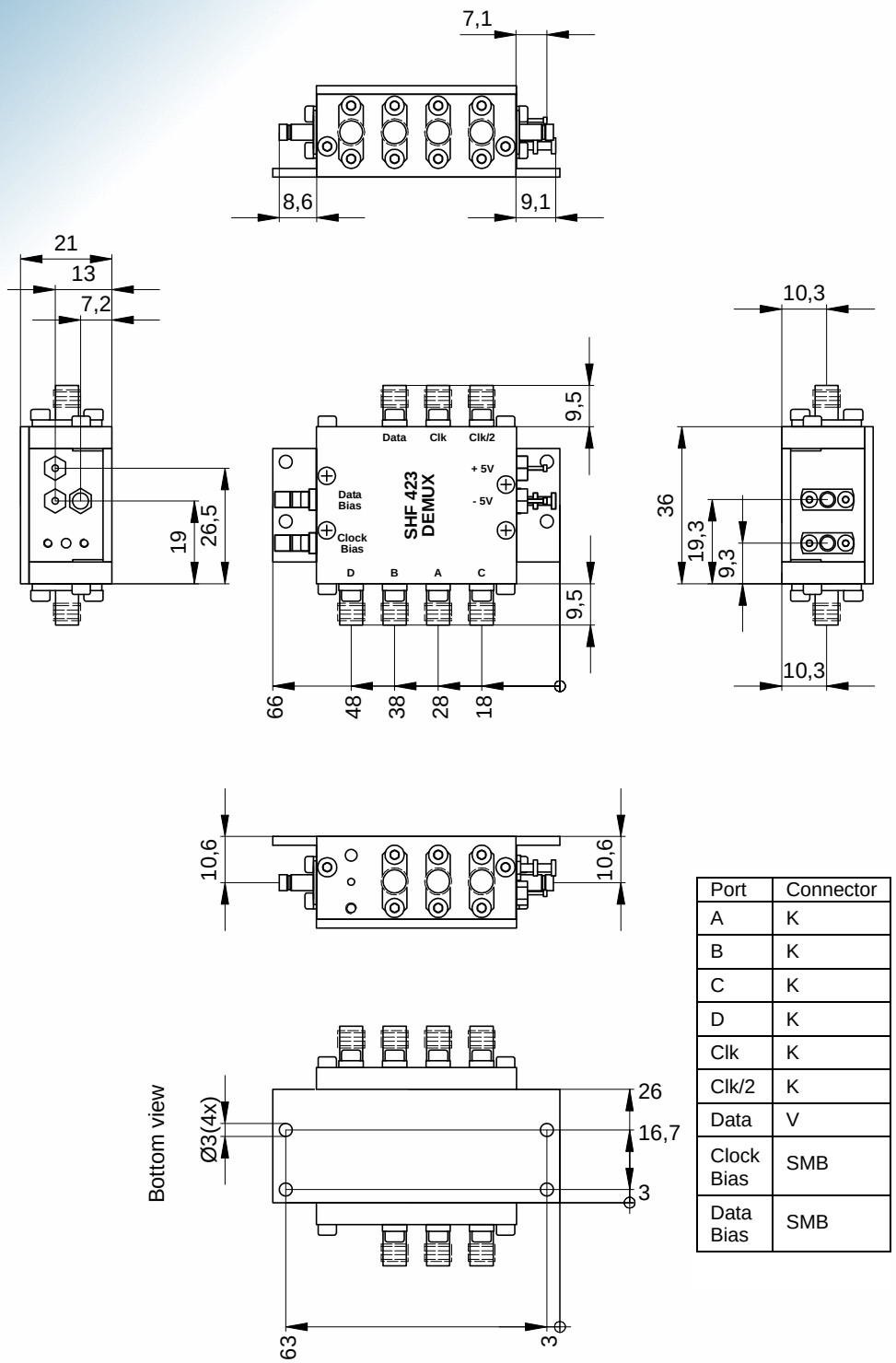


Clock phase margin



The results presented above represent the performance of a typical device

Module outline



Port	Connector
A	K
B	K
C	K
D	K
Clk	K
Clk/2	K
Data	V
Clock Bias	SMB
Data Bias	SMB

Please ensure that adequate cooling of the multiplexer is guaranteed. We recommend a heat sink with a thermal resistance of approx. 3 K/W

All dimensions in mm