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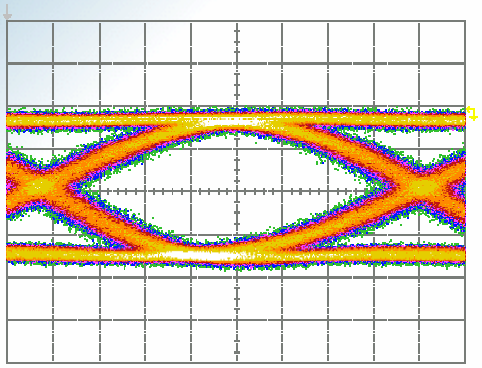


Datasheet

SHF 41210 A

Clock Recovery
Optical Receiver

SHF Communication Technologies AG
the bandwidth company

Description

The SHF 41210 A is an optical receiver and clock recovery unit. This is a half-width plug-in for the SHF 10000 A mainframe. Field installation or upgrade by the end-user is possible for this equipment.

It can be specified as just a receiver (option OE), or just clock recovery (option CR) or with both options. With both options fitted, they are connected internally so that the electrical data and the recovered clock signal are available from the outputs. It is still possible to use both options alone.

The optical receiver converts optical signals with a bit rate up to 50 Gbps into electrical signals. Broadband operation is possible and the wide output dynamic range combined with excellent pulse behavior makes the device ideal for optical system research.

The clock recovery extracts a clock signal at a frequency half of the incoming bit rate from an electrical data signal at a nominal bit rate of about 40 Gbps or about 43 Gbps. It contains two separate VCOs which allow operation in a standard mode at 39.81 Gbps or in an FEC mode to cover FEC bit rates of 42.65 Gbps or 43.01 Gbps respectively. Two reference frequencies are included as standard. The clock recovery option does not support broadband operation.

Features

Optical Receiver

Broadband operation up to 50 Gbps

High optical sensitivity

Wide output dynamic range

High output saturation suitable for 2R regeneration

Excellent pulse behavior

Unsurpassed high power handling capability

High responsivity

Clock Recovery

supports multiple data rates (standard bit rate mode at OC-768, non-FEC rates around 39.8 Gbps and FEC bit rate mode at OC-768 FEC rates around 43 Gbps)

clock output frequency at half and quarter of the nominal input data bit rate

a reference signal at input bit rate divided by 64 is required

only a 50 mV single ended input signal is required

excellent tolerance against input signal jitter

Options

CR – with clock recovery

OE – with optical/electrical converter

C40 – 40GHz clock output for clock recovery

Specifications – SHF 41210 A

Option CR – Clock recovery

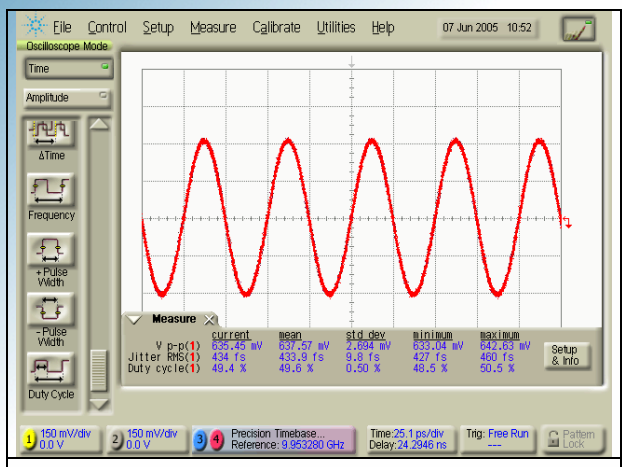
Parameter	Unit	Min.	Typ.	Max.	Comment
40/43 Gbps Data Input					
Operating bit rate VCO1 VCO2	Gbps	 39.5 42.5		 40.1 43.1	 NON-FEC mode FEC mode
Input Voltage	mV	50		1000	
625/672 MHz Reference Clock Input (bit rate divided by 64)					
Input Frequency	MHz	617 664		627 674	NON-FEC mode FEC mode
Input Voltage	mV	200		800	
Half Clock Output (half bit rate)					
Output Frequency	GHz	19.75 21.25		20.05 21.55	NON-FEC mode FEC mode
Output Voltage	mVpp	400	600	800	
RMS-Jitter	fs		400	500	on scope display, measured with Agilent 86100A with precision time base
Clock/4 Output (quarter bit rate)					
Output Frequency	GHz	9.875 10.625		10.025 10.775	NON-FEC mode FEC mode
Output Voltage	mVpp	400	600	800	
RMS-Jitter	fs			700	on scope display, measured with Agilent 86100A with precision time base
Full Clock Output (optional, full bit rate)					
Output Frequency	GHz	39.5 42.5		40.1 43.1	NON-FEC mode FEC mode
Output Voltage	mVpp	400	600	800	
RMS-Jitter	fs		500	600	on scope display, measured with Agilent 86100A with precision time base

Option OE – Optical receiver

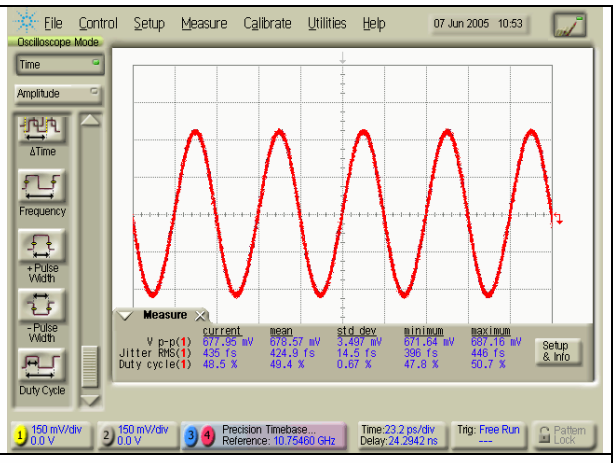
Parameter	Unit	Min.	Typ.	Max.	Comment
Wavelength range		C and L band			
High frequency 3dB point	GHz	30			
Low frequency 3dB point	kHz			30	
Conversion gain	mV/mW	350	450		at 1550 nm
Receiver sensitivity	dBm		-9		
Output saturation voltage (peak-peak)	V		5	6	
Rise/fall times	ps		9	10	10…90%
Optical input power	dBm			13	CW

Test Results

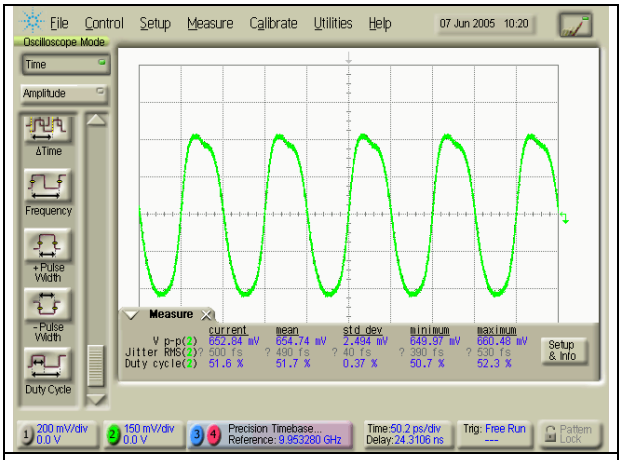
Option CR – Clock recovery



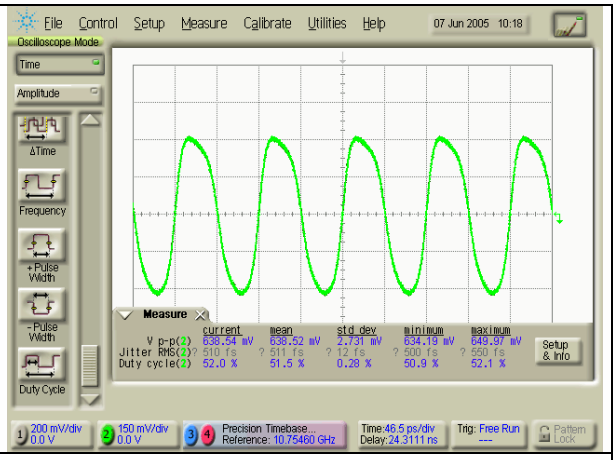
Half Clock Out @ 39.81 Gbps



Half Clock Out @ 43.018 Gbps



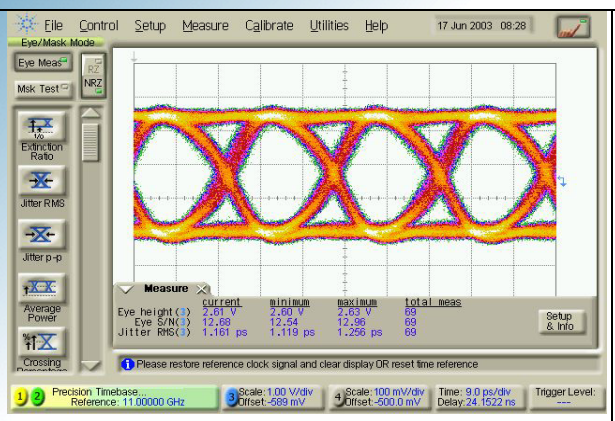
Clock/4 Out @ 39.81 Gbps



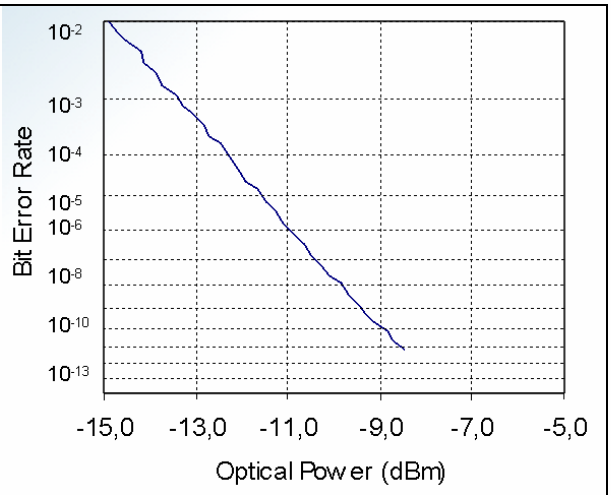
Clock/4 Out @ 43.018 Gbps

Test Results

Option OE – Optical receiver



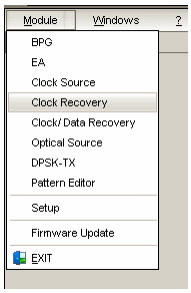
40 Gbps electrical output signal with 6dBm optical input power



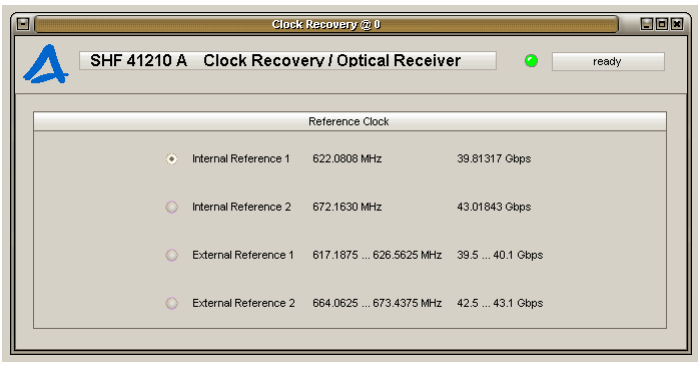
Sensitivity measurement

Application Remarks Clock Recovery

1. Open the “Clock Recovery Module” from the Module Menu.



2. The Clock Recovery Module is used to control the SHF 41210 A. The following screen is displayed when Clock Recovery Module is selected.



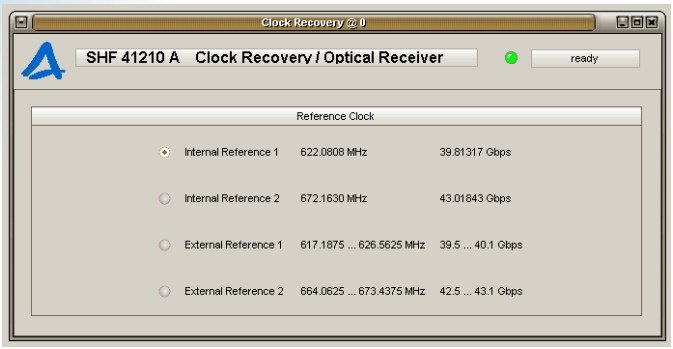
3. The unit can be operated in two bit rate ranges – the “NONFEC” range between 39.5 Gbps and 40.1 Gbps and the “FEC” range between 42.5 Gbps and 43.01 Gbps. The desired range has to be selected in the reference clock section.

4. The internally used phase detector needs a bit rate divided by 64 reference signal. If the operating bit rate deviates from those supported by the internal reference oscillators, an external reference signal has to be applied, e.g. operation at exactly 40 Gbps requires a 625 MHz reference signal (40G/64). The user has to select the appropriate setting in the reference clock section. If an operating mode using an external reference is selected it is indicated by a green LED next to this reference clock input (Ref. Clock In).

5. Depending on the topology used to split the incoming signal into the data and clock recovery path it might be necessary to improve the input reflection coefficient with an attenuator.

Operation at 39.81 Gbps

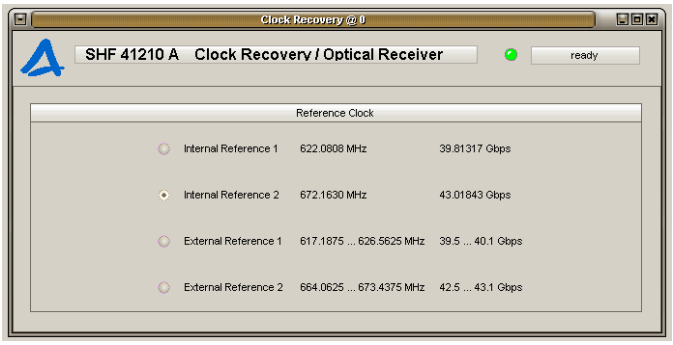
Set the reference clock selector to “Internal Reference 1”.



Apply a data signal to the “Data In” input.
The recovered 19.9 GHz clock signal is available at the “Half Clock Out” output.

Operation at 43.01 Gbps

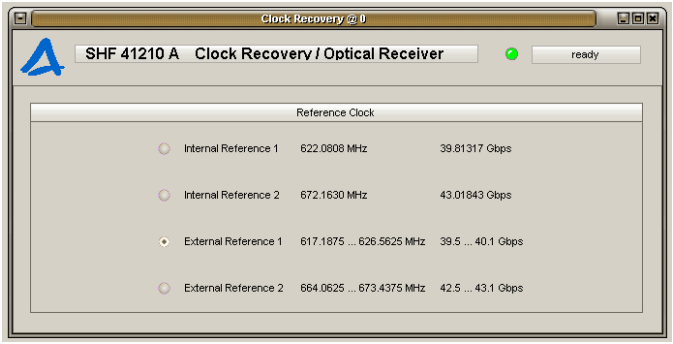
Set the reference clock selector to “Internal Reference 2”.



Apply your 43.01 Gbps data signal to the “Data In” input.
The recovered 21.5 GHz clock signal is available at the “Half Clock Out” output.

Operation between 39.5 Gbps and 40.1 Gbps

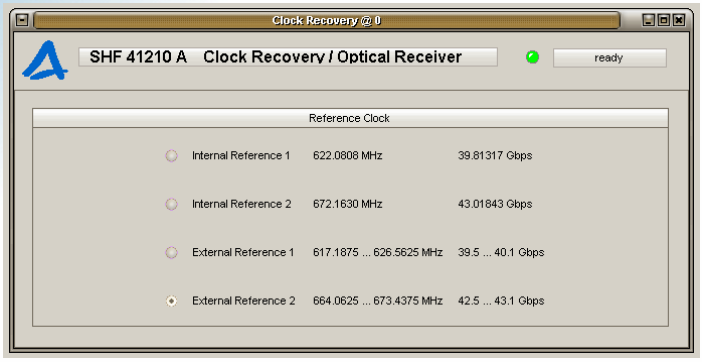
Set the reference clock selector to “External Reference 1”.



Apply a reference clock signal (bit rate divided by 64) to the “Ref Clock In” input.
Apply a data signal to the “Data In” input.
The recovered clock signal is available at the “Half Clock Out” output.

Operation between 42.5 Gbps and 43.1 Gbps

Set the reference clock selector to “External Reference 2”.



Apply a reference clock signal (bit rate divided by 64) to the “Ref Clock In” input.
Apply a data signal to the “Data In” input.
The recovered clock signal is available at the “Half Clock Out” output.

Topologies

The incoming data signal has to be separated into two paths – the data path to the error analyzer and the clock path to the clock recovery module. If you have an optical signal there are two possibilities to split – optical or electrical. From our point of view its better to split the optical signal (Fig. 1), provided that you have two high speed photo diodes available.

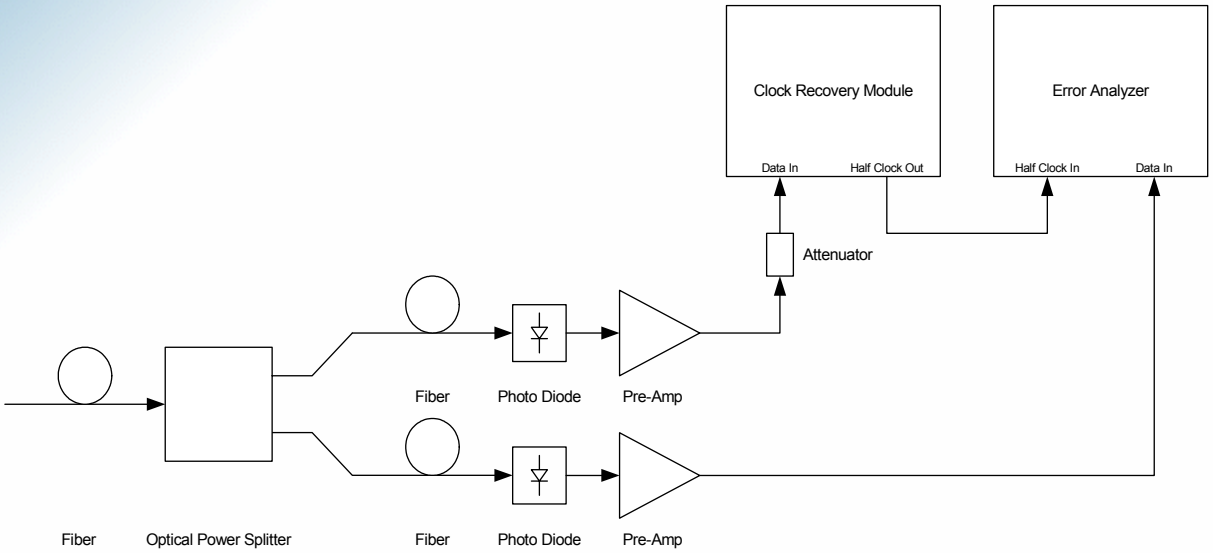


Fig. 1

If you have to split the electrical signal, Fig. 2 applies. In case a 6 dB power splitter is used we recommend using an attenuator of at least 6 dB at the clock recovery data input to prevent deterioration of the data signal going to the error analyzer.

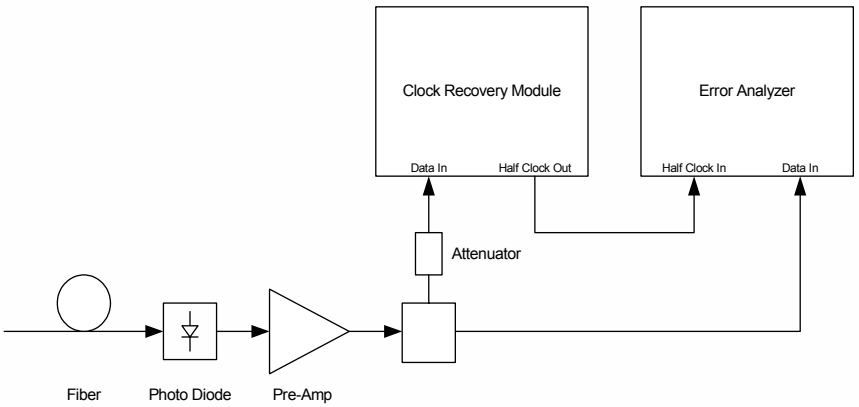


Fig. 2