

Data Sheet

SHF 12126 A



Compact Multi-Channel
Bit Pattern Generator
32 Gbps NRZ
32 GBaud PAM4



Description

The SHF 12126 A is a three channel 32 Gbps NRZ/32 GBaud PAM4 bit pattern generator. It features two single ended data outputs with individual 4-Tap pre-emphasis capabilities, 2 UI skew control and duty cycle adjustment up to 32 Gbps. In addition a differential 32 GBaud PAM4 output is provided. Digital bit sequences such as standard pseudo-random bit sequences (PRBS) or short user defined bit patterns are generated by the unit at the data outputs. Many applications in research, product development as well as production tests require these data streams for testing electrical/optical components or testing signal integrity in high speed digital data communication. A wide range of operating bit rates from 7 to 32 Gbps/32 GBaud is covered.

The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The generator operates at full clock, i.e. a 32 GHz clock signal is required for 32 Gbps/32 GBaud operation.

For trigger purposes three clock output signals (clock, clock/2 and clock/16) are provided on the rear panel of the instrument.

Its compact size allows placement very close to the DUT in the test setup.

Features

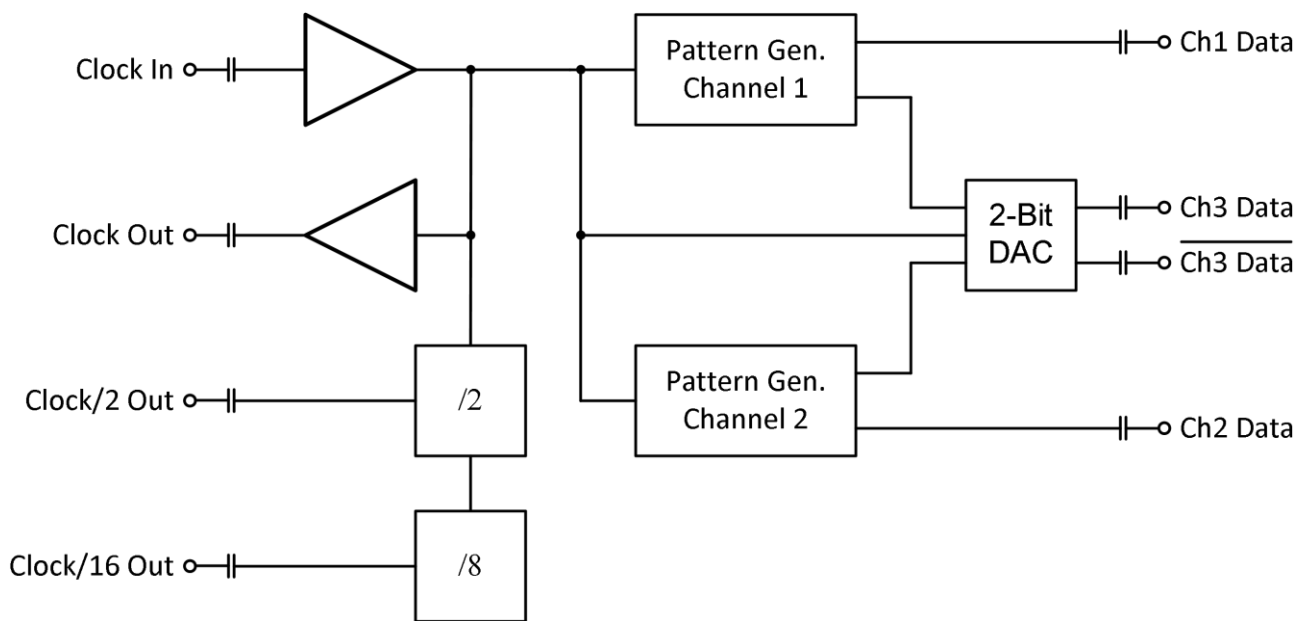
- One differential output channel up to 32 GBaud PAM4 (7 to 32 Gbaud operation, 'gap-free')
- Two single ended output channels up to 32 Gbps (7 to 32 Gbps operation, 'gap-free')
- Output amplitude control
- 4-Tap-FIR pre-emphasis individually adjustable for both 32 Gbps NRZ channels
- Skew control over two UI with 1/32 UI resolution for each 32 Gbps NRZ output
- PRBS 2^7-1 , $2^{11}-1$, $2^{15}-1$, $2^{23}-1$, $2^{31}-1$
- 32 Bit user programmable pattern @ 32 Gbps NRZ channels
- Three clock outputs (input clock, input clock divided-by-2 and 16) for trigger purposes
- Built-in frequency counter for input clock
- Control by Ethernet interface
- Low power consumption
- Compact size: 221.4 mm (W) x 50.8 mm (H) x 177 mm (D)



Applications

- Research, Development, Production Tests
- On-Wafer Testing
- CEI-28G
- 100G Ethernet
- Infiniband
- Fibre Channel[®]
- High Speed Serial
- Backplane Applications

Block Diagram





Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Data Outputs (Channel 1 and 2, single ended 32 Gbps NRZ)						
Minimum Bit Rate	Gbps				7	
Maximum Bit Rate	Gbps		32			
Output Amplitude	mV	V_{out}	350	430	500	adjustable by up to -6 dB, AC coupled, no pre-emphasis applied
Jitter (RMS)	fs	J_{RMS}		450	600	measured at 32 Gbps, on scope display ¹
Jitter (PP)	ps	J_{PP}		2.7	4	measured at 32 Gbps, on scope display ¹
Crossing	%		47	50	53	
Duty Cycle	%		47	50	53	of two consecutive eyes, can be adjusted using BCC
Skew Control	UI		-1		+1	adjustable in 1/32 UI-steps
Connector Type	Ω			50		2.92 mm (K) female
Rise/Fall Time	ps	t_r/t_f		14	15	20%...80%, on scope display
Data Outputs (Channel 3, differential 32 GBaud PAM4)						
Minimum Baud Rate	GBaud	$R_{out,min}$			7	
Maximum Baud Rate	GBaud	$R_{out,max}$	32			
Output Amplitude	mV	V_{out}	550	630	750	Single ended, full scale, adjustable up to -6 dB, see table on page 5
Rise- / Fall Time	ps	t_r/t_f		8	10	20%...80%, deconvolved ²
Equivalent Bandwidth	GHz	BW	22	27		Derived from Rise Time using formula ³ , -3 dB bandwidth
Connector Type	Ω			50		1.85 mm (V) female

¹ Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2³¹-1

² Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r,deconvolved} = \sqrt{(t_{r,measured})^2 - (t_{r,oscilloscope})^2} = \sqrt{(t_{r,meas.})^2 - (3.68 \text{ ps})^2}$

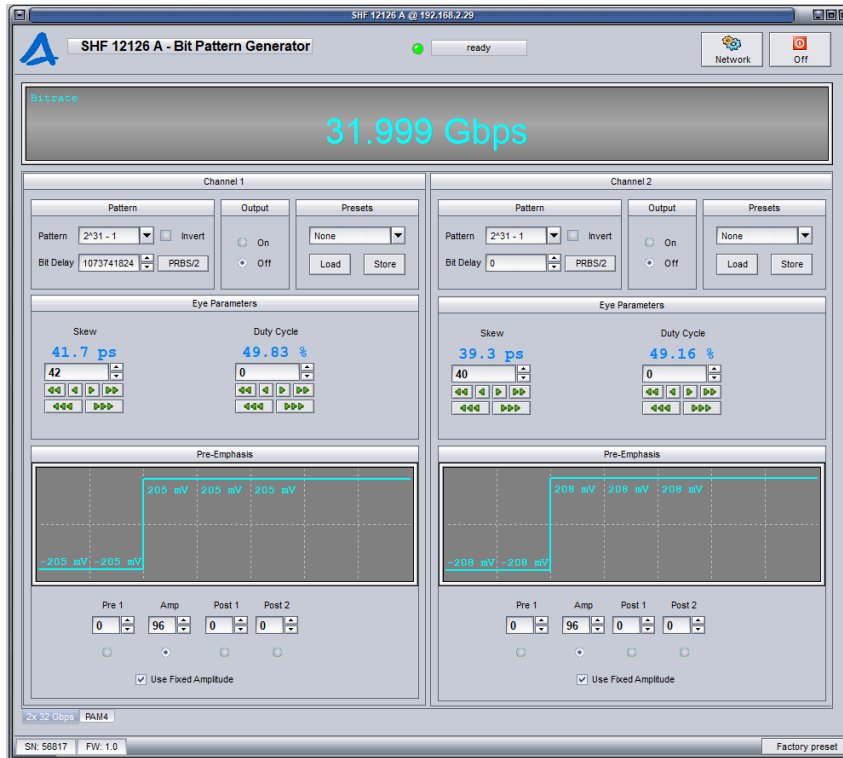
³ Calculation based on formula: $BW = \frac{0,22}{T_r}$



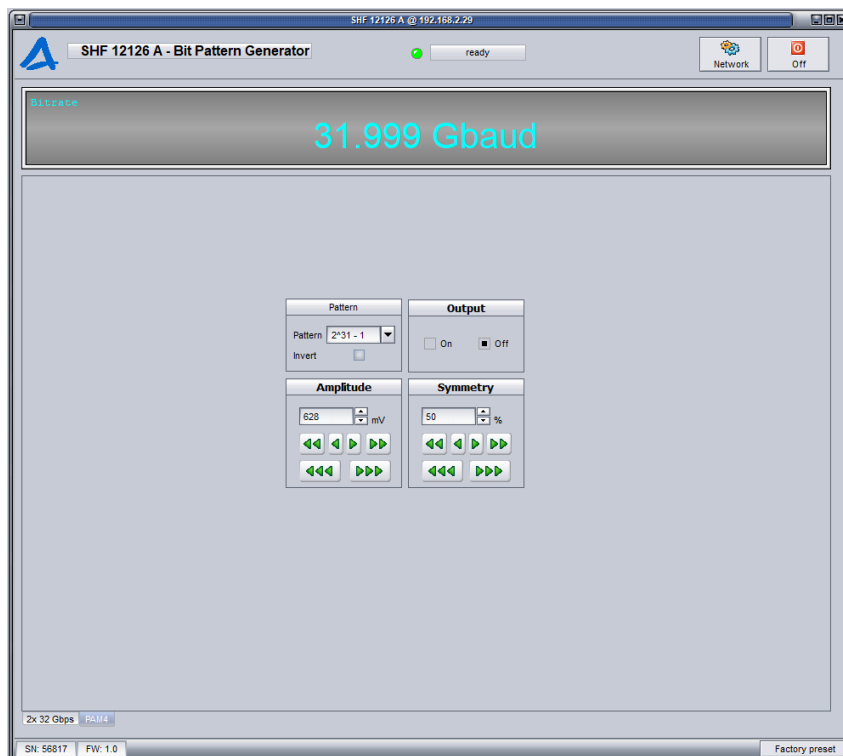
Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock						
Connector Type						2.92 mm (K) female
Clock Input						2.92 mm (K) female
Clock Output	Ω			50		2.92 mm (K) female
Clock/2 Output						2.92 mm (K) female
Clock/16 Output						2.92 mm (K) female
Clock Input Frequency	GHz	f_{in_clock}	7		32	
Input Level	mV _{pp}	V_{in_clock}	600		1000	AC coupled
Output Level						
Clock	mV _{pp}	V_{out_clock}	450	550	700	AC coupled
Clock/2			600	750	900	AC coupled
Clock/16			300	400	550	AC coupled
Output Frequency						
Clock	GHz	f_{out_clock}	7		32	Input frequency
Clock/2	GHz		3.5		16	half of input frequency
Clock/16	GHz		0.438		2	input frequency/16
Pattern						
Output Pattern						ITU-T (CCITT) conform PRBS patterns at a length of 2^7-1 , $2^{11}-1$, $2^{15}-1$, $2^{23}-1$ & $2^{31}-1$ plus user defined pattern
User Pattern Memory Size Channel 1&2	bit				32	
Clock Output Pattern						Output can be set to transmit a clock pattern clock/2, clock/4, clock/8, clock/16
General						
Supply Voltage	V	V_{cc}	11.5	12	12.5	+12 V switching power supply is included
Power Consumption	W	P_{tot}			16	
Height	mm	H		50.8		
Width	mm	W		221.4		
Depth	mm	D		177		
Weight	g	m			1700	
Operating Temperature	°C	$T_{ambient}$	15		35	



Graphical User Interface



User Interface in 2x32 Gbps Mode for Channels 1 and 2

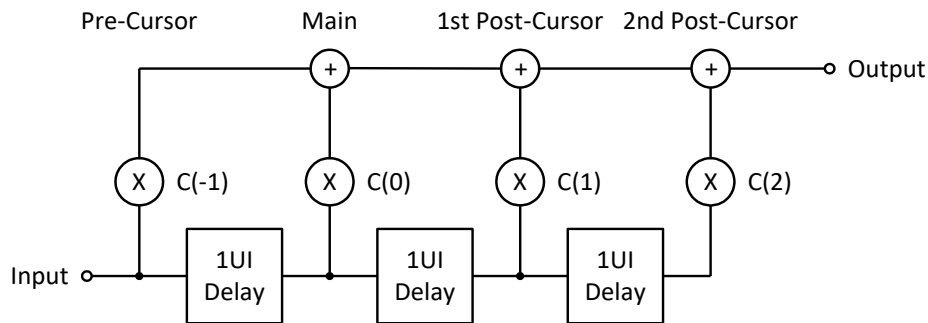


User Interface in 32 GBaud PAM-4 Mode for Channel 3

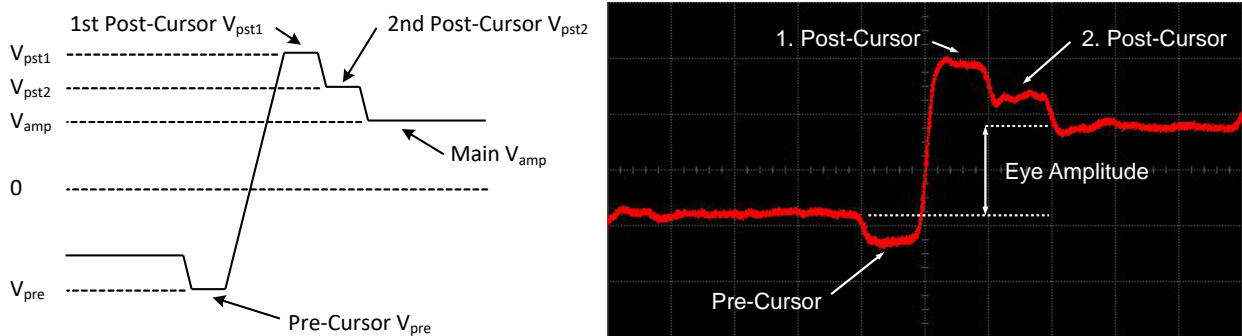
Pre-Emphasis Terms and Definitions (Channel 1 and 2 only)

Pre-emphasis based on a finite impulse response (FIR) filter is a way to compensate for high frequency losses in a transmission path. It helps to reduce the inter-symbol interference when the filter coefficients can be set adequately to compensate the imperfections of the channel's impulse response. The basic idea is to boost the high-frequency components while leaving the low frequency components in their original state.

The SHF 12126 A features a 4-Tap FIR filter structure for each channel as depicted in the following picture.



The structure can be used very flexible. Up to four taps can be used and each one is individually controllable. Polarity inversion allows to add or subtract the tap from the main signal. Depending on the weight of the taps different configurations as pre- and post-cursors are possible. The most common configuration is probably the use of one pre- and two post-cursors. As depicted in the following picture.



The ratio of the individual taps to the final eye amplitude is given by the following equations:

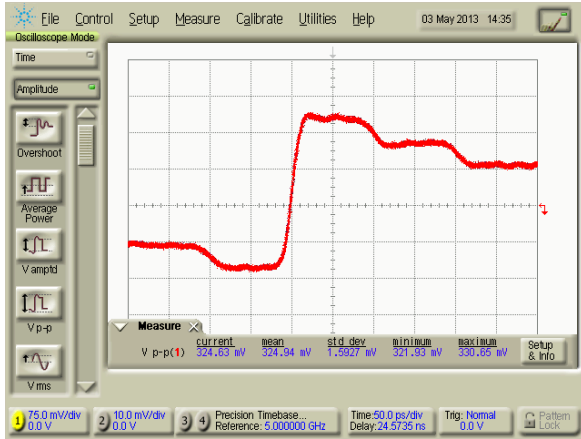
$$R_{pre}[dB] = 20 \cdot \log \left(\frac{|V_{pre}|}{V_{amp}} \right)$$

$$R_{pst1}[dB] = 20 \cdot \log \left(\frac{|V_{pst1}|}{V_{amp}} \right)$$

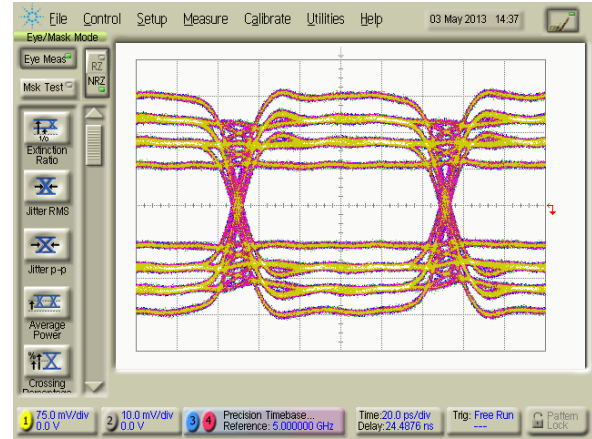
$$R_{pst2}[dB] = 20 \cdot \log \left(\frac{|V_{pst2}|}{V_{amp}} \right)$$



The following pictures show how pre- and post-cursor appear in the waveform or eye diagram of the signal.



10 Gbps – One Pre- & Two Post-Cursors



10 Gbps – One Pre- & Two Post-Cursors

Pre-Emphasis Software Representation

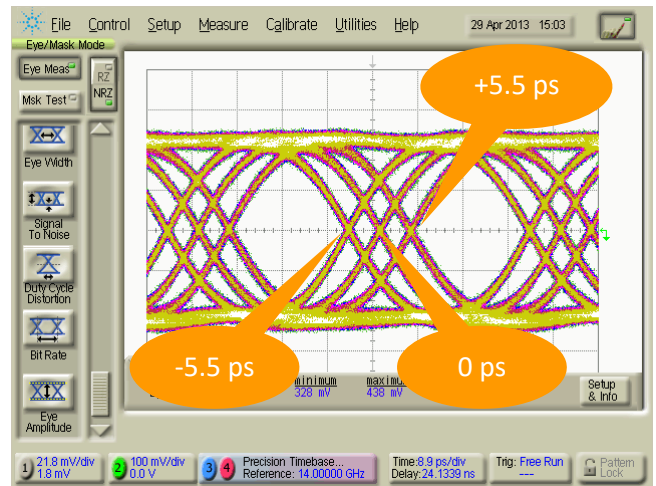


Skew Control Function (Channel 1 and 2 only)

The skew control function allows adjusting the channel timing relative to each other. As a result, timing delays between the two output channels can be compensated. The skew can be controlled in steps of $1/32$ UI. The maximum skew range is 2 UI, i.e. two eye lengths. Since the built-in phase rotator is optimized for operation between 25 Gbps and 30 Gbps step accuracy might degrade at lower and higher bitrates.



Skew Control Software Representation

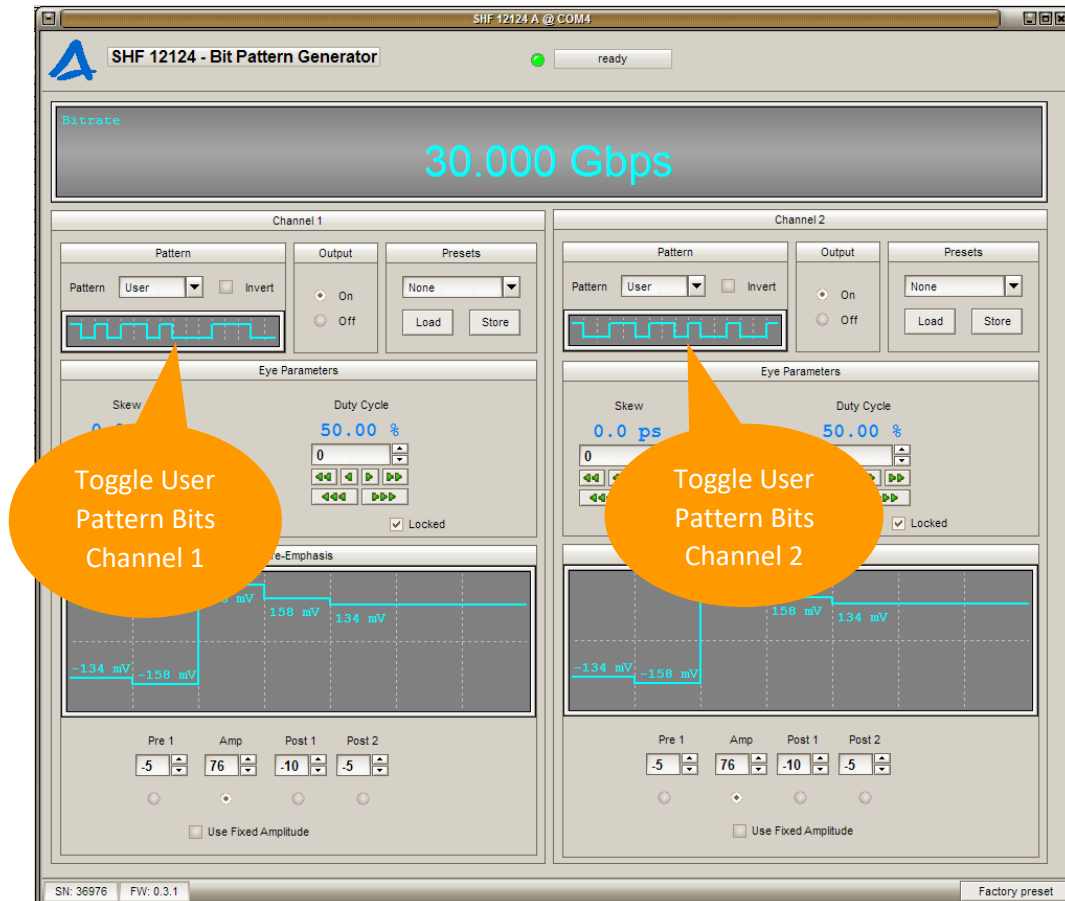


Skew Control Eye Diagram Representation



User Pattern Function

Besides the five pseudo-random bit sequences and the clock patterns a 32-Bit user pattern can be transmitted from each output. The user pattern can be set using a graphical representation in the user interface.

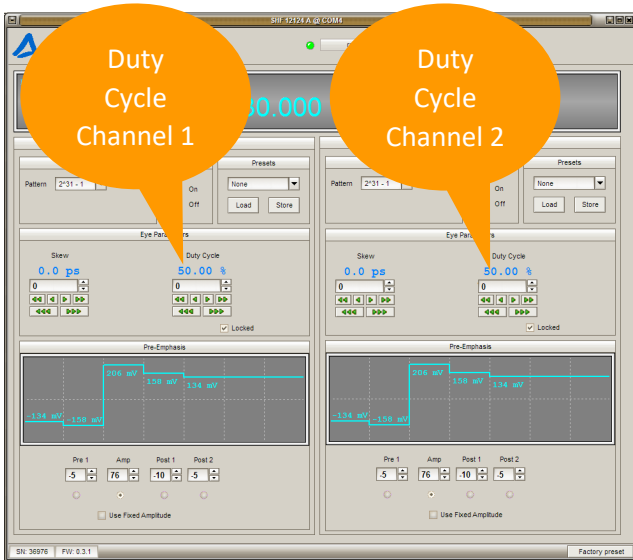


User Pattern Software Representation

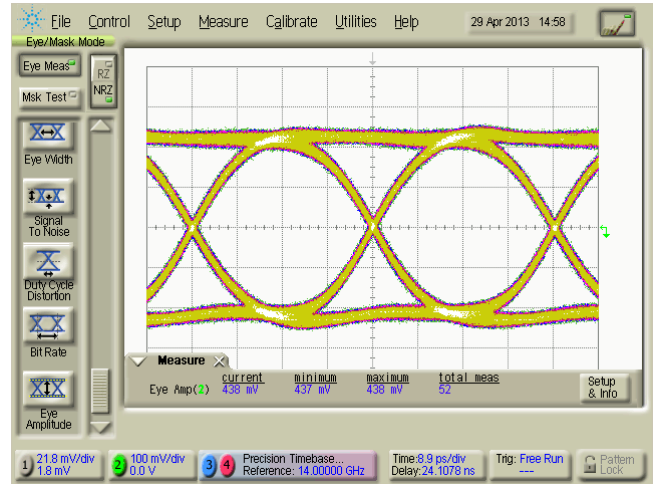


Duty Cycle Control Function (Channel 1 and 2 only)

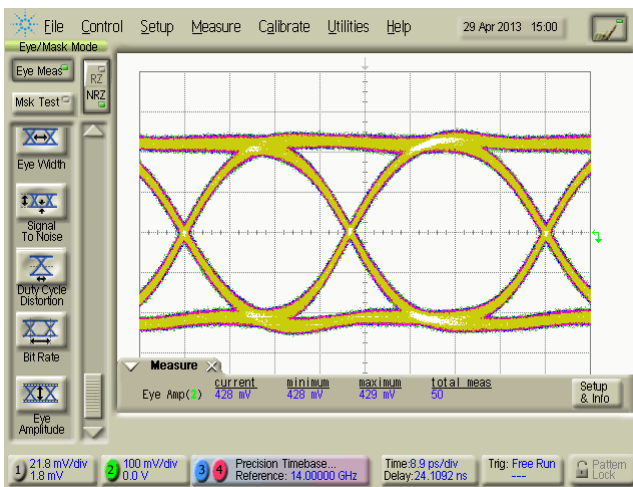
The duty cycle control function allows adjusting the length of consecutive eyes with a range of approximately +/-5% and with a 0.33% resolution.



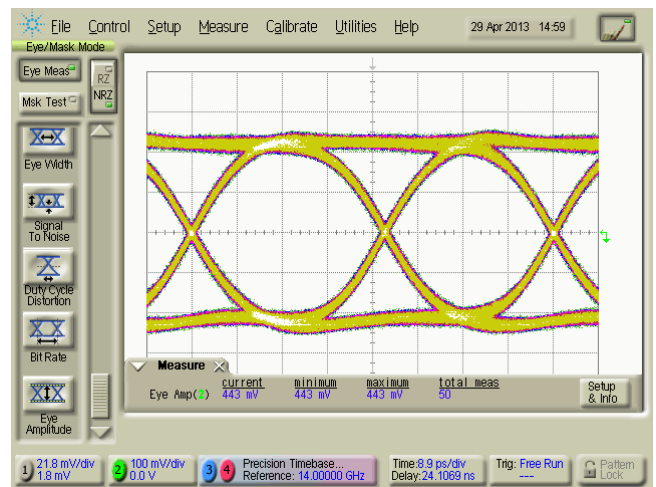
Duty Cycle Control Software Representation



Duty Cycle Control Set to 50%



Duty Cycle Control Set to less than 50%

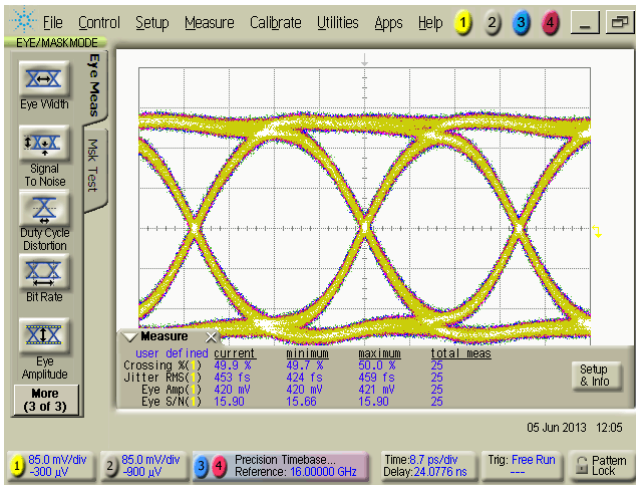


Duty Cycle Control Set to more than 50%

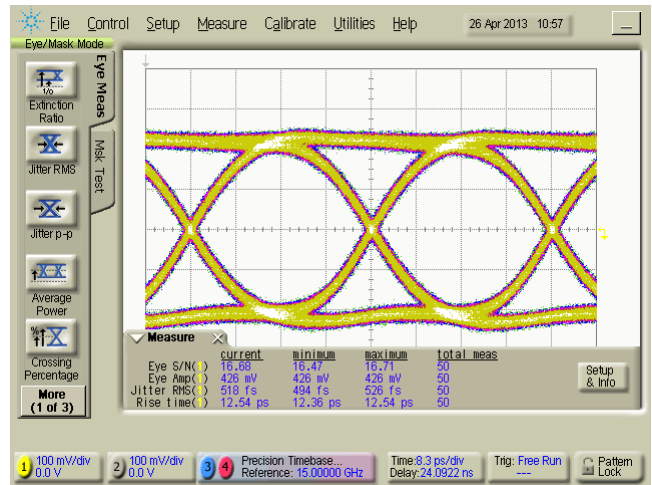


Typical Output Waveforms

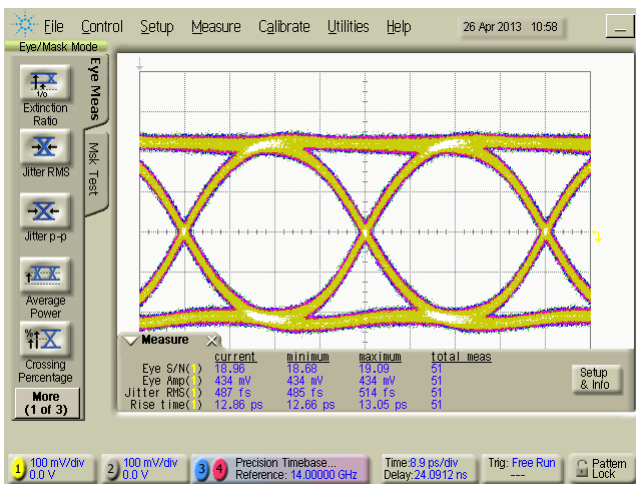
Data Output Signals (Channel 1 and 2 only, Pre-Emphasis completely deactivated)



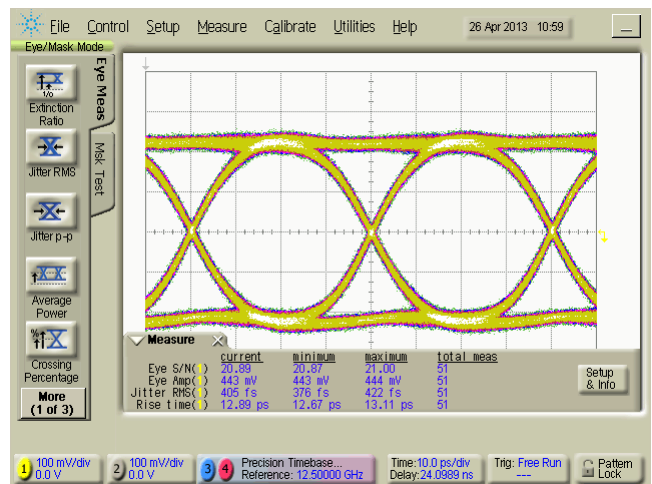
32 Gbps output eye at maximum output level



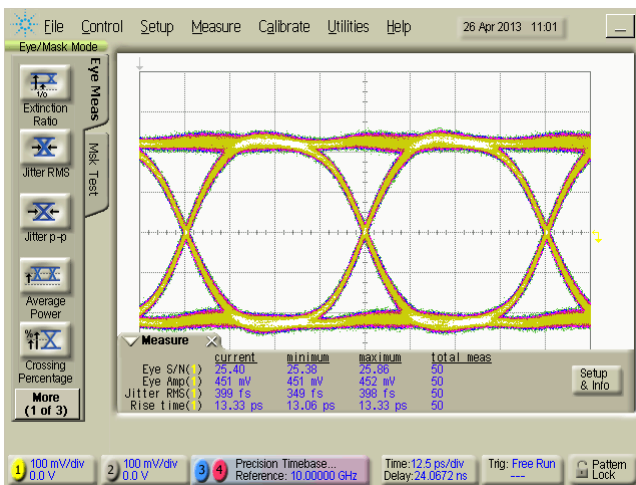
30 Gbps output eye at maximum output level



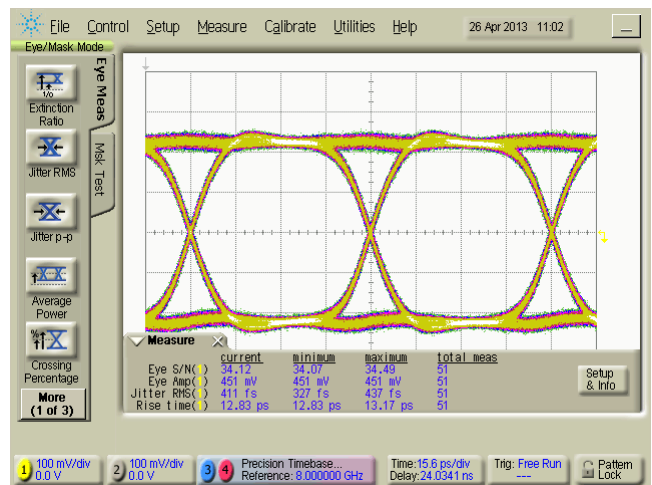
28 Gbps output eye at maximum output level



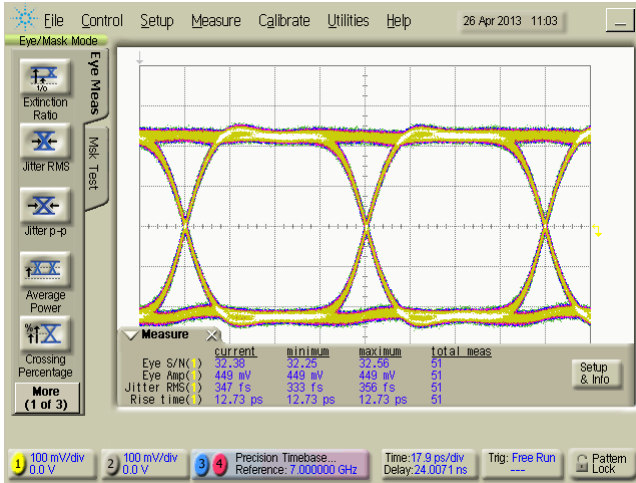
25 Gbps output eye at maximum output level



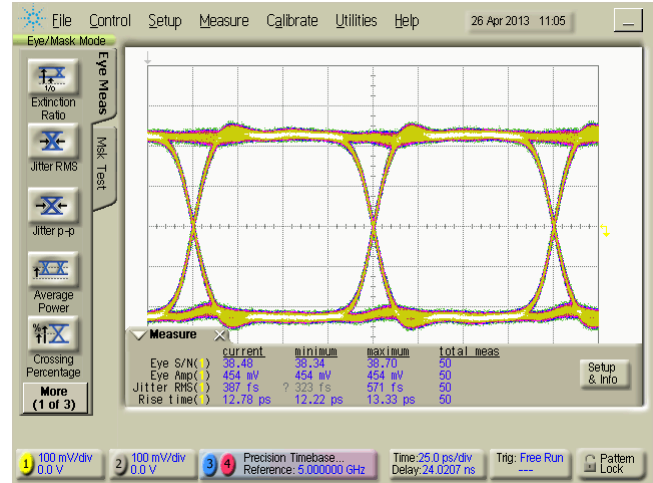
20 Gbps output eye at maximum output level



16 Gbps output eye at maximum output level



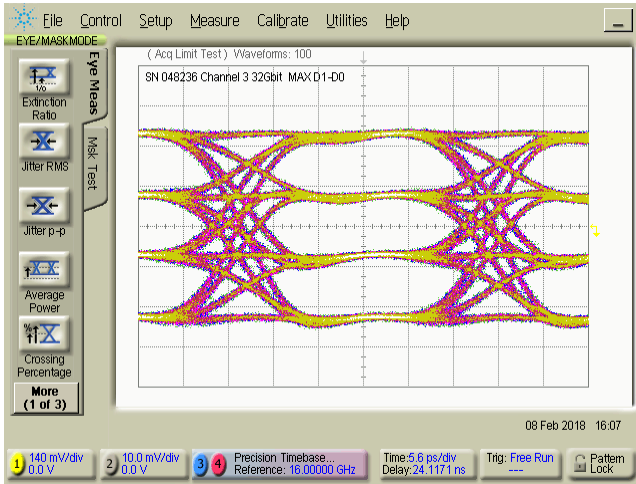
14 Gbps output eye at maximum output level



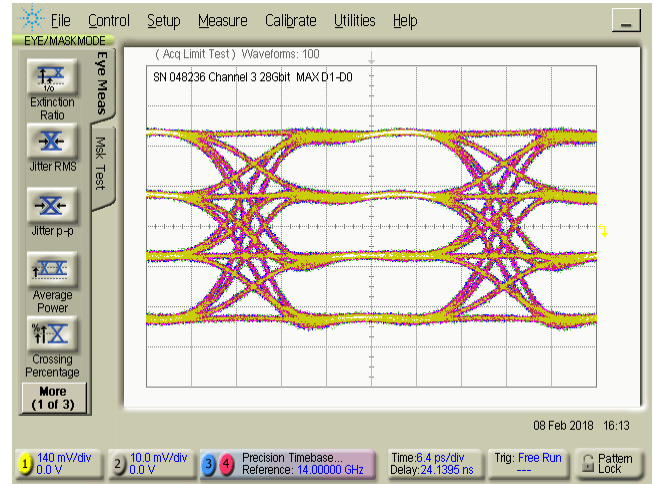
10 Gbps output eye at maximum output level



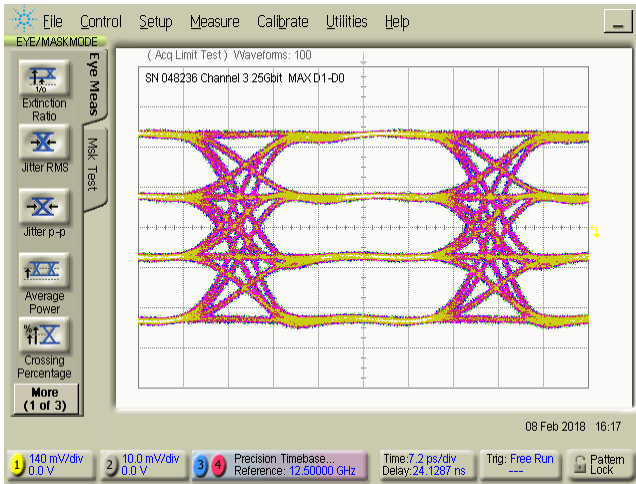
PAM4 Data Output Signals (Channel 3 only)



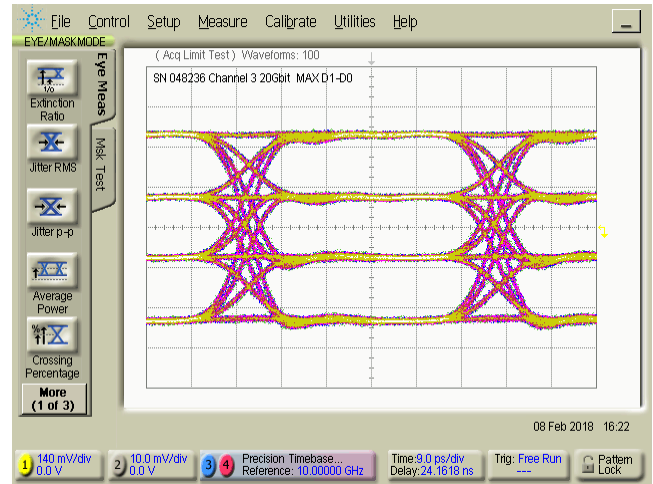
Ch3 @ 32 GBaud



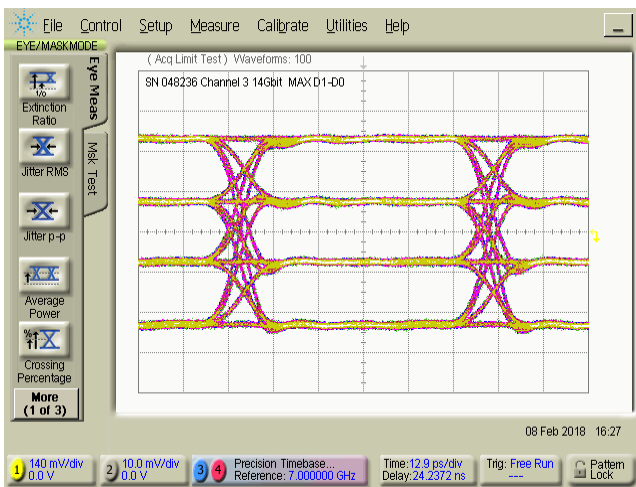
Ch3 @ 28 GBaud



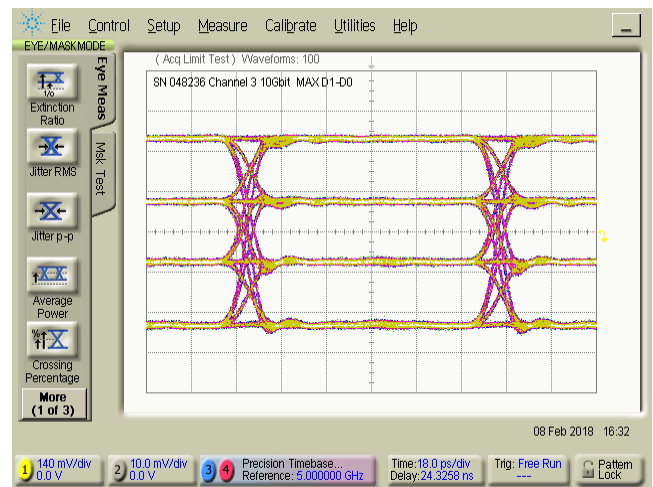
Ch3 @ 25 GBaud



Ch3 @ 20 GBaud



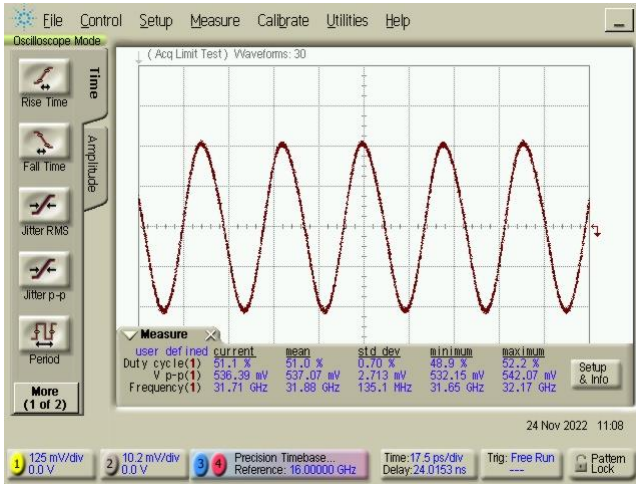
Ch3 @ 14 GBaud



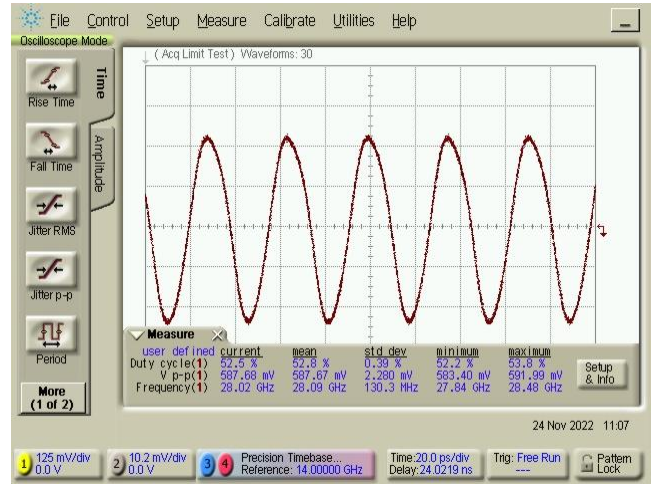
Ch3 @ 10 GBaud



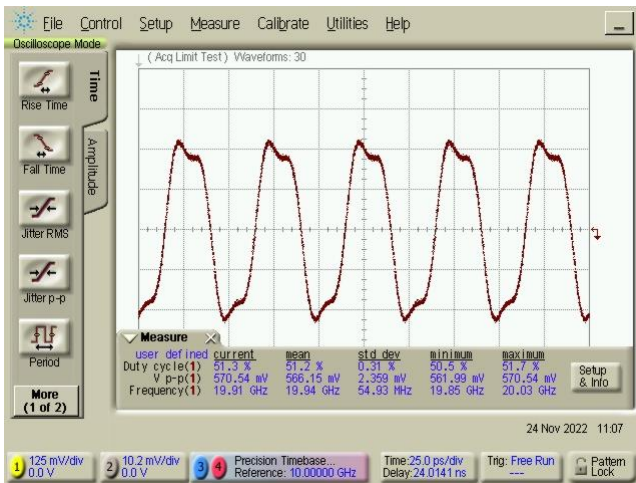
Clock Output Signals



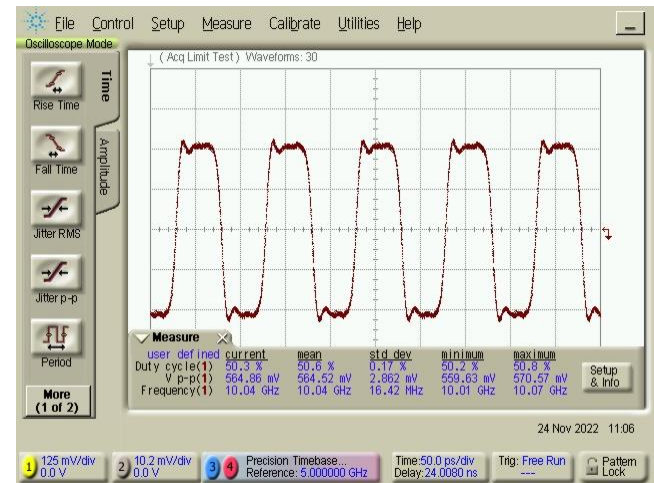
Clock output signal @ 32 Gbps data rate



Clock output signal @ 28 Gbps data rate



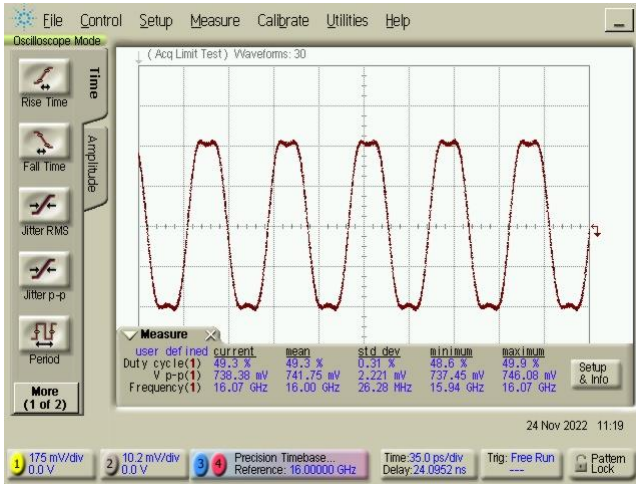
Clock output signal @ 20 Gbps data rate



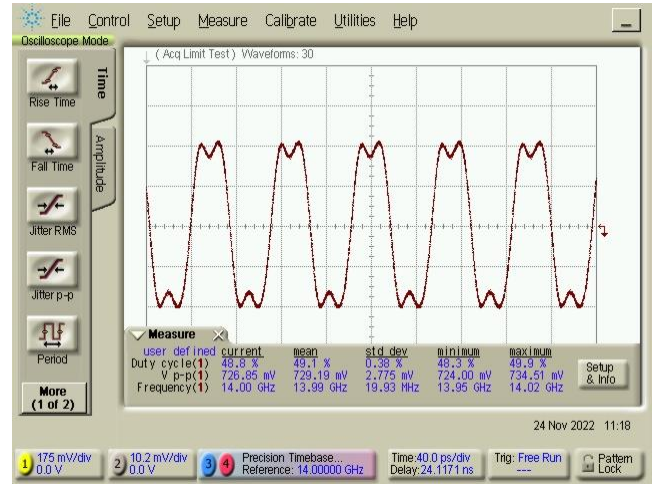
Clock output signal @ 10 Gbps data rate



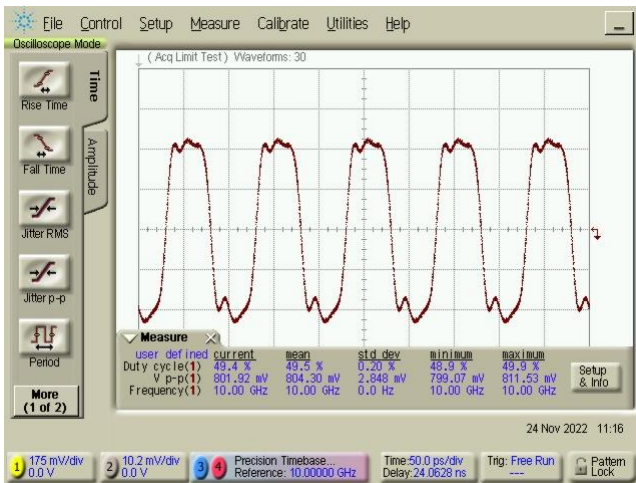
Clock/2 Output Signals



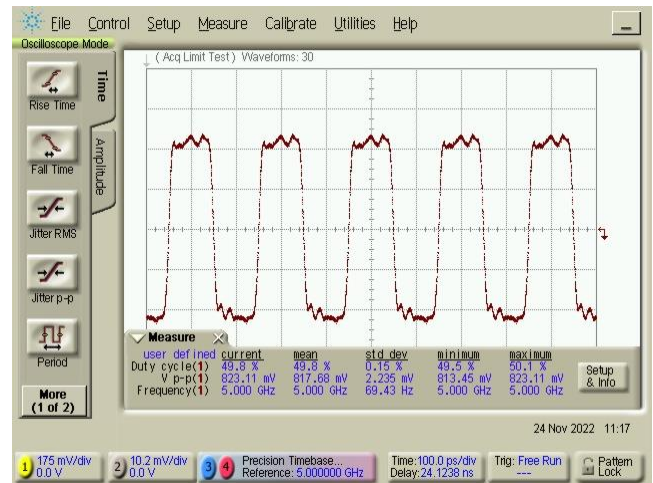
Clock/2 output signal @ 32 Gbps data rate



Clock/2 output signal @ 28 Gbps data rate



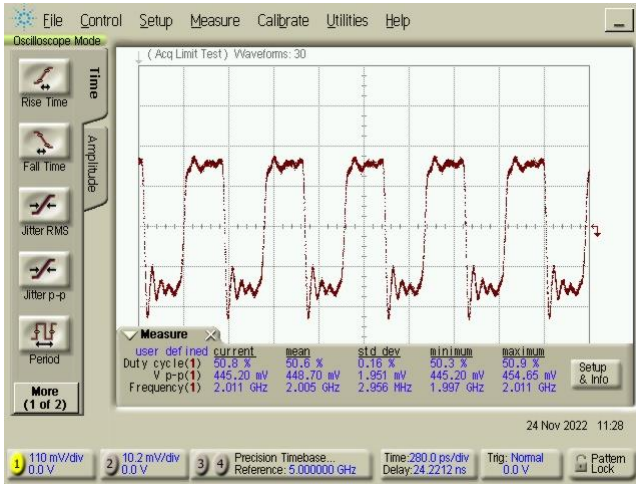
Clock/2 output signal @ 20 Gbps data rate



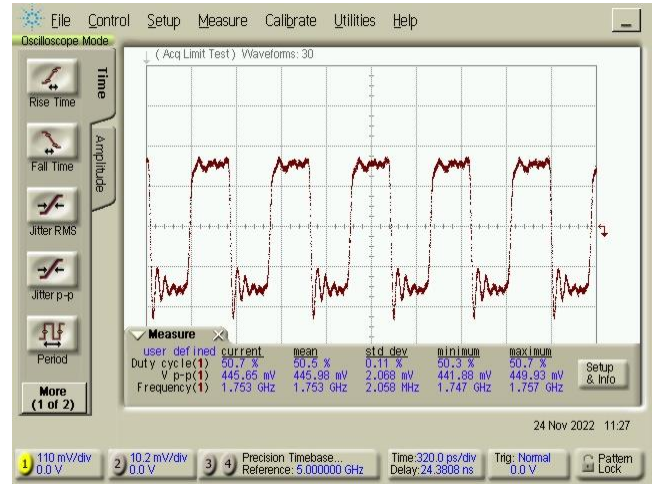
Clock/2 output signal @ 10 Gbps data rate



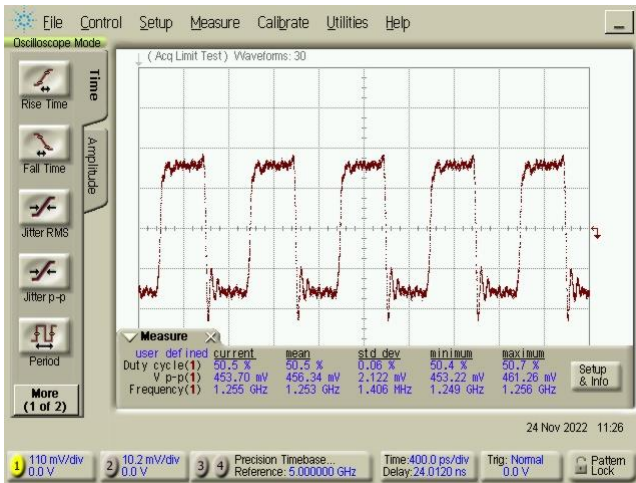
Clock/16 Output Signals



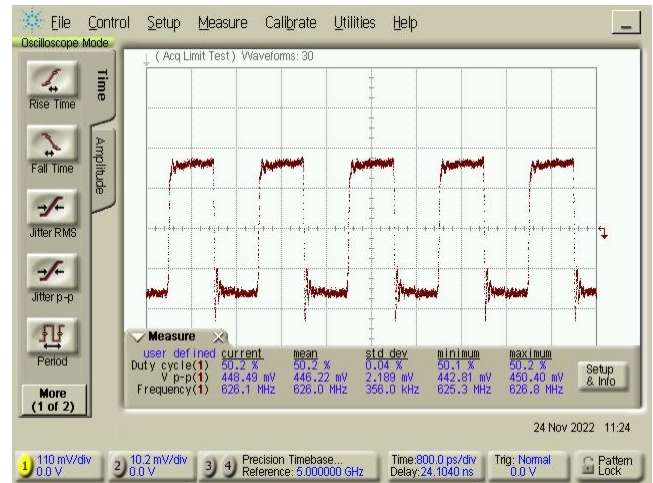
Clock/16 output signal @ 32 Gbps data rate



Clock/16 output signal @ 28 Gbps data rate



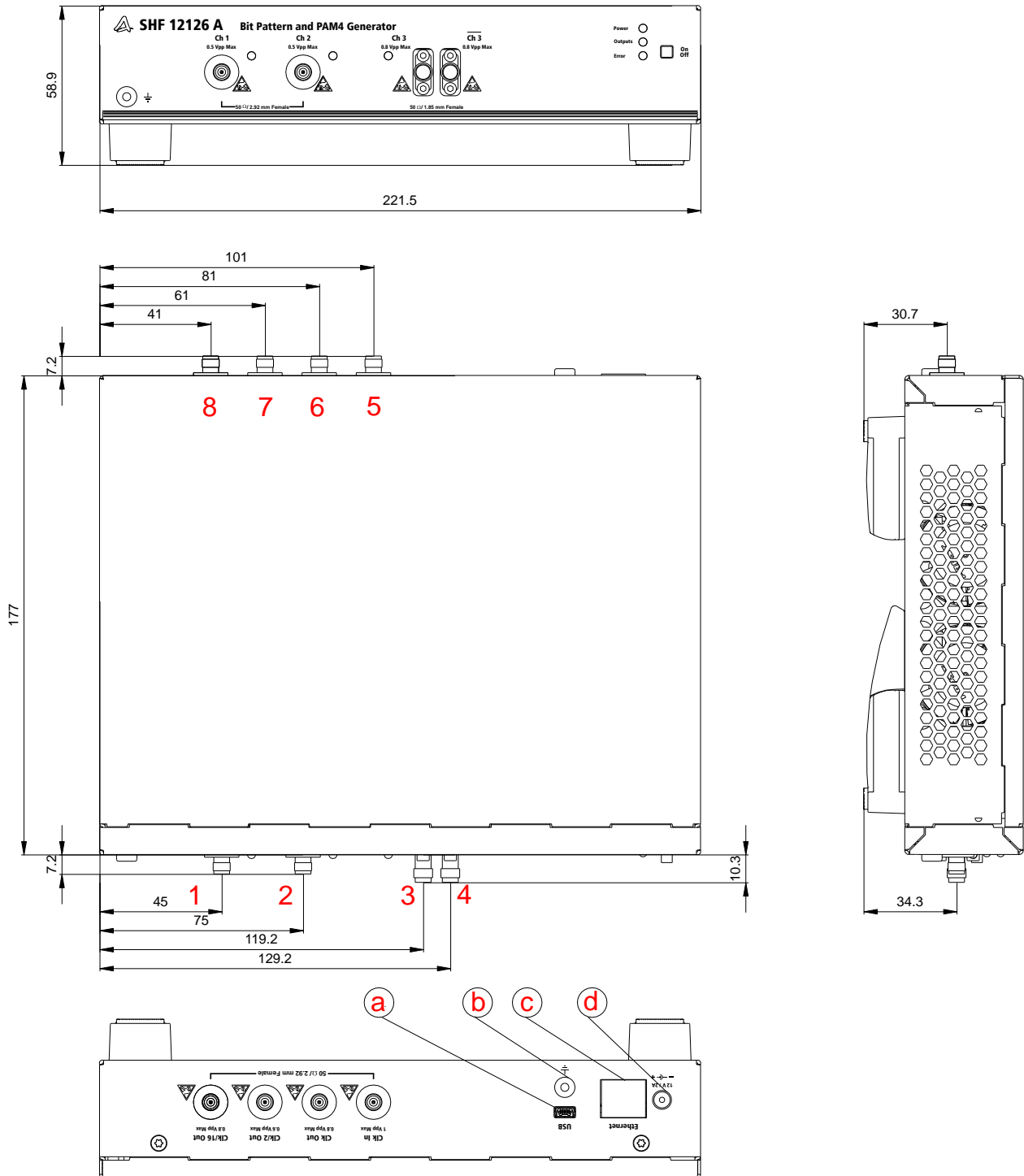
Clock/16 output signal @ 20 Gbps data rate



Clock/16 output signal @ 10 Gbps data rate



Mechanical Drawing



Pos.	Designation	Connector
1	Channel 1	2.92mm (K) Female
2	Channel 2	2.92mm (K) Female
3	Channel 3	1.85mm (V) Female
4	Channel 3	1.85mm (V) Female
5	Clock Input	2.92mm (K) Female
6	Clock Output	2.92mm (K) Female
7	Clock/2 Output	2.92mm (K) Female
8	Clock/16 Output	2.92mm (K) Female

Pos.	Designation
a	USB
b	GND
c	Ethernet
d	Power Supply

all dimensions in mm



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