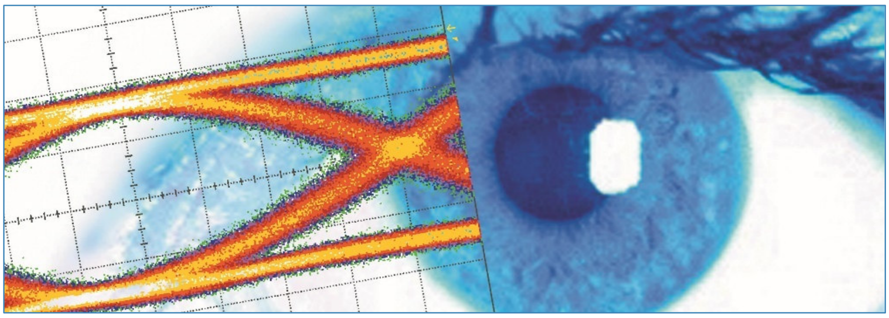


Data Sheet

SHF 12105 A

Bit Pattern Generator

Description

The SHF 12105 A is a synchronized multi-channel 64 Gbps bit pattern generator (BPG). It generates digital bit sequences such as pseudo-random bit sequences (PRBS) or user defined bit patterns.

Operating bit rates from 6 to 64 Gbps, continuously without gaps, is covered by the generated data patterns. Depending on the configuration, the instrument features up to eight independent 64 Gbps differential channels (16 outputs).

The operating bit rate is set by the clock signal from an external clock source. The outputs can operate at both full clock and half clock, e.g., either a 64 GHz or a 32 GHz clock signal can be used for 64 Gbps operation.

The SHF 12105 A can be controlled remotely via an Ethernet interface either by use of the SHF Control Center software provided by SHF or by custom software.

Further to the mode of operation as a multi-channel binary BPG, the functionality can be easily extended by attaching one of SHF's extender heads:

- By using high resolution DAC such as the SHF 6-Bit DAC the easy-to-use graphical user interface enables the generation of arbitrary signals and the system becomes a fully functional AWG.
- In case a multiplexer (MUX) extender head is attached, 120 Gbps NRZ signals can be brought as close as possible to the DUT.
- PAM4 Signal up to 128 GBaud (256 Gbps) can be generated by attaching the PAM4 multiplexer (PAM-MUX).

Features

- Four, six or eight 64 Gbps high quality differential data output channels
- Broadband operation up to an aggregated bit rate of 512 Gbps
- Built-in PRBS patterns and 8 Gbit user pattern per channel to support user defined patterns
- Standard Patterns such as JP03A, JP03B, QPRBS13, PRBS13Q, PRBS31Q, SSPRQ, Transmitter Linearity, SSPR, etc. are included and can be generated with combined signals
- All channels synchronized and independent
- Outputs adjustable up to -10 dB
- All outputs can be used single ended or differential
- Skew adjustment for each differential output
- Bit shift for each differential output
- Frame trigger output
- Error injection capabilities
- Controlled by intuitive graphical user interface SHF Control Center
- Remote control over Ethernet
- DC Offset (available with 'Option HV')
- Clock distribution for trigger signals and DUTs
- Jitter transparent output signals

Applications

The SHF 12105 A is the ideal pattern source for many R&D or production applications which require high speed test data streams for electrical/optical components or transmission systems. The flexible channel configurations, the wide gap-free data rate coverage and the advanced features make this BPG the perfect fit for

- single channel applications,
  e.g., OC-768/STM-256 (using 40G NRZ, DPSK), Fiber Channel®, PCI Express, Serial ATA

- multi-channel applications,
  e.g., OC-768/STM-256 (using 40GBaud QPSK), 100GbE (using 4x32G DP-QPSK)

- multi-level[1] multi-channel applications or
  e.g., for 400G & 1TB DWDM (e.g., using DP-16QAM or 56G PAM4)

- AWG applications
  the SHF 12105 A + DAC combination is a full "remote head" non-interleaved AWG (Arbitrary Waveform Generator) at a speed of up to 64 GBaud

Configurations

The SHF 12105 A can be equipped in a variety of different configurations.

- Oct 64 – Eight differential outputs from 6 to 64 Gbps (sixteen single-ended outputs in total)
- Hex 64 – Six differential outputs from 6 to 64 Gbps (twelve single-ended outputs in total)
- Quad 64 – Four differential outputs from 6 to 64 Gbps (eight single-ended outputs in total)

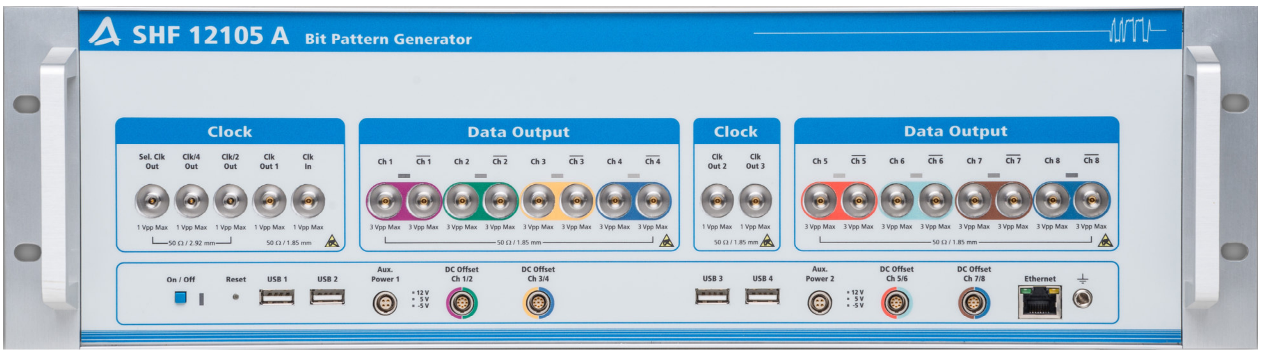


Figure 1 - Front panel of the SHF 12105 A in config. Oct 64 and incl. Opt. AddClock

[1] up to 64 level signals can be generated with the help of one of SHF's external DAC modules.

Options

Option HV - High Output Voltage

Maximum output amplitude of a 64 Gbps data output channel is internally amplified to 2 V.

Figure 2 - SHF 12105 A with extender heads

Option DC Offset – Output Offset Adjust

A DC offset output voltage can be adjusted internally or by applying an external voltage to the front panel connector. This integrated Bias-T is only available with 'Option HV'.

Option AddClock – Two additional full clock outputs

The option AddClock adds two additional full clock outputs, for example to drive the extender heads.

Option Extender SHF C603 A

Two output channels can be multiplexed externally to a data stream up to 120 Gbps by use of a SHF C603 A 2:1 multiplexer. For details please be referred to the data sheet of the SHF C603 A.

Option Extender DAC (e.g., SHF 613 A, SHF 614 C, SHF 615 B)

Operating the SHF 12105 A together with SHF DAC will make the system a 60 GSa/s Arbitrary Waveform Generator (AWG). The vertical resolution is depending on the number of BPG outputs and DAC inputs bits. Example applications include PAM4 with pre-emphasis. For details, please refer to the data sheet of the DACs and the chapters AWG & User-Defined Waveform Capabilities and PAM4 Mode in this document.

Option Extender SHF 616 B

Four output channels can be multiplexed and combined externally to a PAM4 data stream up to 128 GBaud by use of a SHF 616 B. For details please be referred to the data sheet of the SHF 616 B.

Block Diagram

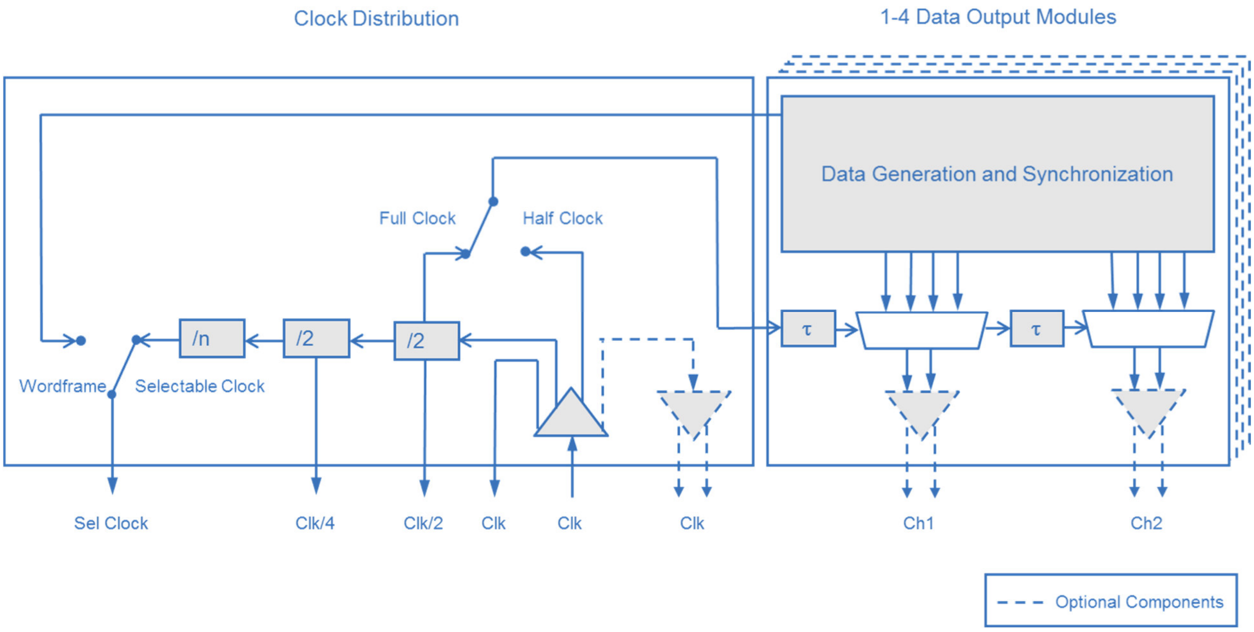


Figure 3 - Block diagram of the SHF 12105 A

The pattern generator consists of up to 32 16 Gbps pattern generation blocks which are synchronized to each other. Four outputs of the pattern generation blocks are 4:1 multiplexed to generate one 64 Gbps data output steam. Each data output module includes two data output channels consisting of a delay line for skew control, a 4:1 MUX and optional amplifiers (Option HV) to raise the output amplitude to 2 V.

The clock distribution section processes the incoming clock signal to generate the clock out, clock/2 out, clock/4 out, selectable clock out and word frame signals. With option AddClock, two additional full clock outputs are provided, for example to drive the optional available extender heads. Internally the SHF 12105 A works in half clock mode. To enable full clock operation, the incoming clock is divided by 2 by selecting full clock mode in the software.

Specifications

Absolute Maximum Ratings

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on RF Clock Input Port	V	V_{DCin}	-10		+10	AC coupled input
External DC Voltage on RF Clock Output Ports	V	V_{DCin}	-10		+10	AC coupled outputs
External DC Voltage on RF Data Output Ports	V	V_{DCin}	-10 none[2] none[2]		+10 none[2] none[2]	with Option HV with Option HV & Offset without Option HV
External DC Voltage on DC Offset Ports	V	$V_{Off,Ext}$	-4		+4	with Option HV & Offset
External DC Current on DC Offset Ports	mA	$A_{Off,Ext}$	-110		+110	with Option HV & Offset

2 DC-coupled RF data outputs must not be charged by an external DC voltage

64 Gbps Data Output Specifications (without Option HV)

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Minimum Bit Rate	Gbps			4	6[3]	
Maximum Bit Rate	Gbps		64	65		
Maximum Output Level	mV	V_{out}	650 1300	730 1460	800 1600	Single ended Differential Eye amplitude; Adjustable by up to -10 dB; DC coupled ground referenced CML interface
Output DC Level	mv	V_{DCOut}	-400	-500	-600	@ 50 Ω load; constant when adjusting output amplitude
Jitter (RMS) on scope display[4]	fs	J_{RMS}		500	650	
Jitter (RMS) deconvolved[5]	fs	J_{RMS}		460	620	
Jitter (PP)	ps	J_{PP}		2.5	4	
Rise/Fall Time on scope display[6]	ps	t_r/t_f		9	11	20%...80%
Rise/Fall Time deconvolved[7]	ps	t_r/t_f		8.2	10.4	20%...80%
Crossing	%		46	50	55	
Duty Cycle	%			50		of two consecutive eyes; software adjustable
Skew Control	ps		-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew	ps				3	at 64 Gbps with skew control set to 0 ps
Connector Type	Ω			50		1.85 mm (V); female connector

[3] By use of the "Bitrate Divider" – function the minimum output bit rate can be reduced further down to 1.5 Gbps (see page 14)
[4] Measured with a 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1
[5] Calculation based on typical jitter from oscilloscope data sheet: $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$
[6] Measured with a 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1
[7] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

64 Gbps Data Output Specifications (with Option HV)

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Minimum Bit Rate	Gbps			4	6[8]	
Maximum Bit Rate[9]	Gbps		64	65		
Maximum Output Level	mV	V_{out}	2000 4000			Single ended Differential Eye amplitude; AC coupled Adjustable by up to -10 dB
Jitter (RMS) On scope display[10]	fs	J_{RMS}		500 600	650 1000	$V_{out} \geq 500$ mV $V_{out} < 500$ mV
Jitter (RMS) Deconvolved[11]	fs	J_{RMS}		460 570	620 980	$V_{out} \geq 500$ mV $V_{out} < 500$ mV
Jitter (PP)	ps	J_{PP}		2.5 3	4 5	$V_{out} \geq 500$ mV $V_{out} < 500$ mV
Rise/Fall Time On scope display[12]	ps	t_r/t_f		9 10	11 12	20%...80% $V_{out} \geq 500$ mV $V_{out} < 500$ mV
Rise/Fall Time Deconvolved[13]	ps	t_r/t_f		8.2 9.3	10.4 11.4	20%...80% $V_{out} \geq 500$ mV $V_{out} < 500$ mV
Crossing	%		46 40		54 60	$V_{out} \geq 1000$ mV $V_{out} < 1000$ mV
Duty Cycle	%		47	50	53	of two consecutive eyes; software adjustable
Skew Control	ps		-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew	ps				3	at 60 Gbps with skew control set to 0 ps
Connector Type	Ω			50		1.85 mm (V); female connector

[8] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 1.5 Gbps (see page 14)

[9] Measured with PRBS 2^{31}-1, BER < 1e-12

[10] Measured with Tektronix DSA8300 with 70 GHz sampling head and phase reference triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[11] Calculation based on typical jitter from oscilloscope data sheet: $J_{RMS\,deconvolved} = \sqrt{(J_{RMS\,measured})^2 - (J_{RMS\,oscilloscope})^2} = \sqrt{(J_{RMS\,measured})^2 - (200\,fs)^2}$

[12] Measured with a 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[13] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\,deconvolved} = \sqrt{(t_{r\,measured})^2 - (t_{r\,oscilloscope})^2} = \sqrt{(t_{r\,meas.})^2 - (3.68\,ps)^2}$

DC Offset Specifications (with Option DC Offset)

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
DC Offset Voltage (internal supply)	V	$V_{Off,Int}$	-2.5[14,15]		+2.5[14,15]	software adjustable; @ load current = 50 mA (R_{load} = 50 Ω)
DC Offset Current (internal supply)	mA	$A_{Off,Int}$	-50[14,15]		+50[14,15]	
DC Offset Voltage (external supply)	V	$V_{Off,Ext}$	-3.5[15,16]		+3.5[15,16]	applied to "DC Offset"-connector
DC Offset Current (external supply)	mA	$A_{Off,Ext}$	-100[15,16]		+100[15,16]	

[14] DC Offset voltage on the RF output port varies with the external load resistance; internal bias-t resistance is ~6.4 Ohm

[15] Consideration of the application note „Impact of Bias Tees on Communication Signals" from www.shf-communication.com recommended

[16] DC Offset voltage on the RF output port varies with the external load resistance; internal bias-t resistance is ~3.9 Ohm

64 Gbps Data Output Specifications (with Option HV)

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input Clock Output Optional Clock Output Clock/2 Clock/4 Sel. Clock Output	Ω			50		Connector Type 1.85 mm (V) female connector 1.85 mm (V) female connector 1.85 mm (V) female connector 2.92 mm (K) female connector 2.92 mm (K) female connector 2.92 mm (K) female connector
Minimum Clock Input Frequency	GHz	f_{in_clock}			3 6	half clock mode[17] full clock mode[17]
Maximum Clock Input Frequency	GHz	f_{in_clock}	32 64			half clock mode[17] full clock mode[17]
Input Level	mV_{pp}	V_{in_clock}	630		1000	AC coupled
Output Level Clock Clock/2 Clock/4 Selectable Clock	mV_{pp}	V_{out_clock}	 450 500 500 250	 700 800 800 450	 1000 1000 1000 600	 AC coupled, @ P_{in}=0 dBm AC coupled AC coupled AC coupled
Output Frequency Clock Clock/2 Clock/4 Selectable Clock Word Frame Trigger	 GHz GHz GHz GHz MHz	f_{out_clock}	 3 1.5 0.75 0.006		 64 32 16 16 500	 same as input frequency half of input frequency quarter of input frequency input frequency/N (N= 4, 8, 16, 32, 64, 128, 256, 512, 1024)

[17] The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The outputs can operate at both full clock and half clock, so e.g., a 20 GHz or a 40 GHz signal is required for 40 Gbps operation.

General Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Weight	kg	m			45	Fully Equipped
Dimensions	mm	WxDxH				600x480x150
Operating Temperature	°C	T_{OP}	10		35	
Storage Temperature	°C	T_{ST}	-20		70	@ 95 % RH max.
Working Humidity	%		20		90	Non condensing

Rear Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Power Supply	V	U	100 210	110 230	135 240	50…60 Hz
Power Consumption	W	P			400	Max. Configuration @110-230 V
Power Supply Connector						IEC-60320 C14
Common Ground Connector						4 mm socket
Network Connectors						RJ-45 Ethernet

Front Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
DC Offset Connectors						Lemo EPZ.0B.309.HLN
Auxiliary Power Outputs	V	U		–5 +5 +12		Max. 1.5 A Max. 1.5 A Max. 1.7 A
Auxiliary Power Connectors						Lemo EPG.OB.304.HLN
Common Ground Connector						4 mm socket
Network Connector						RJ-45 Ethernet

Patterns

Pattern	Polynomial	Reference
PRBS 2^7-1	$G(x) = 1 + x^6 + x^7$	
PRBS 2^9-1	$G(x) = 1 + x^5 + x^9$	ITU-T O.150 5.1 IEEE 802.3 68.6.1
PRBS 2^{10}-1	$G(x) = 1 + x^7 + x^{10}$	
PRBS 2^{11}-1	$G(x) = 1 + x^9 + x^{11}$	ITU-T O.150 5.2
PRBS 2^{13}-1	$G(x) = 1 + x + x^2 + x^{12} + x^{13}$	IEEE 802.3 94.3.10.8
PRBS 2^{15}-1	$G(x) = 1 + x^{14} + x^{15}$	ITU-T O.150 5.3
PRBS 2^{20}-1	$G(x) = 1 + x^3 + x^{20}$	
PRBS 2^{23}-1	$G(x) = 1 + x^{18} + x^{23}$	ITU-T O.150 5.6

User Pattern Capabilities

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
User Pattern Memory size		Gbit			8	Per channel
User Pattern Granularity		Bit		512		For more details see Chapter User Pattern Capabilities

Example Patterns Provided

Pattern	Polynomial
SSPR[18]	OIF-CEI-03.1 Annex 2.D.2
JP03A[18]	IEEE 802.3 94.2.9.1
JP03B[18]	IEEE 802.3 94.2.9.2
QPRBS13[18]	IEEE 802.3 94.2.9.3
Transmitter Linearity[18]	IEEE 802.3 94.2.9.4
PRBS13Q[18]	IEEE 802.3 120.5.11.2.1
SSPRQ[18]	IEEE 802.3 120.5.11.2.3
Square Wave Quaternary[18]	IEEE 802.3 120.5.11.2.4

[18] Is a PAM4 pattern and can be generated by combining the BPG output signals with a DAC

Output Adjustment Capabilities

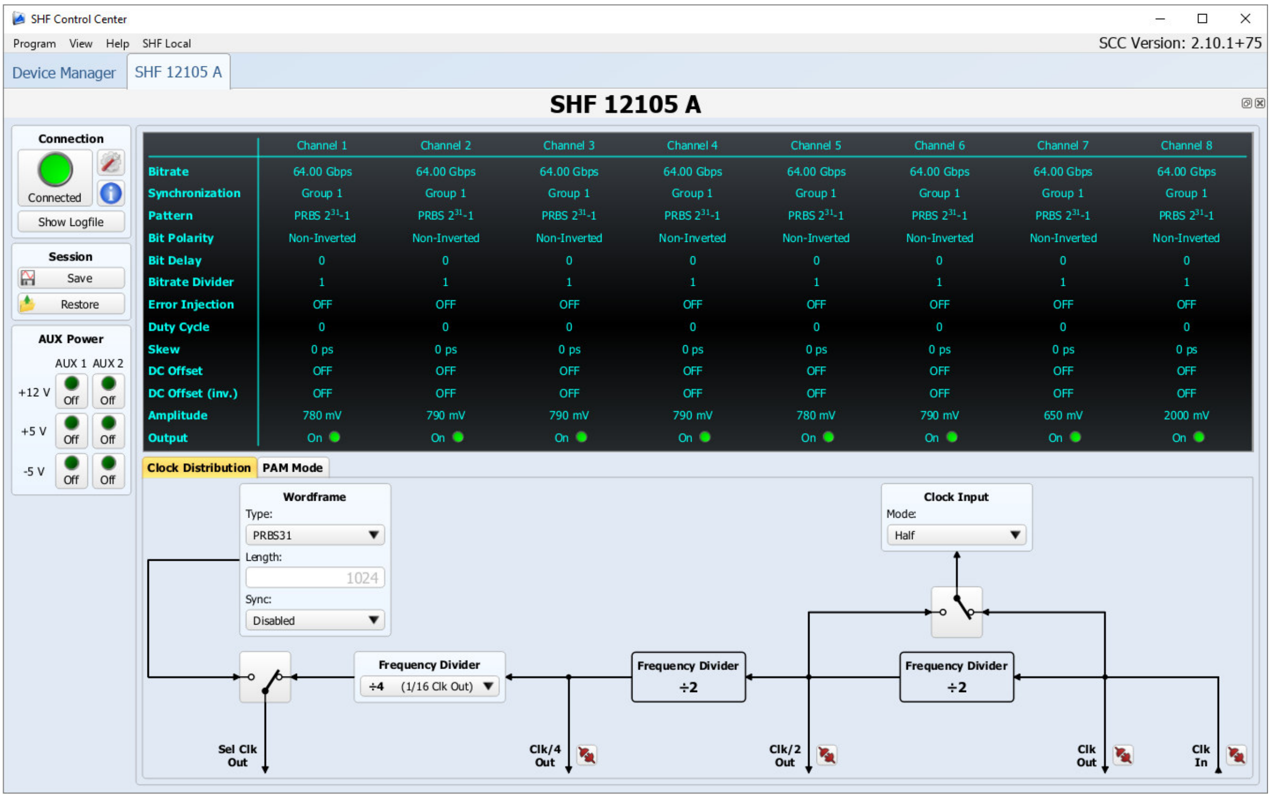


Figure 4 - SHF Control Center window for the SHF 12105 A

<u>Bit Rate</u>

The bit rate of all outputs is continuously adjustable by a single external clock signal.

<u>Clock Input</u>

In full clock mode, the BPG will need a 64 GHz clock signal to generate a 64 Gbps data signal. In half clock mode, a 32 GHz clock signal will be needed to generate a 64 Gbps data signal. Internally the SHF 12105 A operates in half clock mode. When selecting full clock mode, a divider is used to generate the half clock needed internally from the externally provided full clock.

<u>Selectable Clock</u>

The selectable clock output provides a divided clock signal derived from the clock input signal. A divider ratio of 1/n with n = 4, 8, 16, 32, 64, 128, 256, 512 or 1024 can be selected.

<u>Word Frame</u>

To display the pattern trace on the oscilloscope the word frame signal can be used to trigger the oscilloscope. The word frame can be set to one of the PRBS word lengths or to a user defined value.

<u>AUX Power</u>

This control is needed to enable the aux power voltages provided on the front panel.

<u>Group Synchronization</u>

The data outputs can be grouped. All data outputs of one group are bit synchronized to enable AWG functionality together with a DAC, cross talk measurements and PRBS conformed multiplexing.

Pattern Type

Pre-defined PRBS patterns from 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{13}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 and 2^{31}-1 are available. User-defined binary patterns can be loaded from file in single column text file format. All PRBS and user patterns can be assigned individually to each channel.

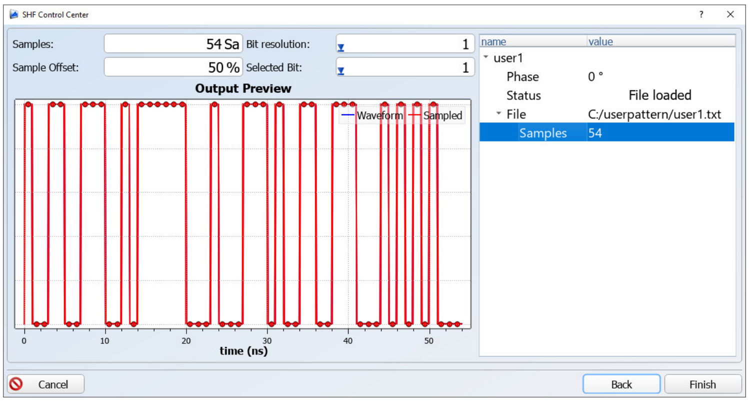


Figure 5 - SHF Control Center upload GUI for binary user patterns

Pattern Polarity

All patterns can be inverted by use of this function

Bit Delay / Bit Shift

In case two or more PRBS patterns of the same length are selected it is possible to control the starting point of each bit sequence (in 1 bit steps up to the total PRBS length).

Bit Rate Divider

The ‘bit rate divider’ is a software function to transmit the same bit multiple times and thus reduces the data rate (divided by 2 or 4).

Error Injection

For testing purposes, a fixed error rate can be added to the date stream.

Duty Cycle

The duty cycle of two consecutive eyes/bits is automatically set to 50%. However, in case the application requires a modification or a further optimization, this could be done with a few clicks.

Skew

The timing of every output channel can be adjusted individually in 0.1 ps steps (please see chapter Skew Control Function for more details).

DC Offset

The DC offset of a high voltage RF output port can be switched between an internal generated DC voltage and an external supplied DC voltage.

Amplitude

The output amplitude of each channel is adjustable independently.

Output On/Off

The outputs can be turned on and of individually. During and after start up these are turned off to prevent any damage to the DUTs attached.

AWG & User-Defined Waveform Capabilities

The SHF 12105 A and a SHF DAC are not just two discrete modules connected together. The SHF Control Center software provides a variety of features which can be used in case a SHF DAC is connected to the BPG.

The software offers an interface for user defined signals by use of the Python programming language or the user may load externally generated signals from software like Matlab. A set of commonly used signals is provided with the SHF Control Center. The software only needs to know which BPG output is physically connected to which DAC input. The SHF Control Center will calculate the user pattern for each channel in a way that the DAC generates the desired arbitrary signal.

The best results are achieved with the SHF 614 C 6-Bit DAC and a SHF 12105 A with at least 6 channels as this architecture provides a vertical resolution of 2^6=64 steps reducing quantization errors.

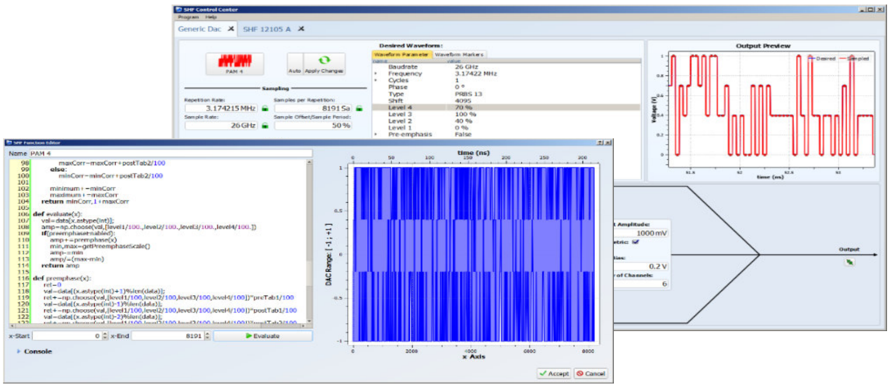


Figure 6 – Arbitrary Waveform Generator Interface

The SHF 12105 A has 8 Gbit of built-in user pattern memory for each output channel. Due to the memory width of 512 bits, there is a granularity requirement of 512 bits which can be overcome by repeating the pattern until the least common multiple of the pattern length and 512 is met.

The SHF Control Center software supports creating, editing and converting different formats of user pattern files to be used with the SHF 12105 A. It will handle all user patterns.

For example, it will repeat automatically user patterns not fulfilling the granularity requirement until the granularity of 512 is met. For patterns up to 16 Mbit this is always possible. Patterns larger than 16 Mbit have to fulfill the following prerequisites:

Pattern length up to	Pattern length has to be a multiple of
16 Mbit	1
32 Mbit	2
64 Mbit	4
128 Mbit	8
256 Mbit	16
512 Mbit	32
1 Gbit	64
2 Gbit	128
4 Gbit	256
8 Gbit	512

Two BPG output channels (1&5, 2&6, 3&7 and 4&8) share one common memory controller, so that their patterns need to be of the same length or need to be repeated until the least common multiple is met. For most applications like PAM, AWG, DACs and Muxes the patterns need to be of the same length anyway.

PAM4 Mode

For binary data a BPG has obvious advantages over an AWG as the bit/baud rate always equals the sample rate (no fractional oversampling) and as logical pattern generation techniques can be applied without utilizing a rather slow and small memory. With the SHF 12105 A these advantages do also apply to a BPG/DAC combination when generating PAM4 signals where even the individual eye heights or pre-emphasis can be achieved and adjusted on the fly without waiting for the memory to be loaded and by still transmitting very long patterns (e.g., PRBS 2^{31}-1 or PRBS31Q).

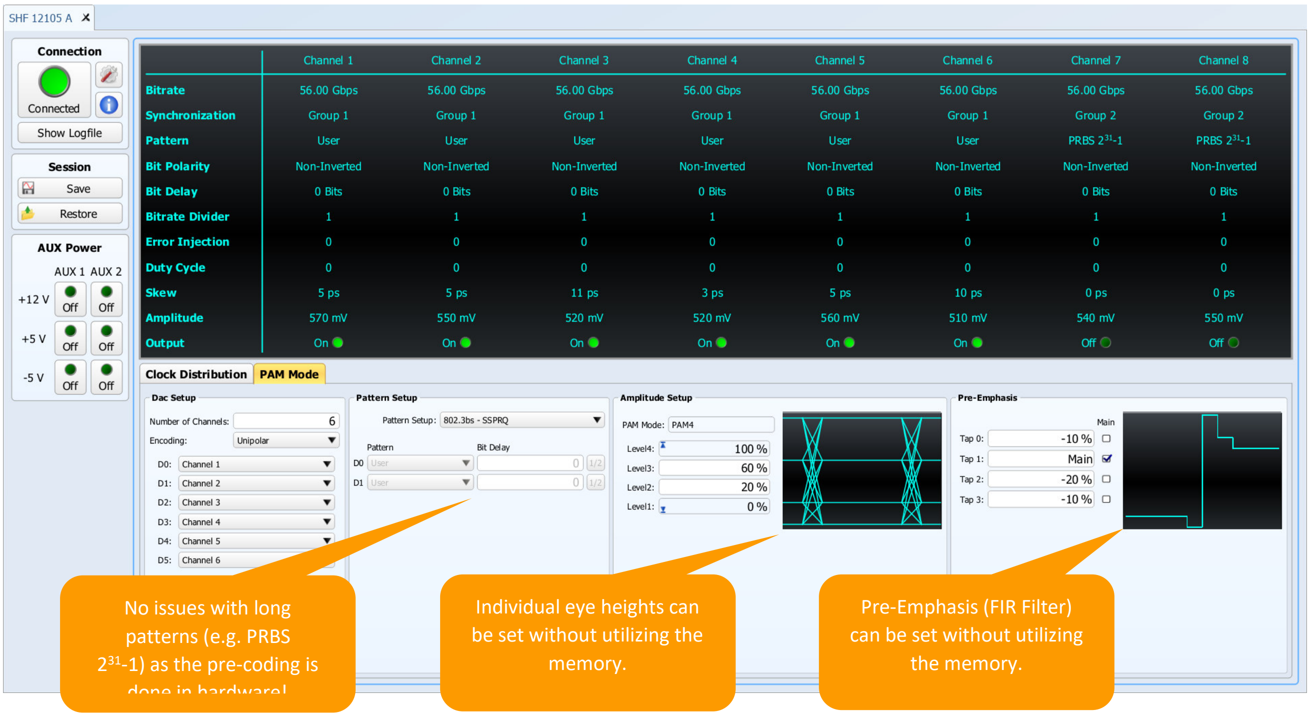


Figure 7 - SCC in PAM Mode

Jitter Transparency

By modulating the clock input signal with a low frequency signal, one can quickly and easily create jittered clock signals with complex properties to drive the SHF 12105 A to emulate jittered high speed NRZ data (Fig.8). Adding a DAC gives the possibility to generate jittered PAM4 signals (Fig. 9 & 10), ensuring the setup is ready for the increase in modulation orders and lane rates for the anticipated serial data protocols to come. For more information see Application Note “Creating Complex Jittered Test Patterns” on SHFs web page.

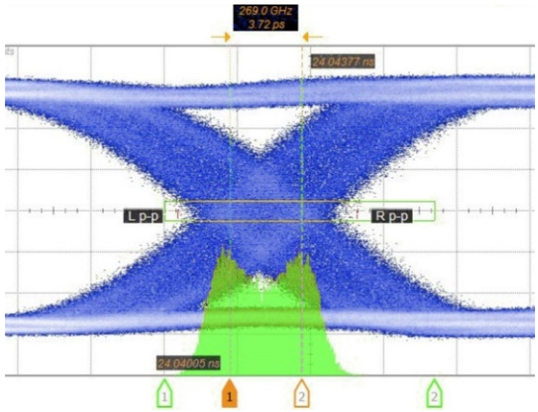


Figure 8 – Sine-jittered data output signal from SHF 12105 A

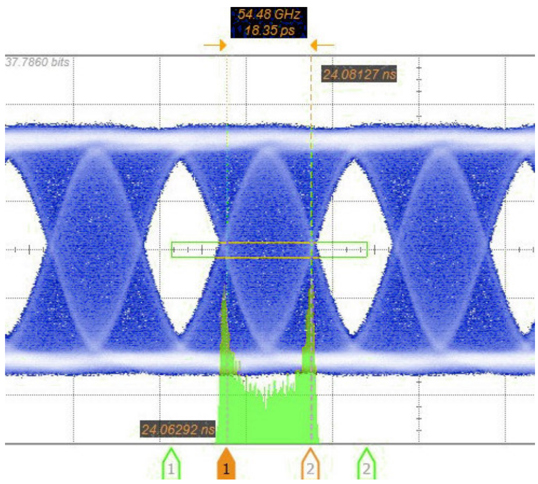


Figure 9 – Sine-jittered data output signal (MSB) from a SHF DAC

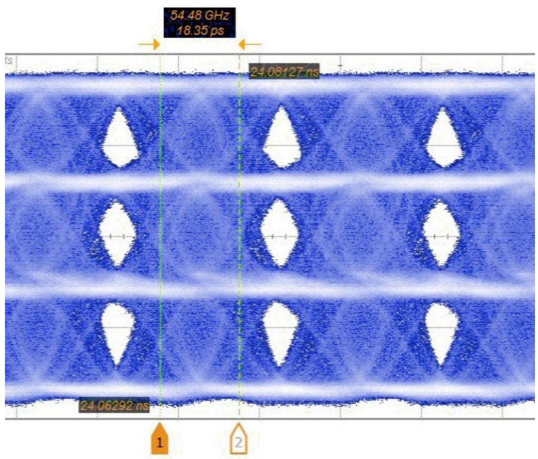


Figure 10 – Sine-jittered data output signal (PAM4) from a SHF DAC

Skew Control and Bit Delay Functions

The skew control and bit delay functions allow adjustment of the channel timing relative to each other. As a result, timing delays between individual output channels can be adjusted in 0.1 ps steps (using skew control), as well as over many integer bit periods (using the bit delay function). The figures below show the SHF Control Center with this feature and an example of delay between two channels for skew within a bit and more than one bit.

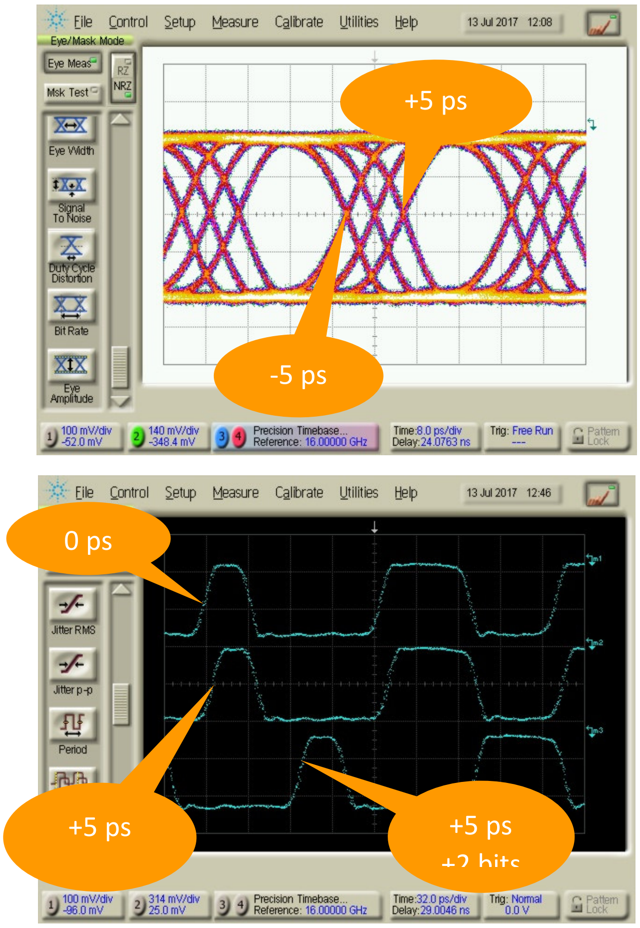


Figure 11 – Skew control & integer bit delay

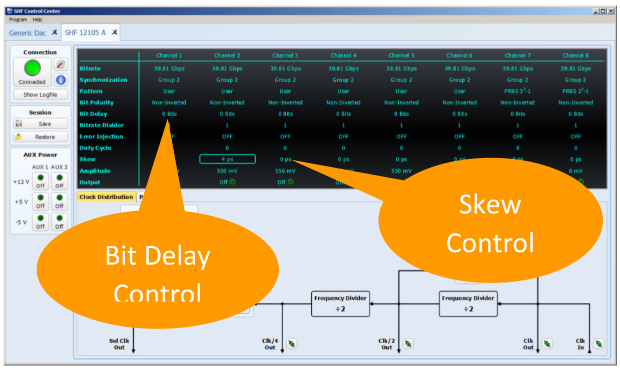
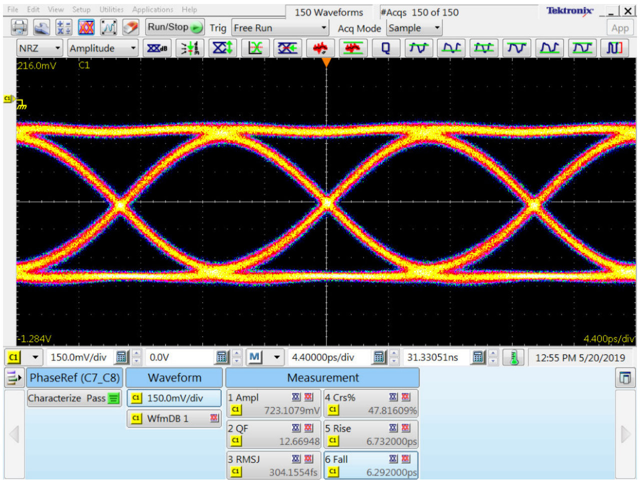


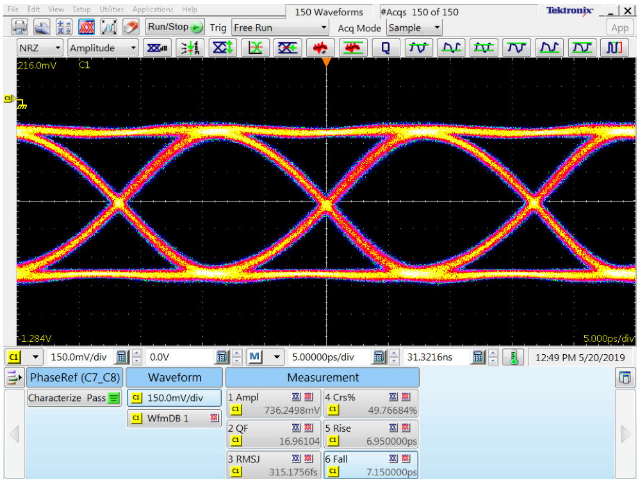
Figure 12 – Bit delay and skew control software representation

Typical Output Waveforms

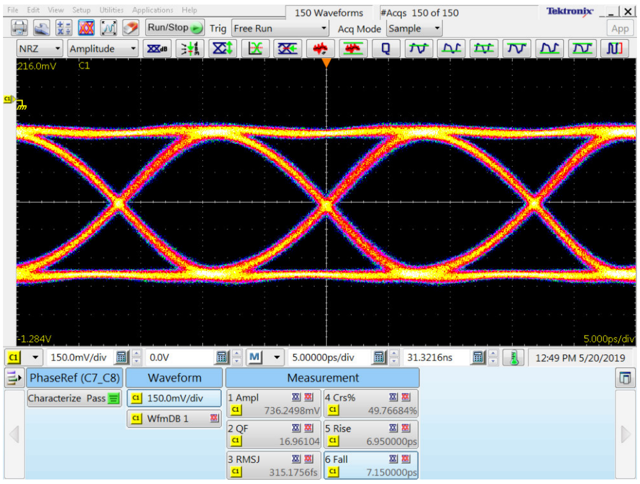
Data Output Signals (without Option HV)



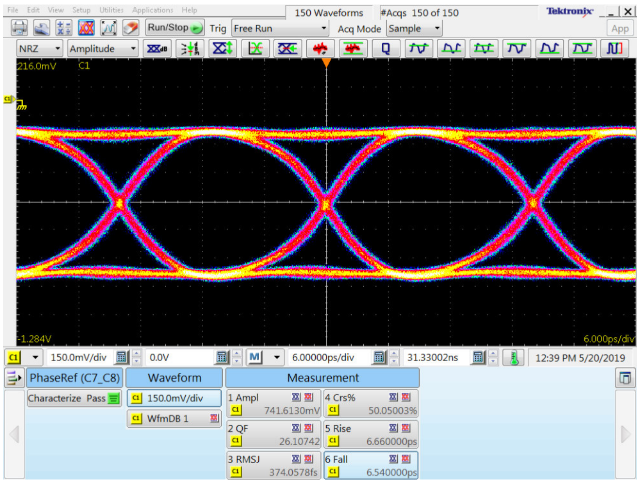
68 Gbps output at maximum output level



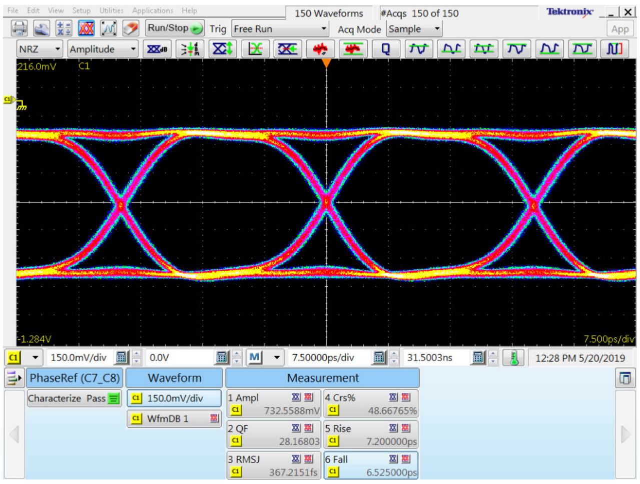
64 Gbps output at maximum output level



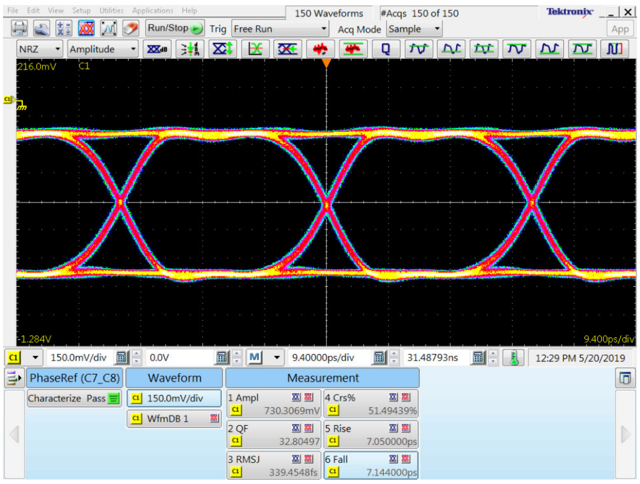
60 Gbps output at maximum output level



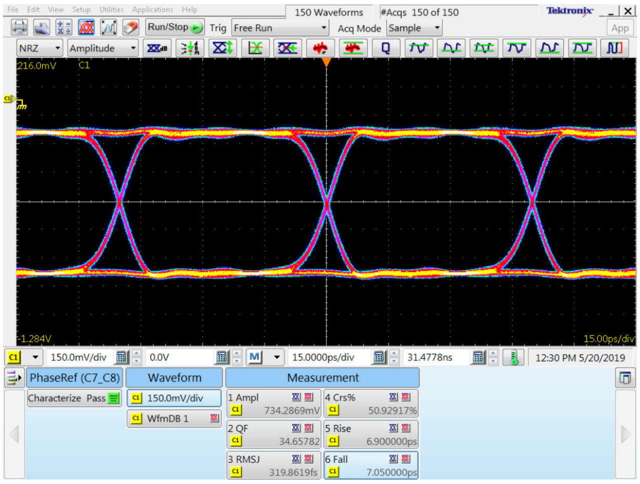
50 Gbps output at maximum output level



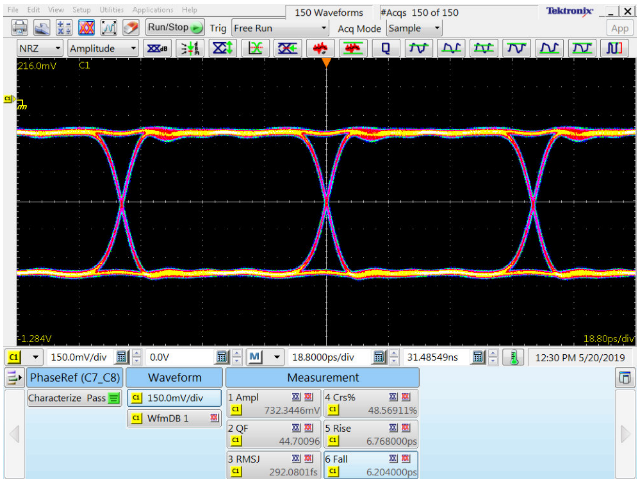
40 Gbps output at maximum output level



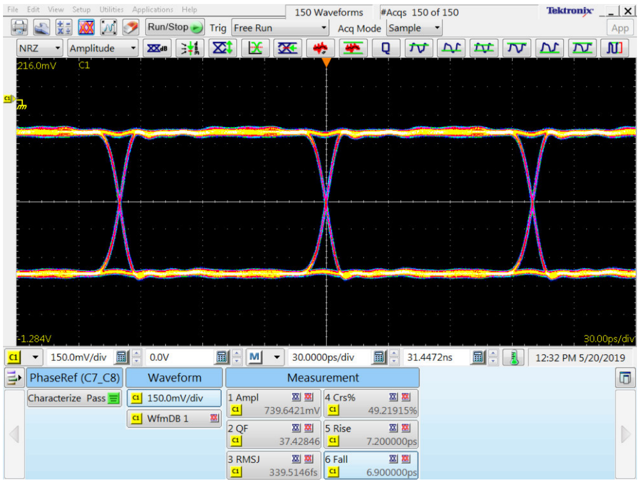
32 Gbps output at maximum output level



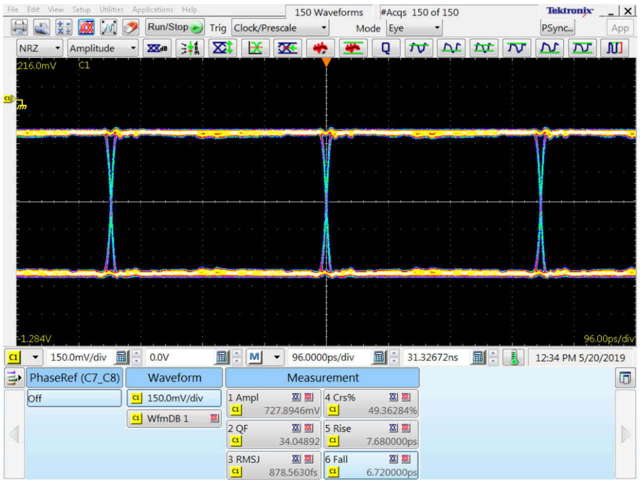
20 Gbps output at maximum output level



16 Gbps output at maximum output level

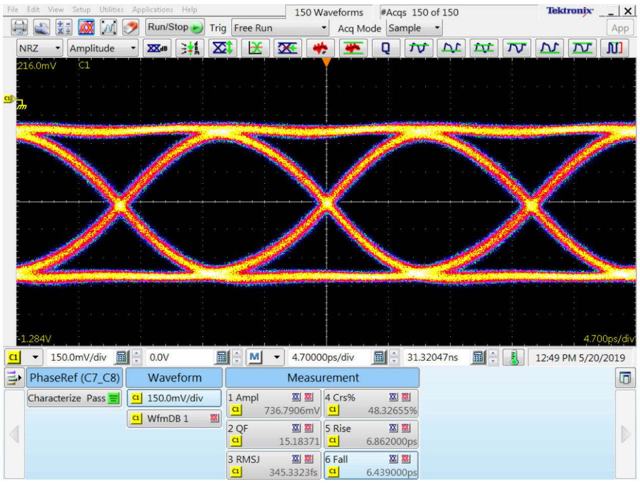


10 Gbps output at maximum output level

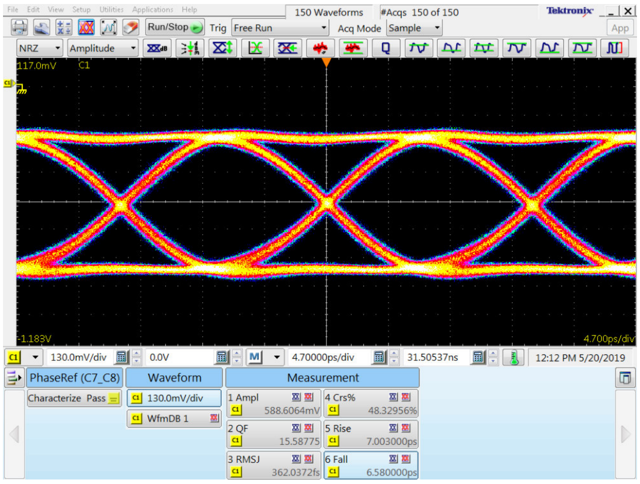


3 Gbps output at maximum output level

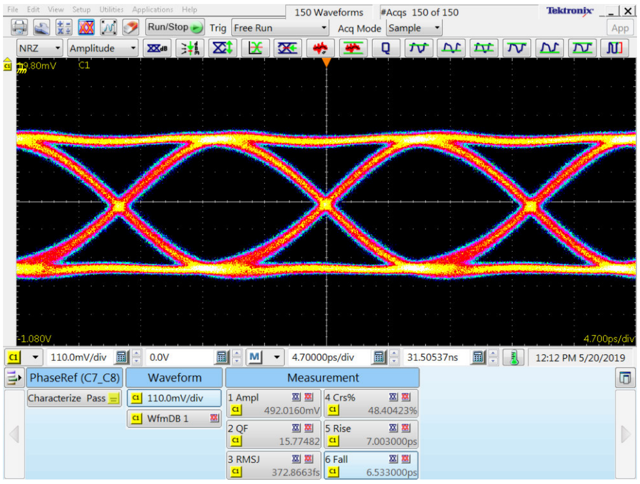
Data Output Signals - Amplitude Adjustment (without Option HV)



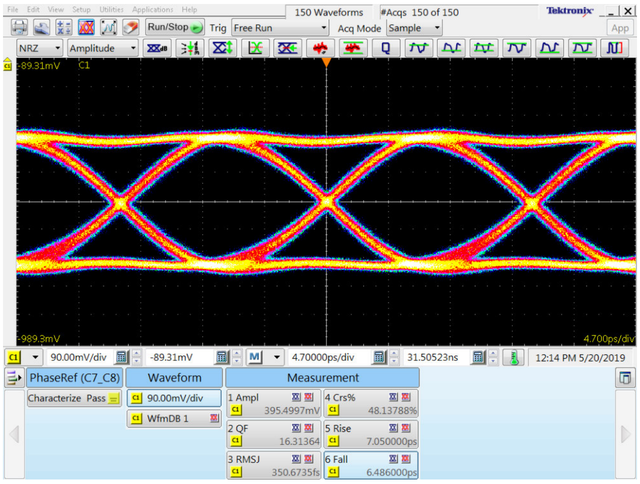
64 Gbps output at 730 mV



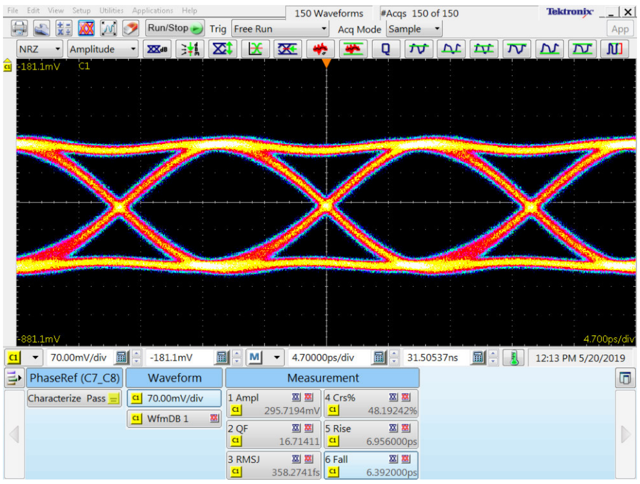
64 Gbps output at 600 mV



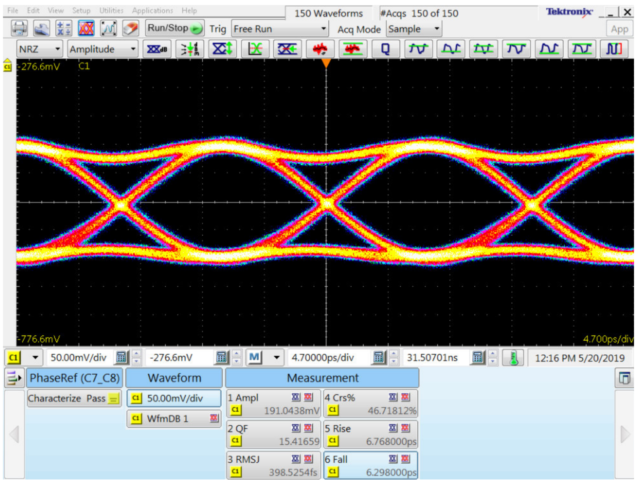
64 Gbps output at 500 mV



64 Gbps output at 400 mV

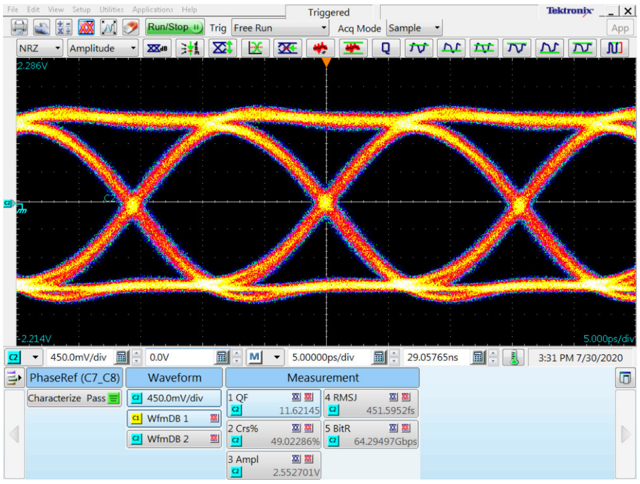


64 Gbps output at 300 mV

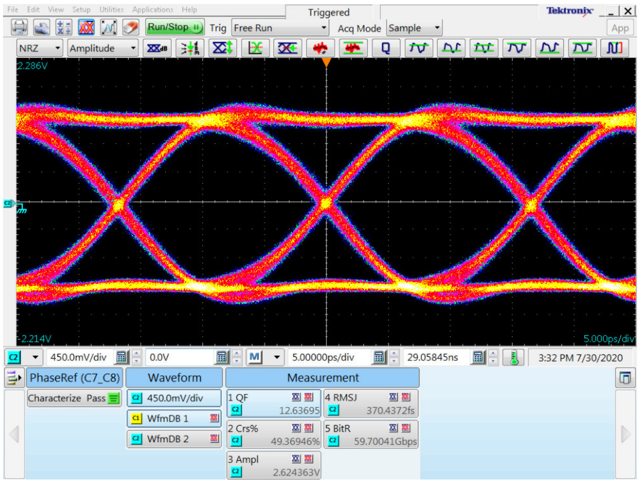


64 Gbps output at 200 mV

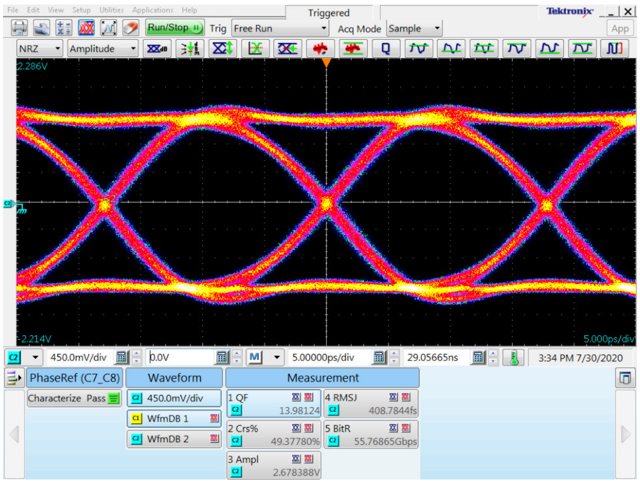
Data Output Signals (with Option HV)



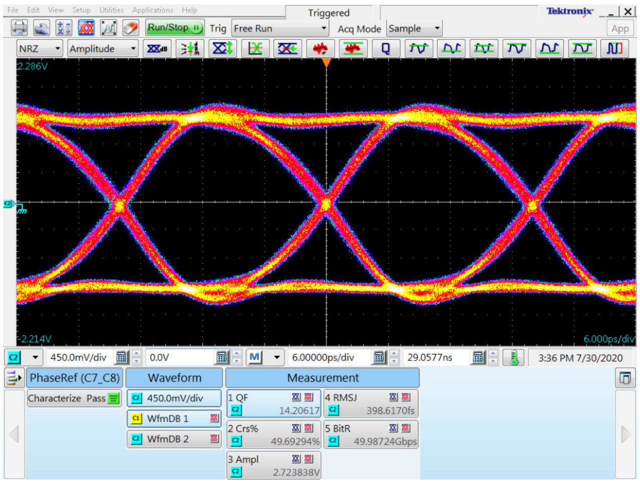
64 Gbps output at maximum output level



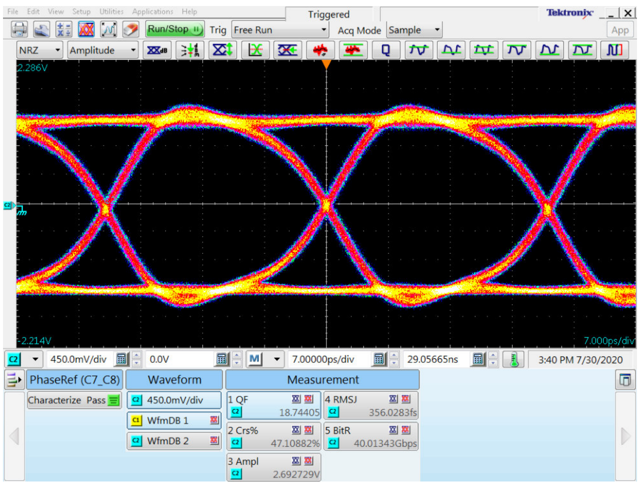
60 Gbps output at maximum output level



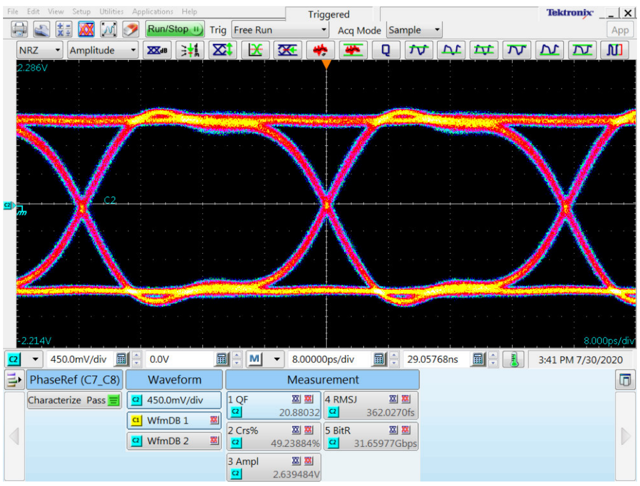
56 Gbps output at maximum output level



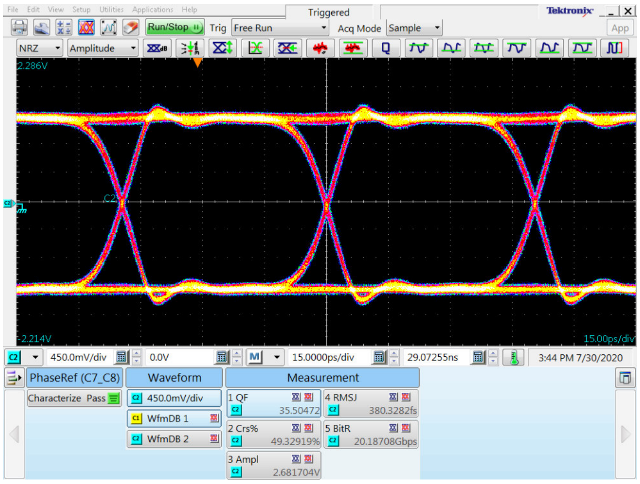
50 Gbps output at maximum output level



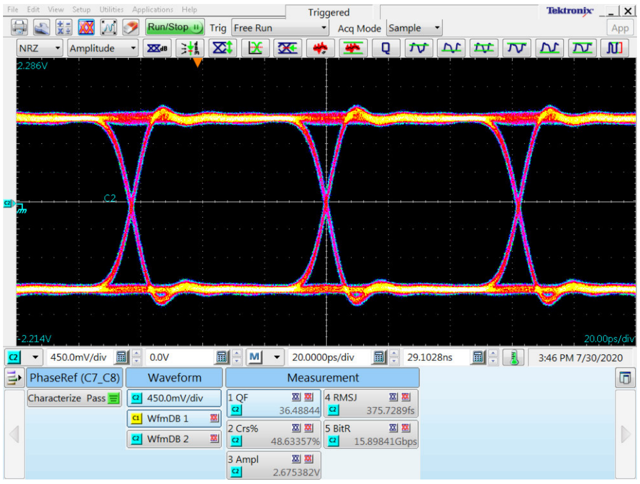
40 Gbps output at maximum output level



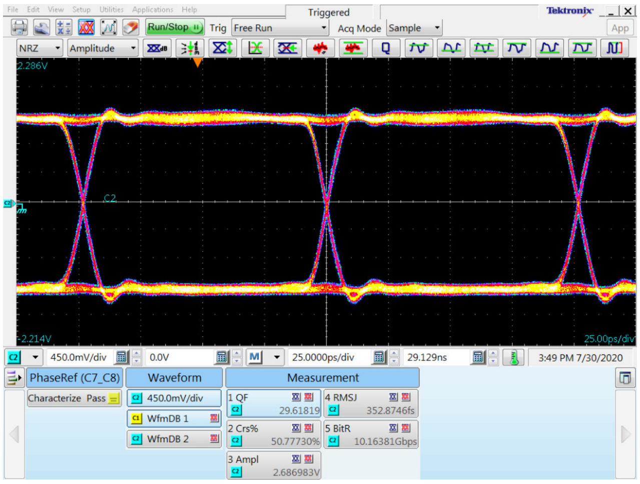
32 Gbps output at maximum output level



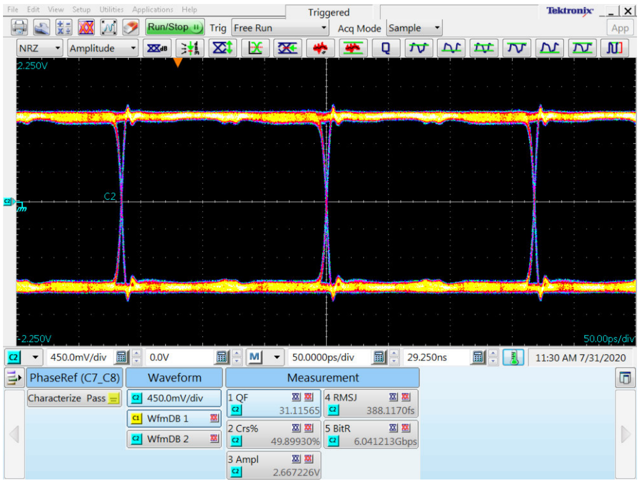
20 Gbps output at maximum output level



16 Gbps output at maximum output level

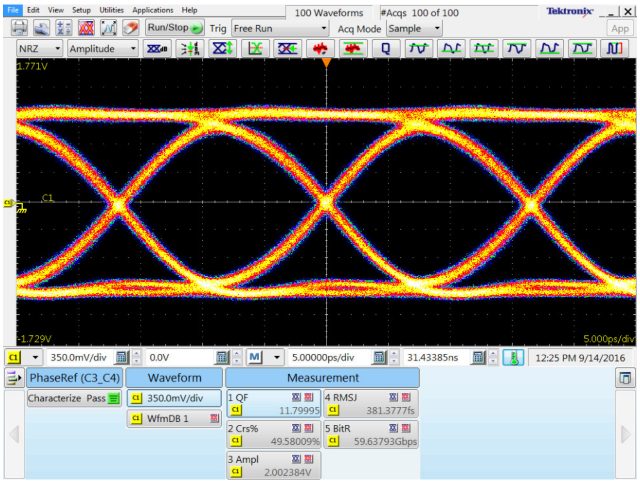


10 Gbps output at maximum output level

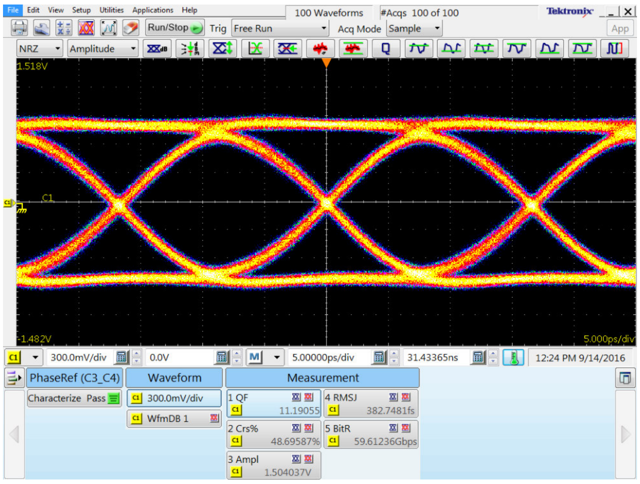


6 Gbps output at maximum output level

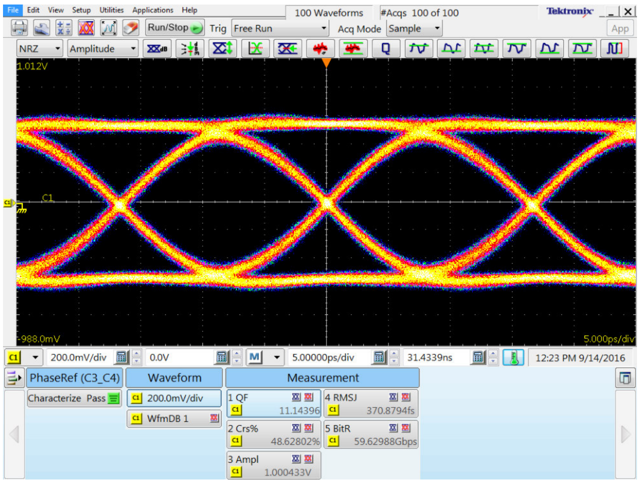
Data Output Signals - Amplitude Adjustment (with Option HV)



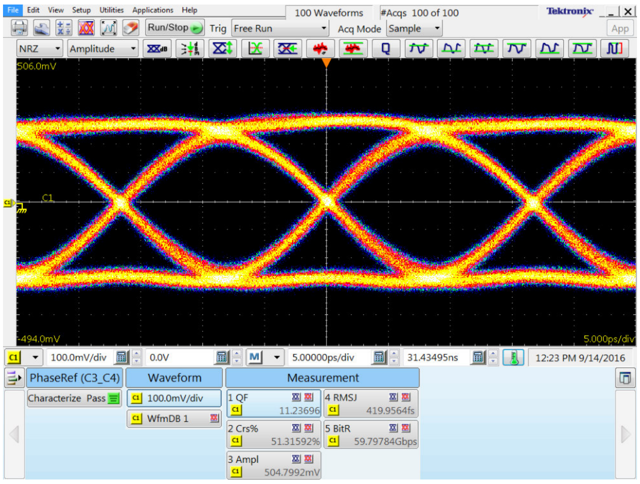
60 Gbps output at 2000 mV



60 Gbps output at 1500 mV

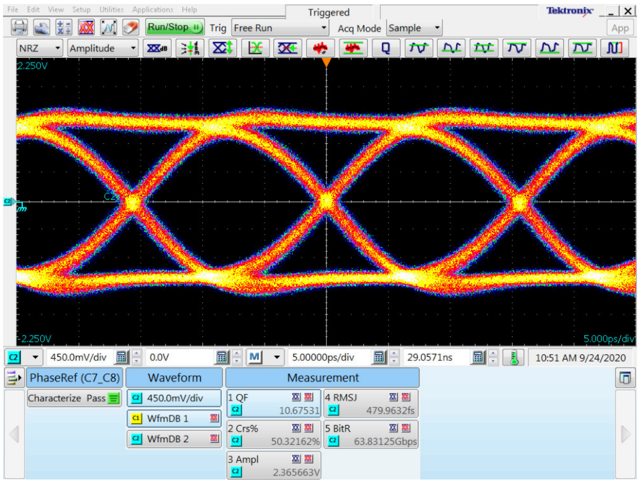


60 Gbps output at 1000 mV

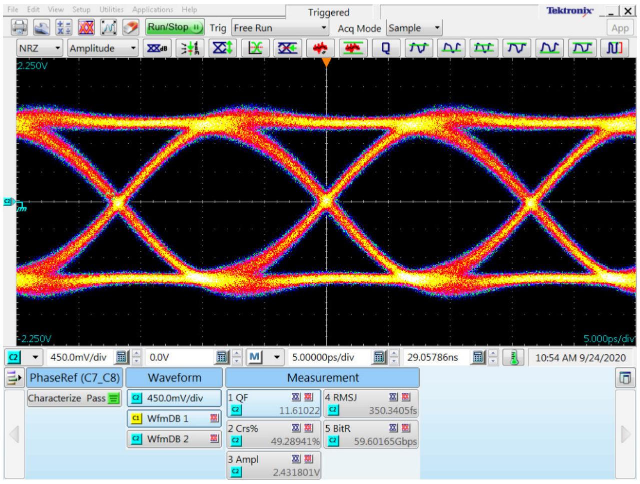


60 Gbps output at 500 mV

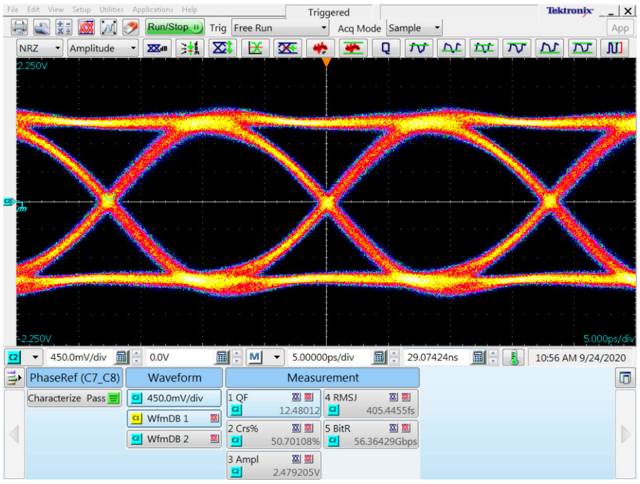
Data Output Signals (with Option HV & Bias-T)



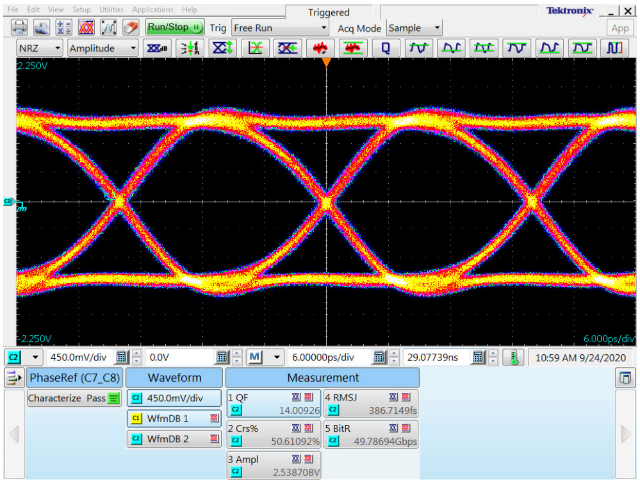
64 Gbps output at maximum output level



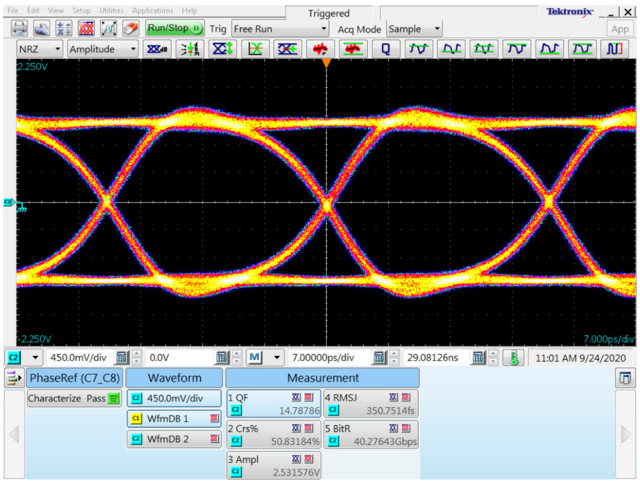
60 Gbps output at maximum output level



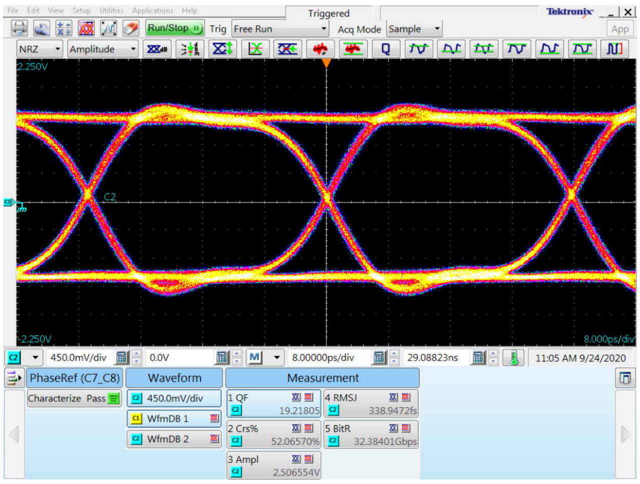
56 Gbps output at maximum output level



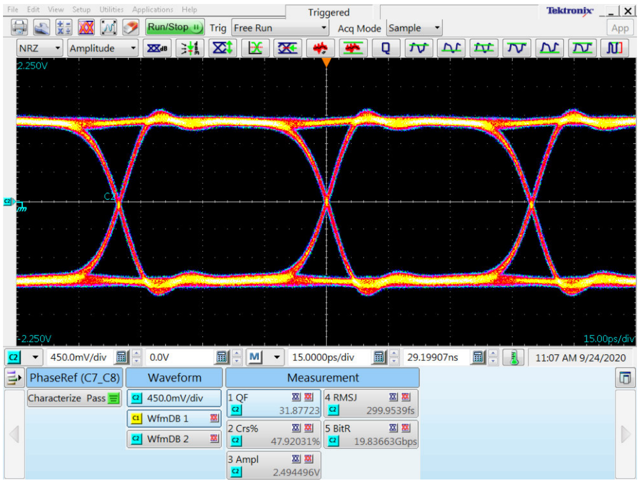
50 Gbps output at maximum output level



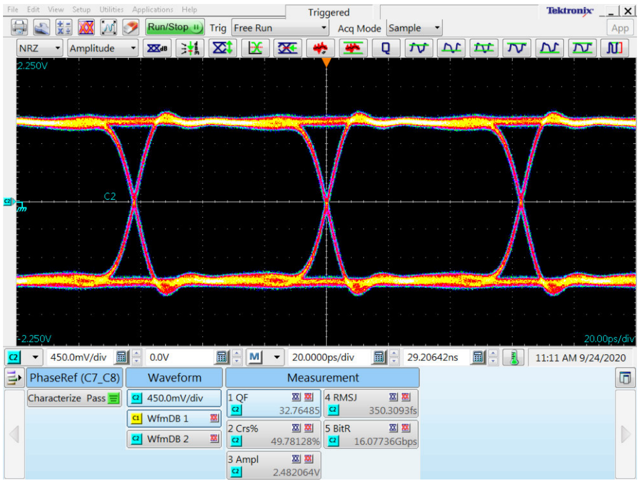
40 Gbps output at maximum output level



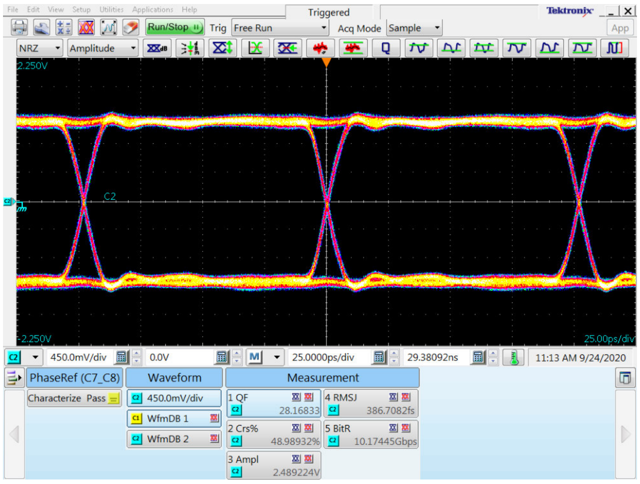
32 Gbps output at maximum output level



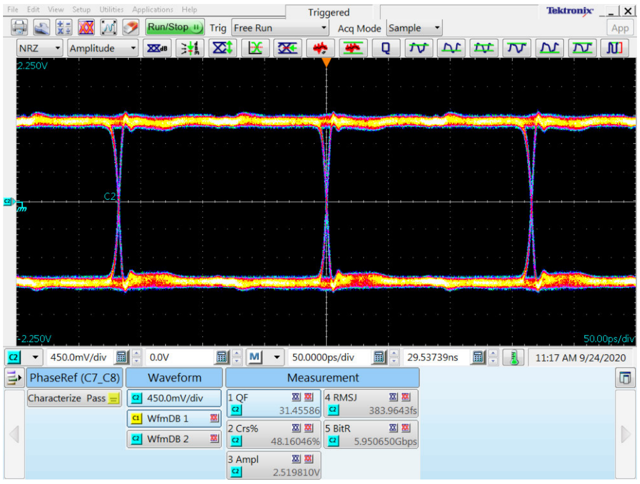
20 Gbps output at maximum output level



16 Gbps output at maximum output level

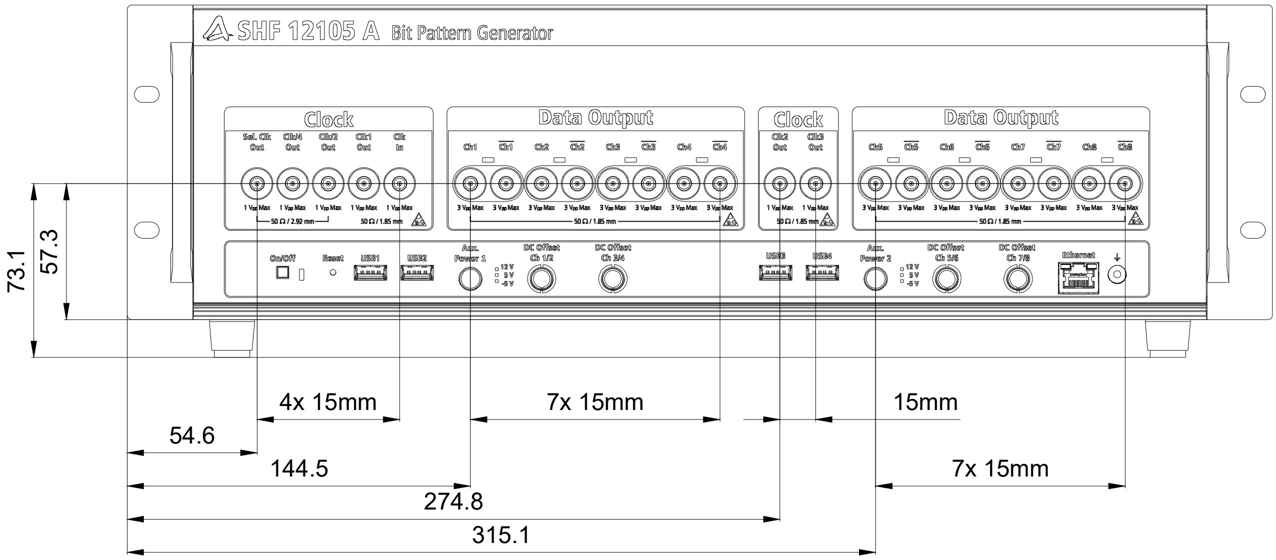


10 Gbps output at maximum output level



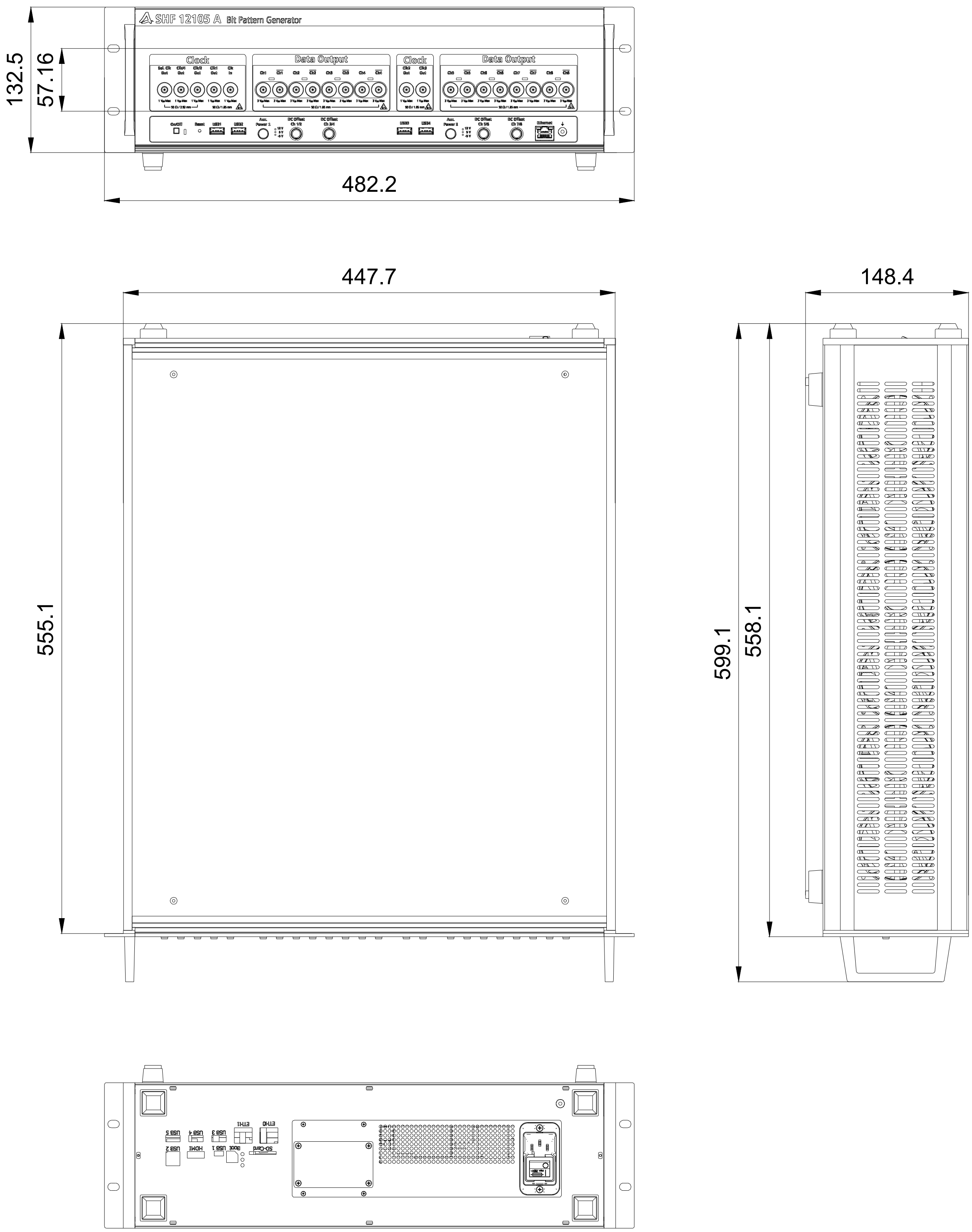
6 Gbps output at maximum output level

Outline Drawing – Front Panel



All dimensions are specified in millimeters (mm).

Outline Drawing – Case



All dimensions are specified in millimeters (mm).

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