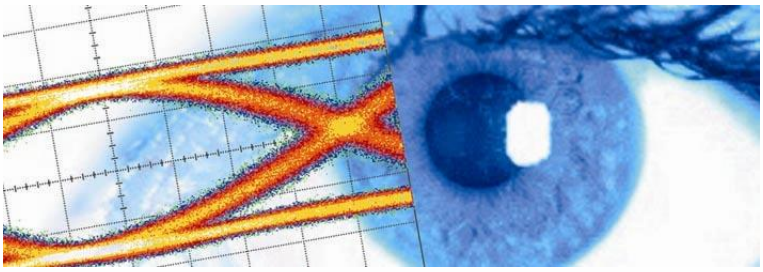
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany

Phone +49 30 772051-0 • Fax ++49 30 7531078

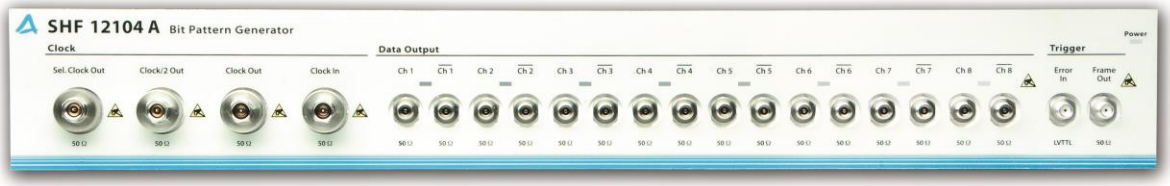
E-Mail: sales@shf.de • Web: http://www.shf.de



Datasheet

SHF 12104 A

Bit Pattern Generator



Description

The SHF 12104 A is a multi-channel 33/60/64 Gbps bit pattern generator (BPG) plug-in, which can be fitted into the SHF 10000 Series mainframes. It generates digital bit sequences such as standard pseudo-random bit sequences (PRBS) or user defined bit patterns.

A wide range of operating bit rates from 3-64 Gbps is covered by the generated data patterns. Depending on the configuration, the instrument features up to four 64 Gbps and/or up to eight 33 Gbps outputs.

The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The 60/64 Gbps outputs can operate at both full clock and half clock, so e.g. a 20 GHz or a 40 GHz signal is required for 40 Gbps operation. The 33 Gbps outputs operate at full clock, so a 33 GHz signal is required for 33 Gbps operation.

Features

- Multiple 60/64 Gbps and 33 Gbps high quality data output channels
- Broadband operation up to aggregated 264 Gbps
- Eight built-in PRBS patterns and 1 Gbit user pattern per channel to support user defined patterns
- Standard Patterns such as JP03A, JP03B, QPRBS13, Transmitter Linearity, SSPR, etc. are included as user patterns
- All channels synchronized but independent
- 33 Gbps outputs adjustable up to -20 dB
- 60/64 Gbps outputs adjustable up to -3 dB
- All outputs can be used single ended or differential
- Bit shift & skew adjustment for each output
- Jitter transparent for jitter tolerance tests
- Frame trigger output
- Error injection capabilities
- Controlled by intuitive graphical user interface BERT Control Center (BCC)

Applications

The SHF 12104 A is the ideal pattern source for any R&D or production application which requires high speed test data streams for electrical/optical components or transmission systems. The flexible channel configurations, the wide gap free data rate coverage and the advanced features make this BPG the perfect fit e.g. for

- single channel applications,
  e.g. OC-768/STM-256 (using 40G NRZ, DPSK), Fiber Channel®, PCI Express, Serial ATA
- multi-channel applications,
  e.g. OC-768/STM-256 (using 40GBaud QPSK), 100GbE (using 4x32G DP-QPSK)
- multi-level[1] multi-channel applications or
  e.g. for 400G & 1TB DWDM (e.g. using DP-16QAM or 56G PAM-4)
- AWG applications
  the 12104 A + DAC combination is a full "remote head" non-interleaved AWG (Arbitrary Waveform Generator) at a speed of up to 60 GBaud

[1] up to 64 level signals can be generated with the help of one of SHF's external DAC modules.

Configurations

The SHF 12104 A can be equipped in a variety of different configurations; either with 60/64 Gbps or 33 Gbps data outputs only or with both types of outputs fitted together in one pattern generator.

Configurations of 60/64 Gbps Data Outputs

- Quad 60 – Four differential outputs from 6 to 60 Gbps (eight outputs in total)
- Dual 60 – Two differential outputs from 6 to 60 Gbps (four outputs in total)
- Single 60 – One differential output from 6 to 60 Gbps (two outputs in total)
- Quad 64 – Four differential outputs from 6 to 64 Gbps (eight outputs in total)
- Dual 64 – Two differential outputs from 6 to 64 Gbps (four outputs in total)
- Single 64 – One differential output from 6 to 64 Gbps (two outputs in total)

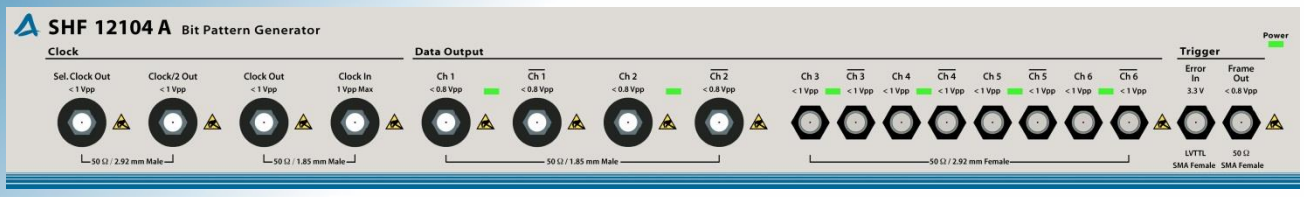
Configurations of 33 Gbps Data Outputs

- Oct 33 – Eight differential outputs from 3 to 33 Gbps (sixteen outputs in total)
- Quad 33 – Four differential outputs from 3 to 33 Gbps (eight outputs in total)
- Dual 33 – Two differential outputs from 3 to 33 Gbps (four outputs in total

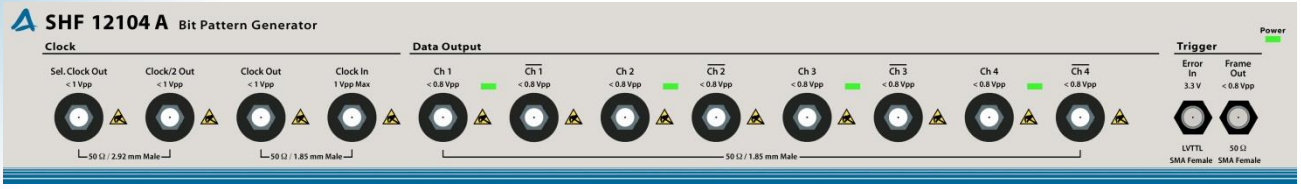
Available Combinations

	No 33 Gbps	**Dual 33 Gbps**	**Quad 33 Gbps**	**Oct 33 Gbps**
No 60/64 Gbps		✓	✓	✓
Single 60/64 Gbps	✓	✓	✓	
Dual 60/64 Gbps	✓	✓	✓	
Quad 60/64 Gbps	✓			

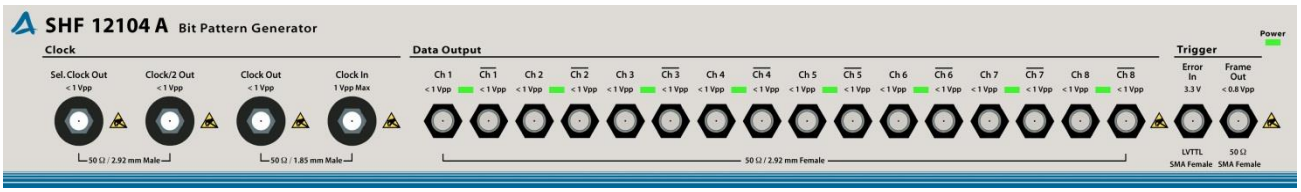
Configuration Examples



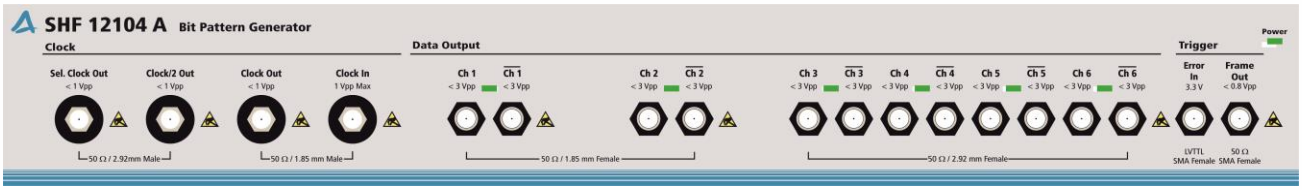
SHF 12104 A in configuration Dual 60/64 & Quad 33



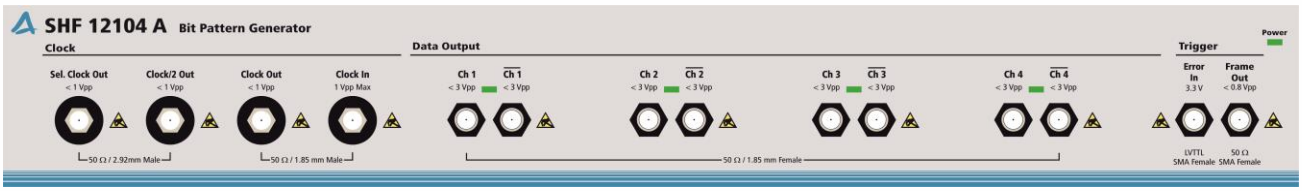
SHF 12104 A in configuration Quad 60/64



SHF 12104 A in configuration Oct 33



SHF 12104 A in configuration Dual 60/64 & Quad 33 (high voltage)



SHF 12104 A in configuration Quad 60/64 (high voltage)

Options

Option HV - High Output Voltage

Maximum output amplitude of a 60/64 Gbps or 33 Gbps data output channel is internally extended to 2 V and can be reduced up to -20 dB using BCC control.

Option Extender SHF 601 A

SHF offers fitting external modules to multiplex two data stream of the SHF 12104 A to one data stream of twice the speed.

Such an extender can be placed very close or even directly to the device under test. In order to serve the individual configuration and testing needs SHF provides the modules without any cabling. However, we would be happy to add the required clock and data cable assemblies tailored to the individual setups.

Two 33G channels can be multiplexed externally to one data stream up to 60 Gbps by the use of a SHF 601 A 2:1 multiplexer. For details please be referred to the data sheet of the SHF 601 A.

Option Extender SHF 603 A

Two 60G channels can be multiplexed externally to 1 data stream up to 120 Gbps by the use of a SHF 603 A 2:1 multiplexer. For details please be referred to the data sheet of the SHF 603 A.

Specifications – SHF 12104 A

60/64 Gbps Data Output Specifications (without Option HV)

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		4	6[2]	
Maximum Bit Rate in 60G configuration		Gbps	60	62		Bit rates above 56 Gbps require half clock mode
Maximum Bit Rate in 64G configuration		Gbps	64	65		Bit rates above 56 Gbps require half clock mode
Maximum Output Level (Eye Amplitude)	V_{out}	mV	550	650	800	adjustable by up to -3 dB DC coupled ground referenced CML interface
Jitter (RMS) on scope display[3]	J_{RMS}	fs		350	550	
Jitter (RMS) deconvolved[4]	J_{RMS}	fs		287	512	
Jitter (PP)	J_{PP}	ps		2	4	
Rise/Fall Time on scope display[5]	t_r/t_f	ps		8	10	20%...80%
Rise/Fall Time deconvolved[6]	t_r/t_f	ps		7.1	9.3	20%...80%
Crossing[7]		%	48		58	@ max. output level
Duty Cycle		%	47	50	53	of two consecutive eyes can be adjusted using BCC
Skew Control		ps	-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew		ps			3	at 60 Gbps with skew control set to 0ps
Connector Type		Ω		50		ruggedized 1.85 mm (V) male connector

[2] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 3 Gbps (see page 10)

[3] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[4] Calculation based on typical jitter from oscilloscope data sheet : $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$

[5] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[6] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

[7] Reducing the output amplitude results in an increased crossing value

60/64 Gbps Data Output Specifications (with Option HV)

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		4	6[8]	
Maximum Bit Rate in 60G configuration		Gbps	60	62		Bit rates above 56 Gbps require half clock mode
Maximum Bit Rate in 64G configuration		Gbps	64	65		Bit rates above 56 Gbps require half clock mode
Maximum Output Level (Eye Amplitude)	V_{out}	mV	2000			adjustable by up to -20 dB AC coupled
Jitter (RMS) On scope display[9]	J_{RMS}	fs		450 600	600 900	V_{out} ≥ 500 mV V_{out} < 500 mV
Jitter (RMS) Deconvolved[10]	J_{RMS}	fs		403 566	566 877	V_{out} ≥ 500 mV V_{out} < 500 mV
Jitter (PP)	J_{PP}	ps		2.5 3	4 5	V_{out} ≥ 500 mV V_{out} < 500 mV
Rise/Fall Time On scope display[11]	t_r/t_f	ps		 9 10	 11 12	20%...80% V_{out} ≥ 500 mV V_{out} < 500 mV
Rise/Fall Time Deconvolved[12]	t_r/t_f	ps		 8.2 9.3	 10.4 11.4	20%...80% V_{out} ≥ 500 mV V_{out} < 500 mV
Crossing		%	45 40		54 60	V_{out} ≥ 1000 mV V_{out} < 1000 mV
Duty Cycle		%	47	50	53	of two consecutive eyes can be adjusted using BCC
Skew Control		ps	-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew		ps			3	at 60 Gbps with skew control set to 0ps
Connector Type		Ω		50		1.85 mm (V) female connector

[8] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 3 Gbps (see page 10)

[9] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[10] Calculation based on typical jitter from oscilloscope data sheet : $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$

[11] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[12] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

33 Gbps Data Output Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		2	3[13]	depending on configuration
Maximum Bit Rate		Gbps	33	34		
Maximum Output Level (Eye Amplitude)	V_{out}	mV	650	700[14]	800	AC coupled adjustable up to -20 dB
Jitter (RMS) on scope display[15],	J_{RMS}	fs		350	550	@ full swing
Jitter (RMS) deconvolved[16]	J_{RMS}	fs		287	512	@ full swing
Jitter (PP)	J_{PP}	ps		2	4	on scope display[15]
Rise/Fall Time on scope display[15]	t_r/t_f	ps		9	11	20%...80%
Rise/Fall Time deconvolved[17]	t_r/t_f	ps		8.2	10.4	20%...80%
Crossing		%	46 46		54 60	V_{out} ≥ 200 mV V_{out} < 200 mV
Duty Cycle		%	47	50	53	of two consecutive eyes can be adjusted using BCC
Skew Control		ps	-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew		ps			3	with skew control set to 0ps
Connector Type		Ω		50		2.92 mm (K) female

[13] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 1.5 Gbps (see page 10)

[14] For PRBS patterns only. Due to the AC coupling certain user patterns may result in eye amplitudes of up to 1.5 V

[15] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[16] Calculation based on typical jitter from oscilloscope data sheet : $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$

[17] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

33 Gbps Data Output Specifications (with Option HV)

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		2	3[18]	depending on configuration
Maximum Bit Rate		Gbps	33	34		
Maximum Output Level (Eye Amplitude)	V_{out}	mV	2000			adjustable by up to -20 dB AC coupled
Jitter (RMS) On scope display[19]	J_{RMS}	fs		450 600	600 900	V_{out} ≥ 500 mV V_{out} < 500 mV
Jitter (RMS) Deconvolved[20]	J_{RMS}	fs		403 566	566 877	V_{out} ≥ 500 mV V_{out} < 500 mV
Jitter (PP)	J_{PP}	ps		2.5 3	4 5	V_{out} ≥ 500 mV V_{out} < 500 mV
Rise/Fall Time On scope display[21]	t_r/t_f	ps		9 10	11 12	20%...80% V_{out} ≥ 500 mV V_{out} < 500 mV
Rise/Fall Time Deconvolved[22]	t_r/t_f	ps		8.2 9.3	10.4 11.4	20%...80% V_{out} ≥ 500 mV V_{out} < 500 mV
Crossing		%	45 40		54 60	V_{out} ≥ 1000 mV V_{out} < 1000 mV
Duty Cycle		%	47	50	53	of two consecutive eyes can be adjusted using BCC
Skew Control		ps	-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew		ps			3	at 60 Gbps with skew control set to 0 ps
Connector Type		Ω		50		2.92 mm (K) female

[18] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 1.5 Gbps (see page 10)

[19] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[20] Calculation based on typical jitter from oscilloscope data sheet : $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$

[21] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1

[22] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

Clock Specifications

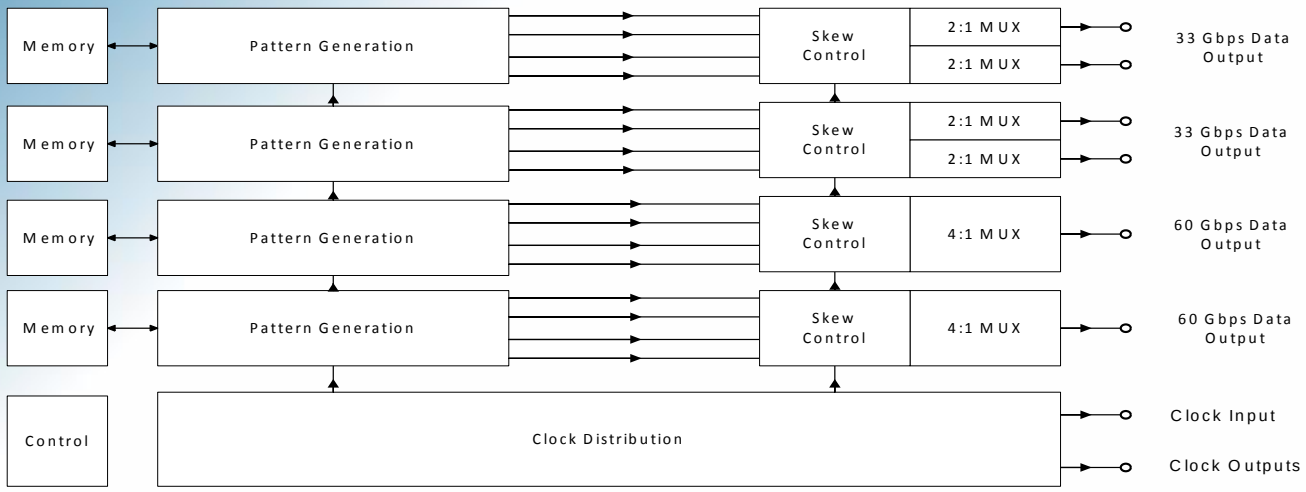
Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Connector Type Clock Input Clock Output Clock/2 Sel. Clock Output		Ω		50		 ruggedized 1.85 mm (V) male connector ruggedized 1.85 mm (V) male connector ruggedized 2.92 mm (K) male connector ruggedized 2.92 mm (K) male connector
Minimum Clock Input Frequency	f_{in_clock}	GHz			3 6	half clock mode[23] full clock mode[23]
Maximum Clock Input Frequency	f_{in_clock}	GHz	30 56			half clock mode[23] full clock mode[23]
Maximum Clock Input Frequency with Option “64 G Output”	f_{in_clock}	GHz	32 56			half clock mode[23] full clock mode[23]
Input Level	V_{in_clock}	mV_{pp}	600		1000	AC coupled
Output Level Clock Clock/2 Selectable Clock	V_{out_clock}	mV_{pp}	 500 500 400	 700 800 600	 1000 1000 800	 AC coupled, @ P_{in}=0dBm AC coupled, AC coupled,
Output Frequency Clock Clock/2 Selectable Clock	f_{out_clock}	 GHz GHz GHz	 1 0.5 0.001		 56 28 14	 same as input frequency half of input frequency input frequency/N (N= 4, 8, 16, 32, 64, 128, 256, 512, 1024)

[23] The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The 60 Gbps outputs can operate at both full clock and half clock, so e.g. a 20 GHz or a 40 GHz signal is required for 40 Gbps operation. The 33 Gbps outputs operate at full clock, so a 33 GHz signal is required for 33 Gbps operation.

Pattern Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Output Pattern						ITU-T (CCITT) conform PRBS patterns at a length of 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 & 2^{31}-1 plus user defined patterns
User Pattern Memory Size for 33 Gbps Data Outputs		Gbit			1	Per channel
User Pattern Memory Size for 60 Gbps Data Outputs		Gbit			1	Per channel
User Pattern Granularity for 33 Gbps Data Outputs		Bit		1024		See Chapter User Pattern Capabilities
User Pattern Granularity for 60 Gbps Data Outputs		Bit		1024		See Chapter User Pattern Capabilities
Frame Trigger Output						
Connector Type		Ω		50		SMA female
Output Level Frame		mV		800		AC coupled

Block Diagram

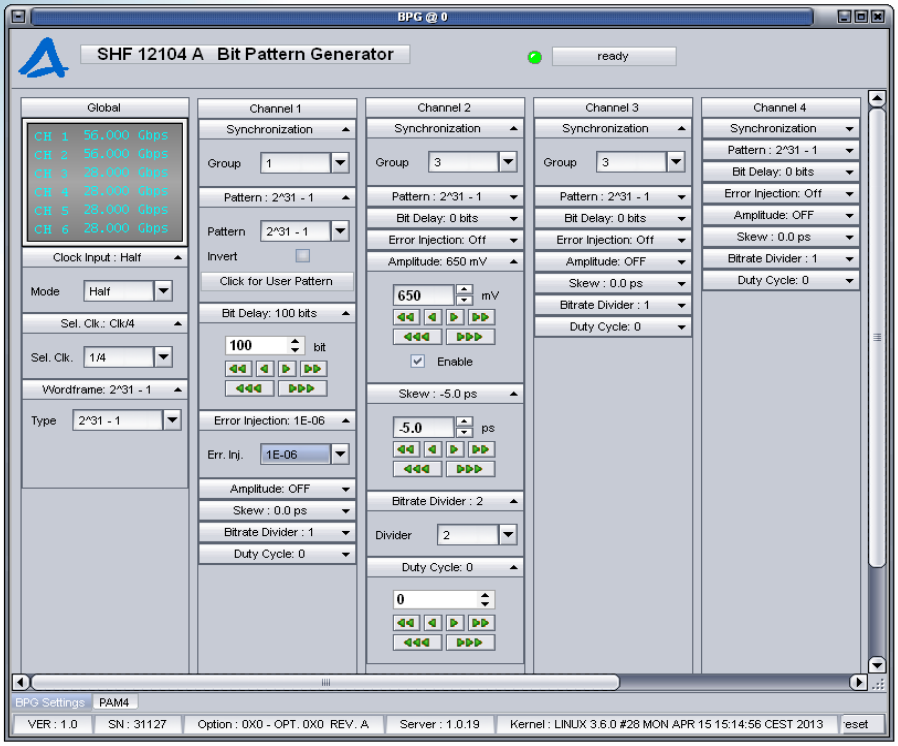


The pattern generator consists of sixteen 16 Gbps pattern generation blocks which are synchronized to each other. The outputs of the pattern generation blocks are either 2:1 multiplexed to generate a 33 Gbps data output stream or 4:1 multiplexed to generate a 60/64 Gbps data output steam. In any configuration where 33 Gbps and 60 Gbps outputs are present at the same time, the 60/64 Gbps outputs will run at double or the same speed of the 33 Gbps outputs.

The 1 Gbit of user pattern for each pattern generation block will be stored in a 1024 bit wide memory. Each pattern generation block includes the multiplexers to generate the 4x16 Gbps data streams from the incoming 1024 bit wide user pattern data.

The clock distribution section processes the incoming clock signal to generate the clock out, clock/2 out, selectable clock out and word frame signals. Furthermore all clocks needed for the internal components will be generated here.

Output Adjustment Capabilities



Synchronization
The data outputs can be grouped. All data outputs of one group are synchronized to enable AWG functionality together with a DAC, cross talk measurements and PRBS conform multiplexing.

Data Rate
The data rate of all outputs is continuously adjustable by a single external clock signal applied to the clock input. The 60 Gbps data outputs are always running at a data rate of twice the speed of the 33 Gbps data outputs.

Pattern Type
All PRBS and user patterns can be assigned individually to each channel.

Bit Delay/Bit Shift
In case two or more PRBS patterns of the same length are selected it is possible to control the starting point of each bit sequence (in 1 bit steps up to the total PRBS length).

Skew
The timing of every output channel can be adjusted individually in 0.1 ps steps (please see chapter Skew Control Function for more details).

Error Injection
For testing purposes a fixed error rate can be added to the date stream.

Amplitude
The output amplitude of each channel is adjustable independently.

Duty Cycle
The duty cycle of two consecutive eyes/bits is automatically set to 50%. However, in case the application requires a modification or a further optimization, this could be done with a few clicks.

Bit Rate Divider
The ‘bit rate divider’ is a software function to transmit the same bit multiple times and thus reduces the data rate (divided by 2).

User Pattern Capabilities

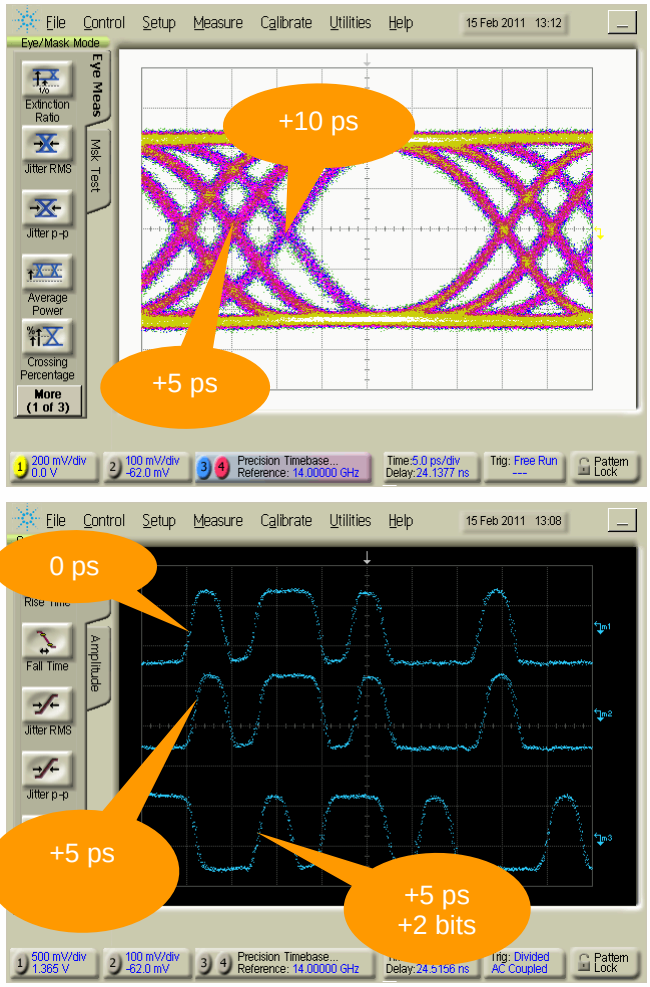
The SHF 12104 A has a built-in 1 Gbit user pattern memory for each output channel which is attached to the pattern generation blocks by a 1024 bit wide interface. Data from the user pattern memory will be multiplexed to generate the 60 Gbps and 33 Gbps output data streams. Thus the pattern length of any user pattern uploaded to the user pattern memory has to be a multiple of 1024.

The Bert Control Center (BCC) software supports creating, editing and converting different formats of user pattern files to be used with the SHF 12104 A. It will handle all user patterns prerequisites. For example it will repeat automatically user patterns not fulfilling the granularity requirement until the granularity of 1024 is met. For patterns up to 1 Mbit this is always possible. Patterns larger than 1 Mbit have to fulfill the following prerequisites:

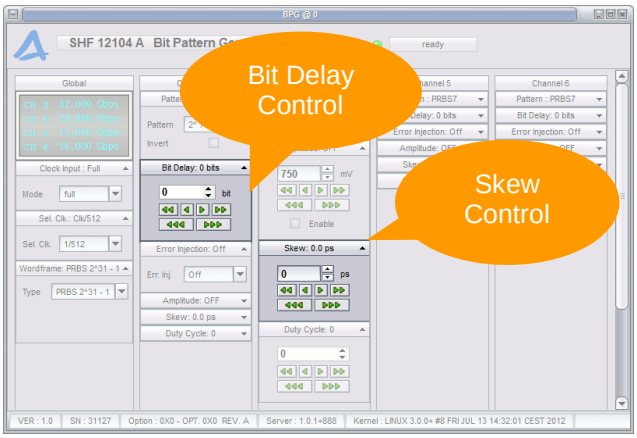
Pattern length up to	Pattern length has to be a multiple of
1 Mbit	1
2 Mbit	2
4 Mbit	4
8 Mbit	8
16 Mbit	16
32 Mbit	32
64 Mbit	64
128 Mbit	128
256 Mbit	256
512 Mbit	512
1 Gbit	1024

Skew Control and Bit Delay Functions

The skew control and bit delay functions allow adjusting the channel timing relative to each other. As a result, timing delays between individual output channels can be adjusted over many bit periods, with the skew function for fine adjustment. The figure below shows the BCC control software with this feature, and an example of delay between two channels for skew within a bit and more than one bit.



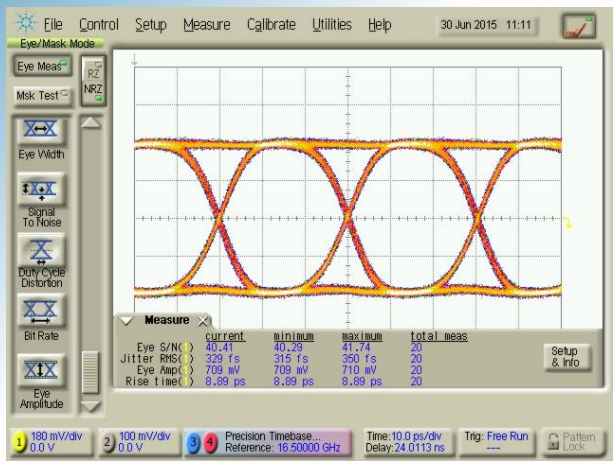
Integer bit delay & skew control



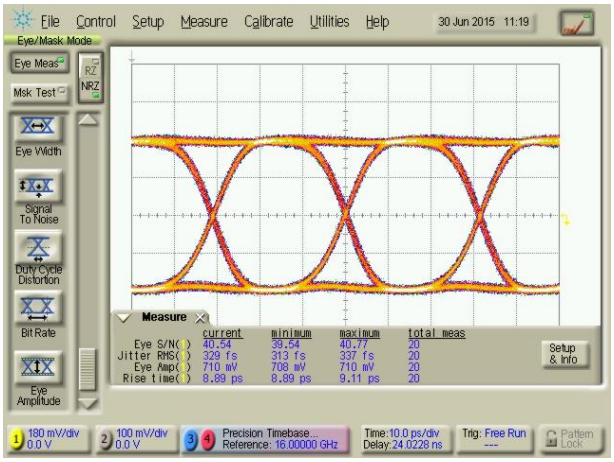
Skew control software representation

Typical Output Waveforms

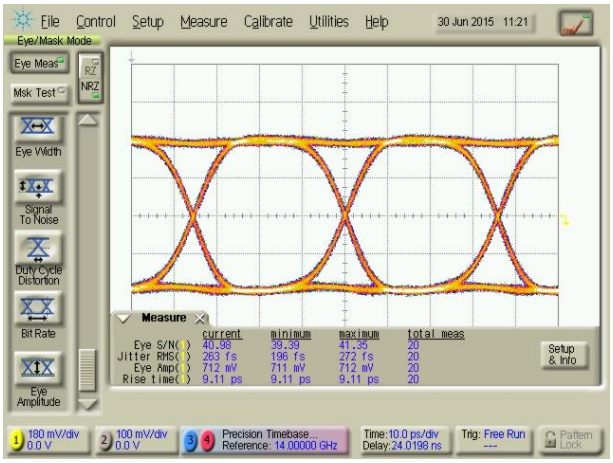
33 Gbps Data Output Signals (without Option HV)



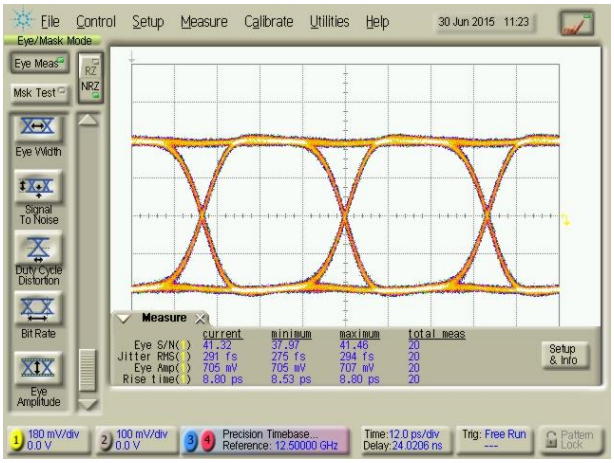
33 Gbps output at maximum output level



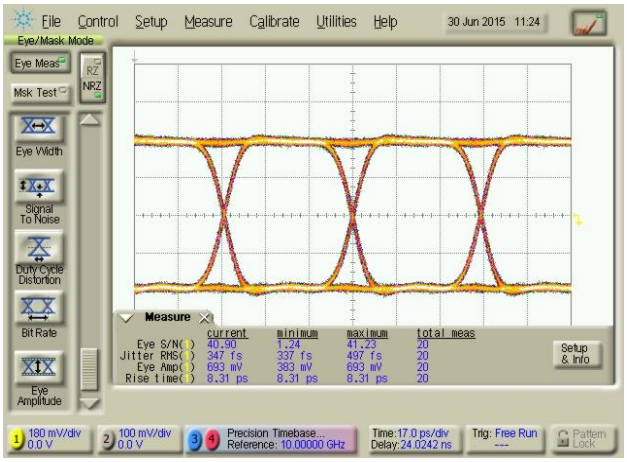
32 Gbps output at maximum output level



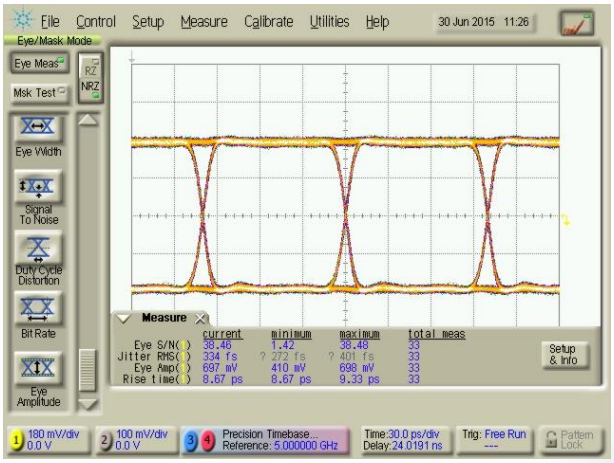
28 Gbps output at maximum output level



25 Gbps output at maximum output level

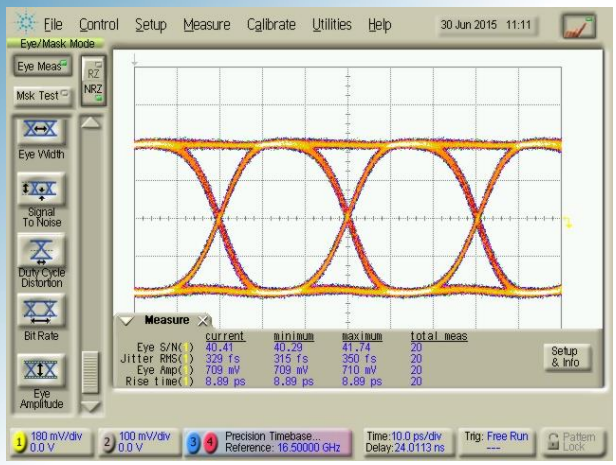


20 Gbps output at maximum output level

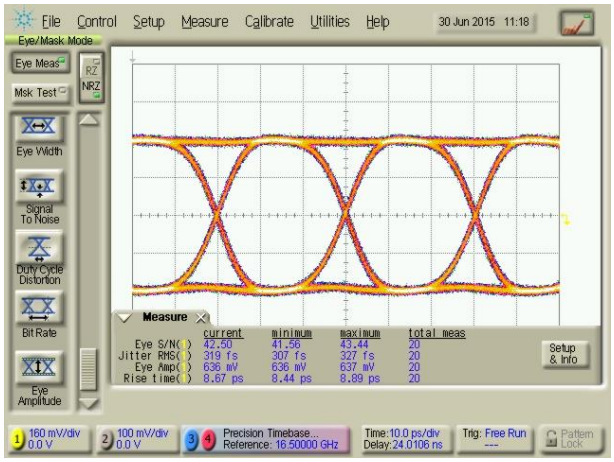


10 Gbps output at maximum output level

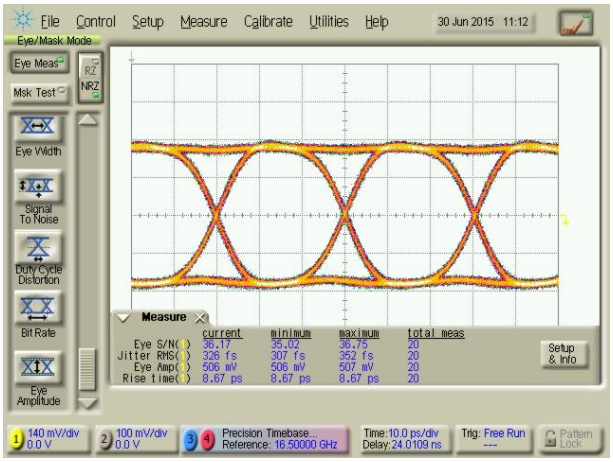
33 Gbps Data Output Signals - Amplitude Adjustment (without Option HV)



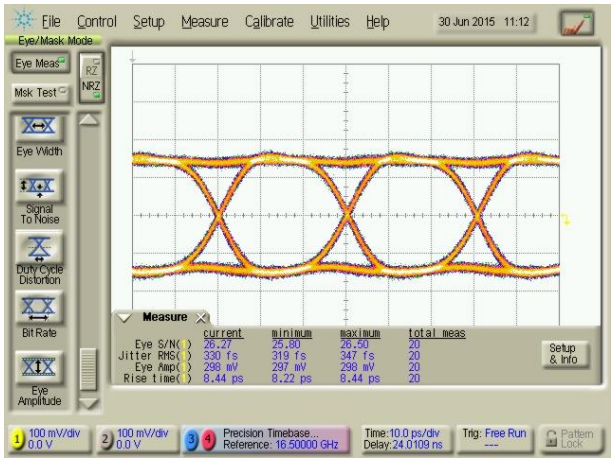
33 Gbps output at 700 mV



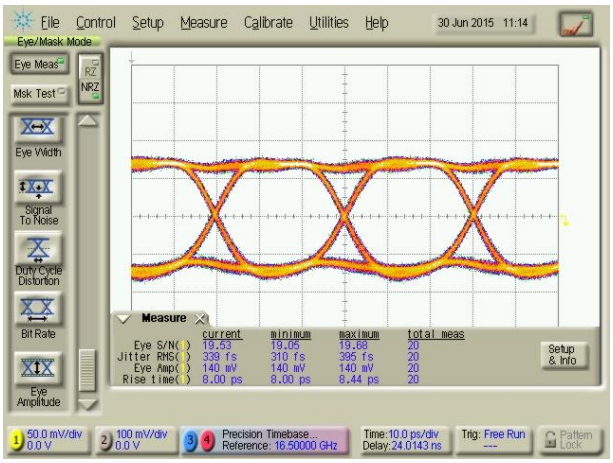
33 Gbps output at 600 mV



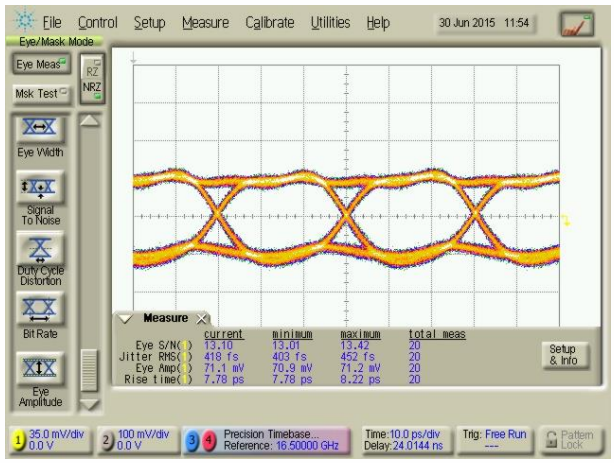
33 Gbps output at 500 mV



33 Gbps output at 300 mV

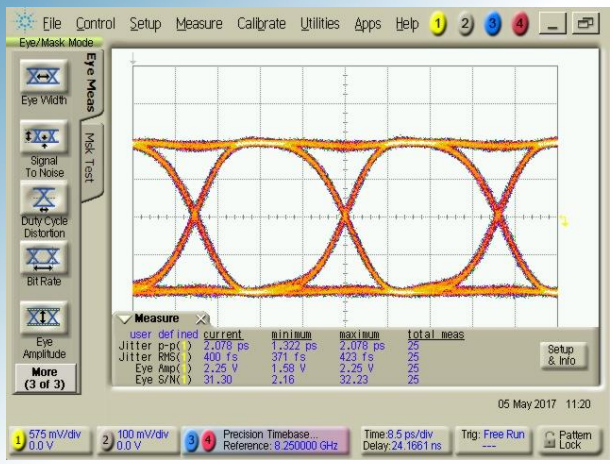


33 Gbps output at 150 mV

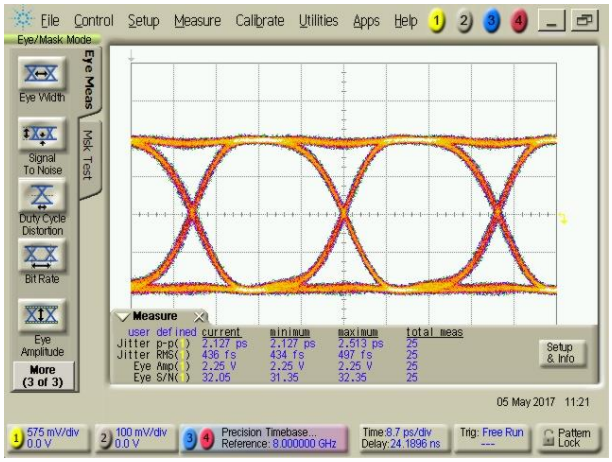


33 Gbps output at 70 mV

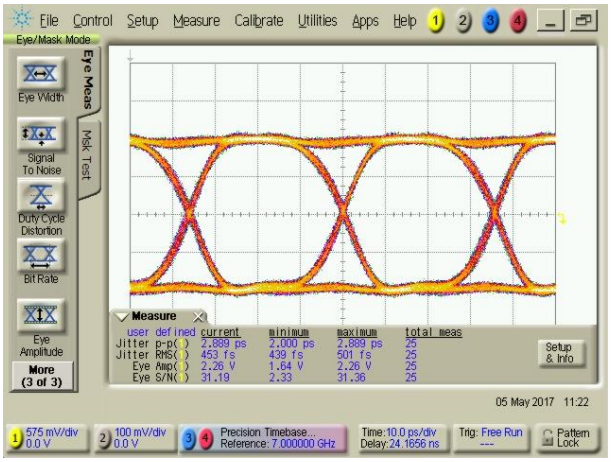
33 Gbps Data Output Signals (with Option HV)



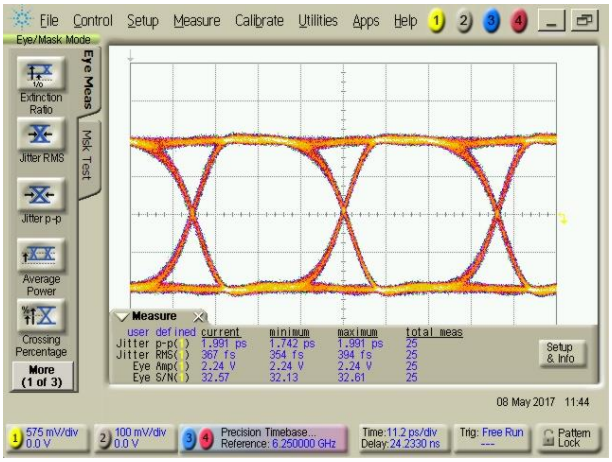
33 Gbps output at maximum output level



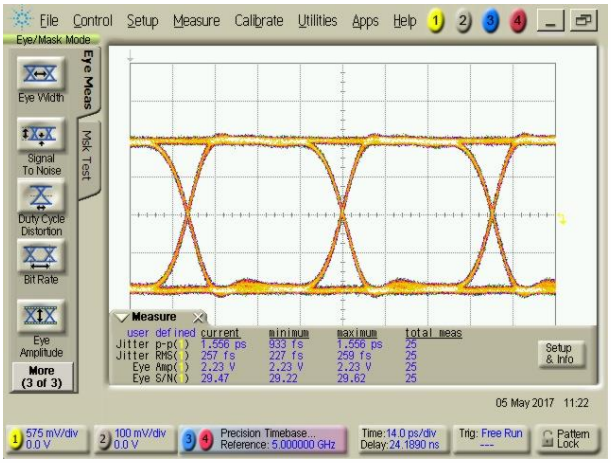
32 Gbps output at maximum output level



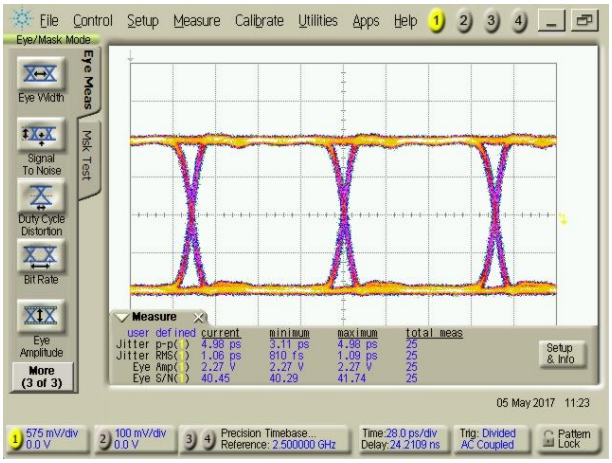
28 Gbps output at maximum output level



25 Gbps output at maximum output level

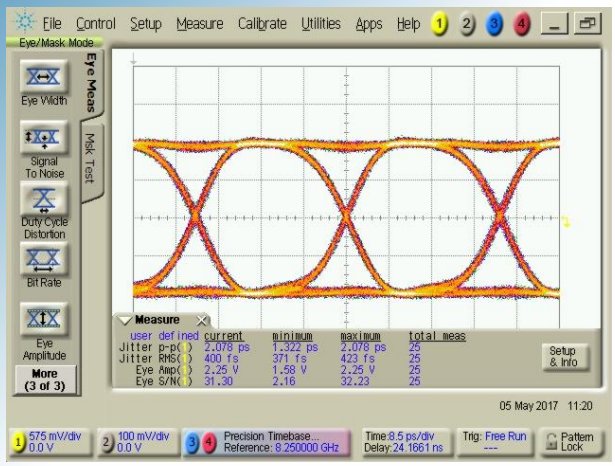


20 Gbps output at maximum output level

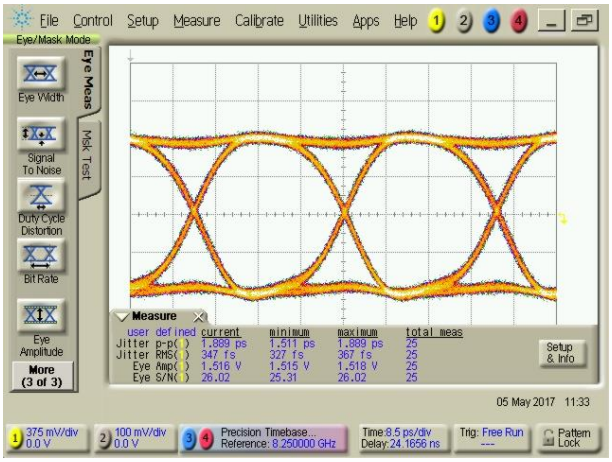


10 Gbps output at maximum output level

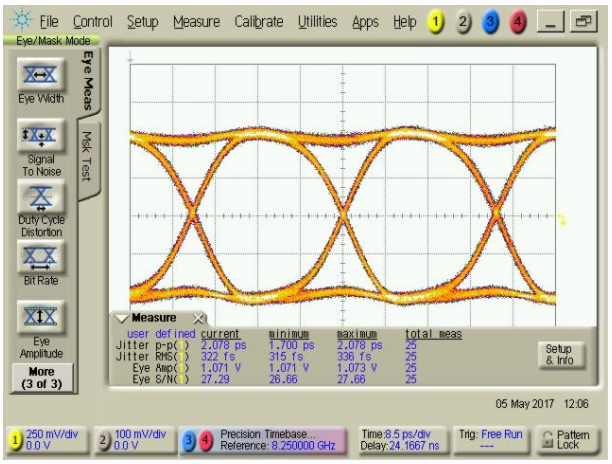
33 Gbps Data Output Signals - Amplitude Adjustment (with Option HV)



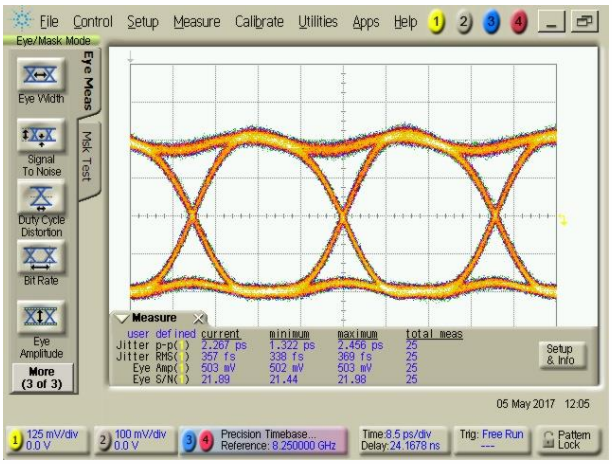
33 Gbps output at 2000 mV



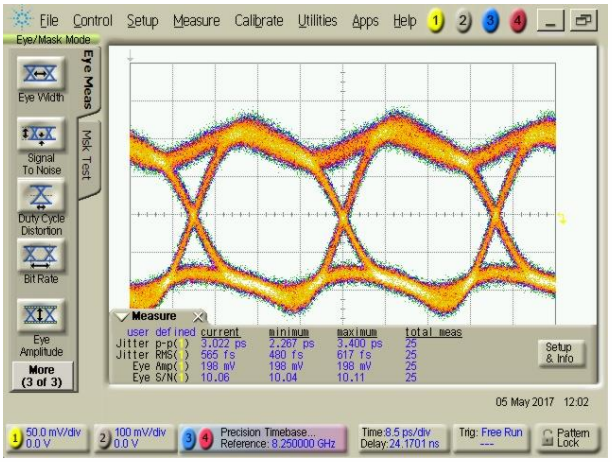
33 Gbps output at 1500 mV



33 Gbps output at 1000 mV

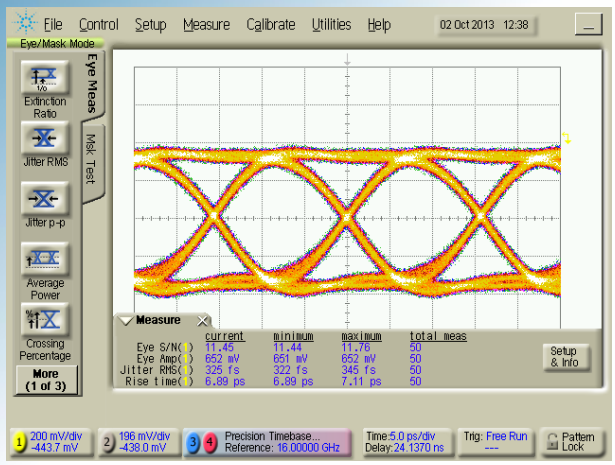


33 Gbps output at 500 mV

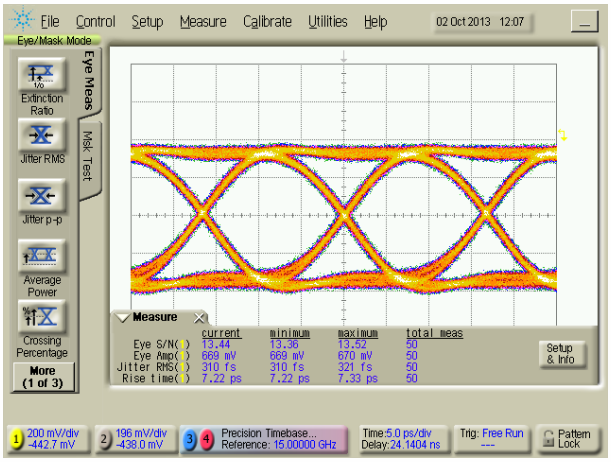


33 Gbps output at 200 mV

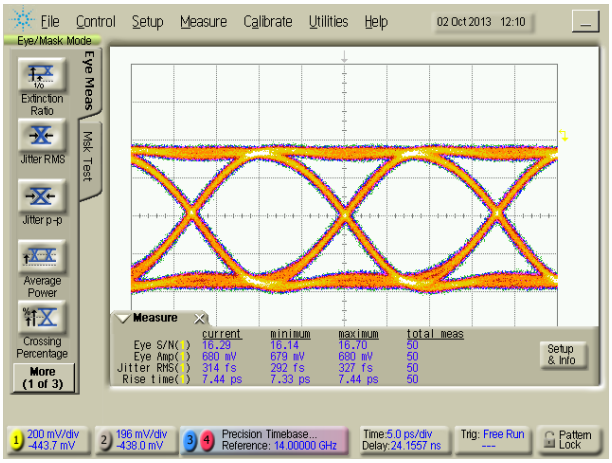
60/64 Gbps Data Output Signals (without Option HV)



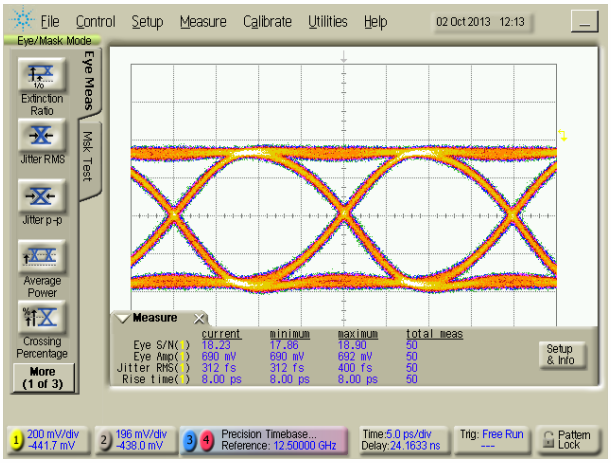
64 Gbps output at maximum output level



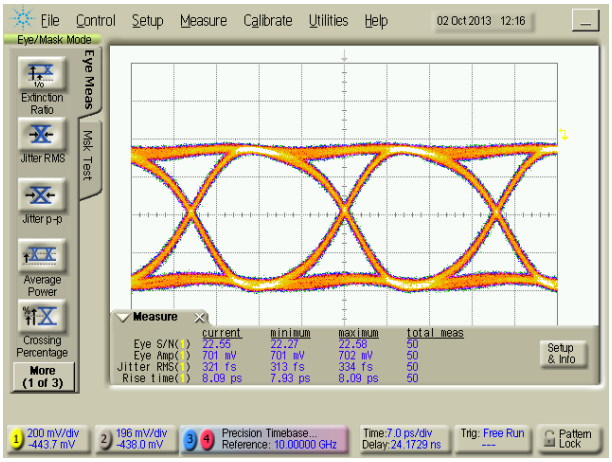
60 Gbps output at maximum output level



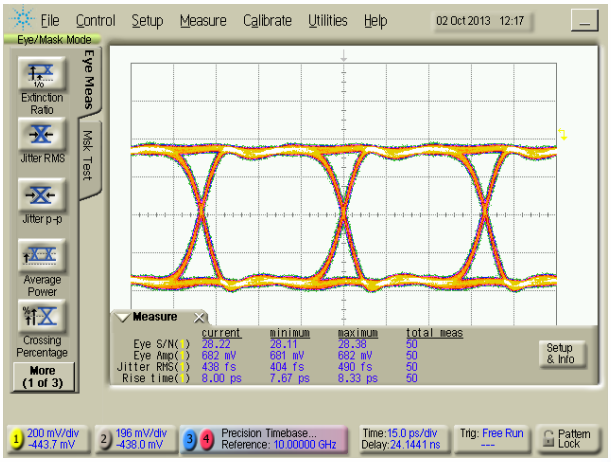
56 Gbps output at maximum output level



50 Gbps output at maximum output level

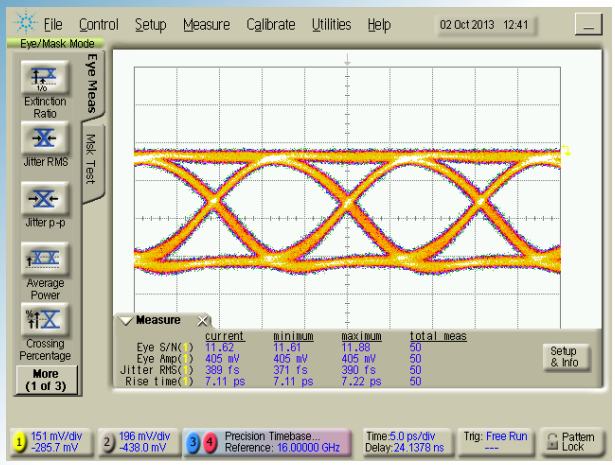


40 Gbps output at maximum output level

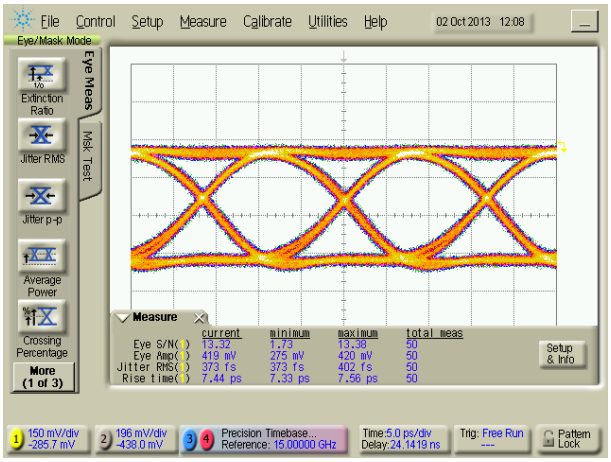


20 Gbps output at maximum output level

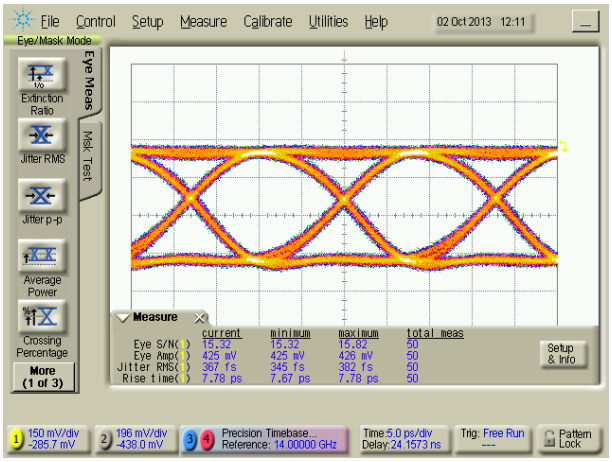
60/64 Gbps Data Output Signals – Minimum Output Amplitude (without Option HV)



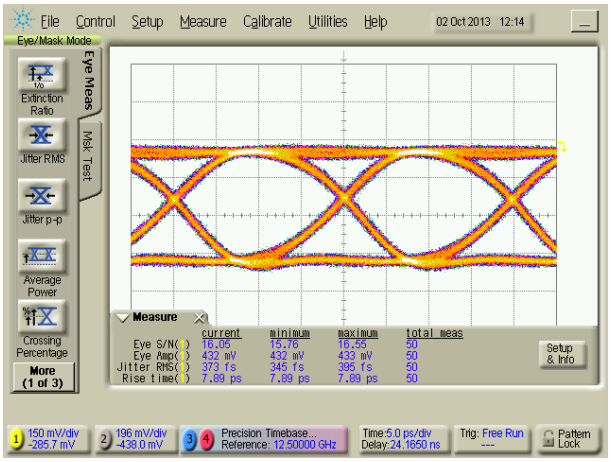
64 Gbps output at minimum output level



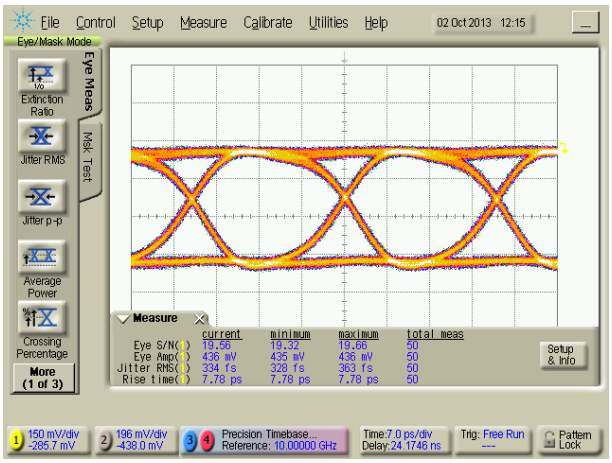
60 Gbps output at minimum output level



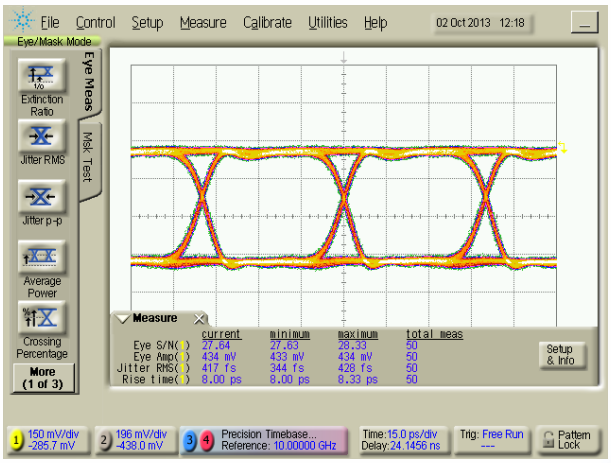
56 Gbps output at minimum output level



50 Gbps output at minimum output level

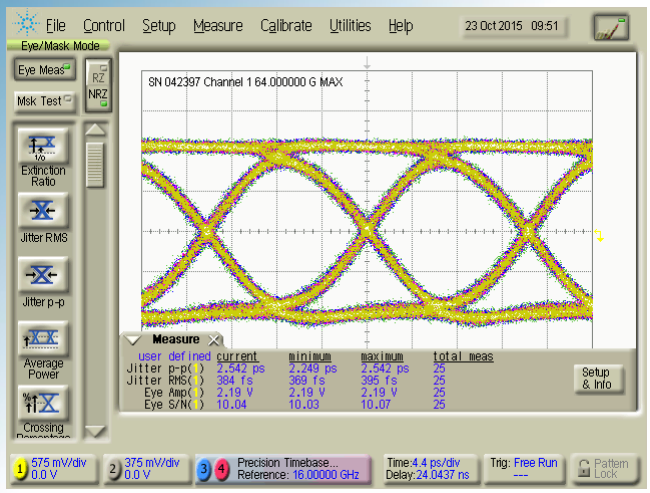


40 Gbps output at minimum output level

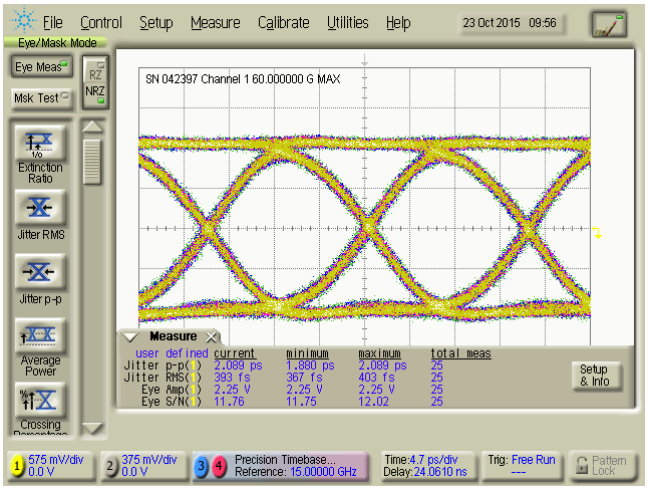


20 Gbps output at minimum output level

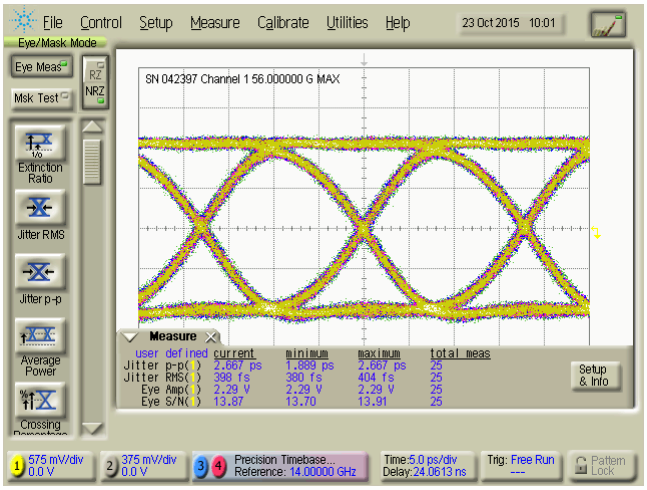
60/64 Gbps Data Output Signals (with Option HV)



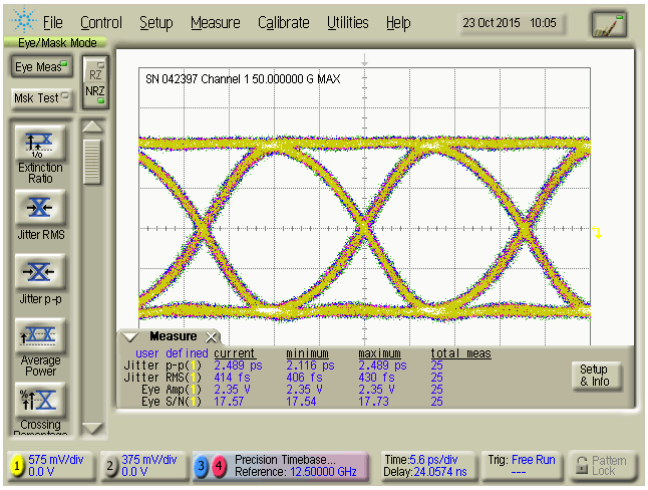
64 Gbps output at maximum output level



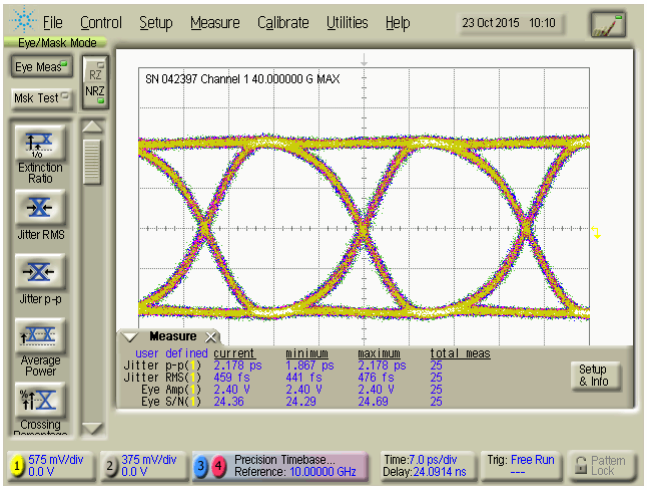
60 Gbps output at maximum output level



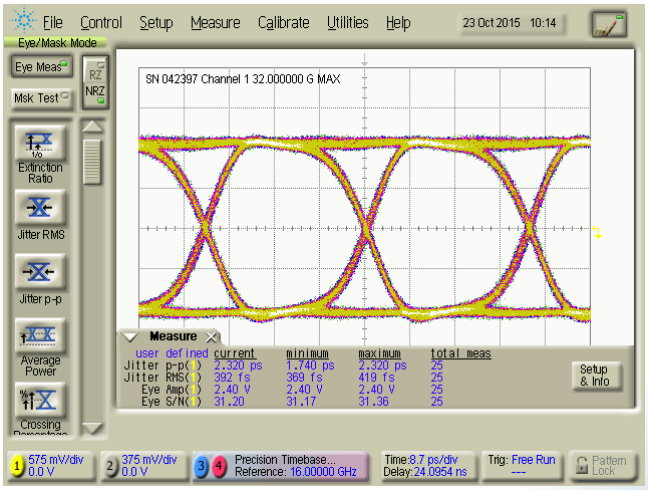
56 Gbps output at maximum output level



50 Gbps output at maximum output level

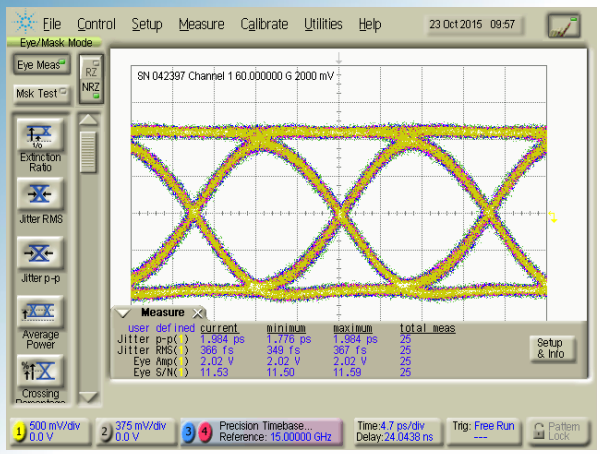


40 Gbps output at maximum output level

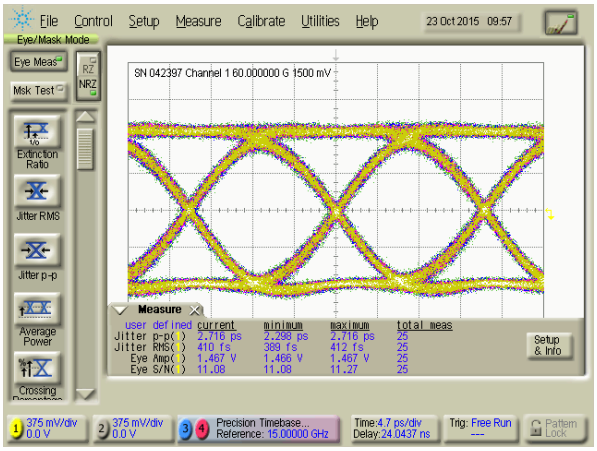


32 Gbps output at maximum output level

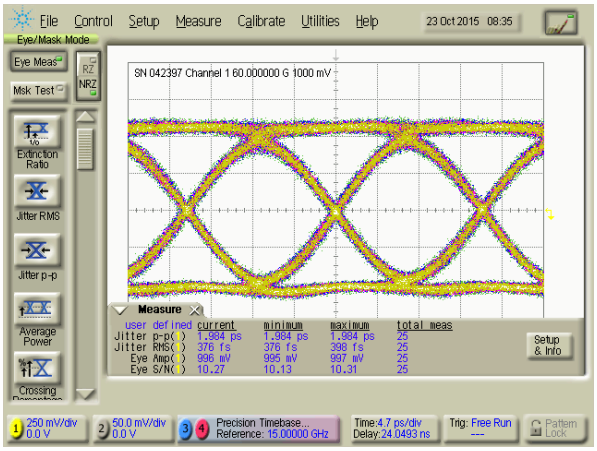
60/64 Gbps Data Output Signals - Amplitude Adjustment (with Option HV)



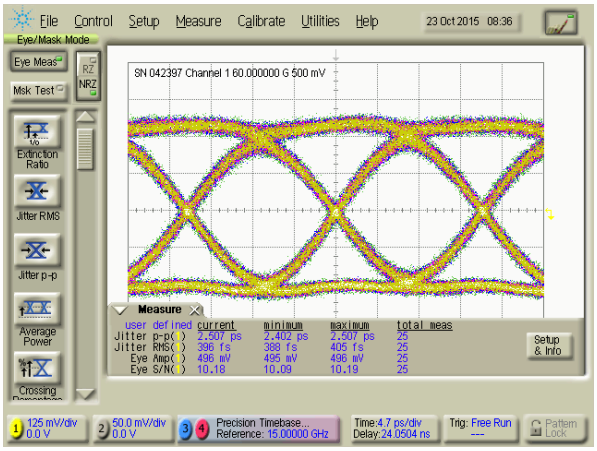
60 Gbps output at 2000 mV



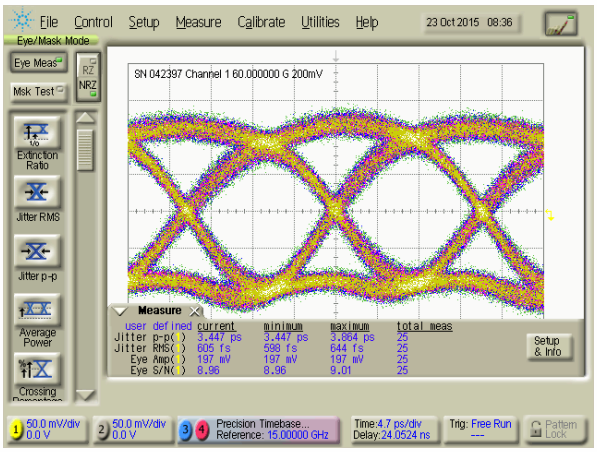
60 Gbps output at 1500 mV



60 Gbps output at 1000 mV

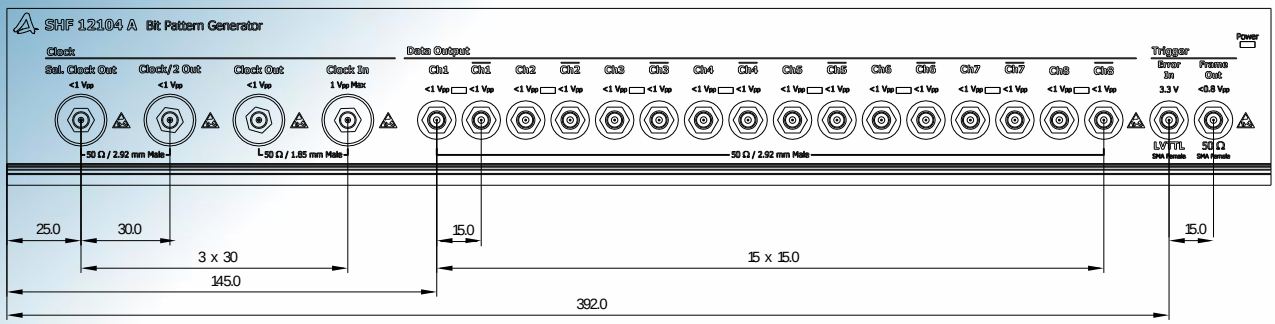


60 Gbps output at 500 mV

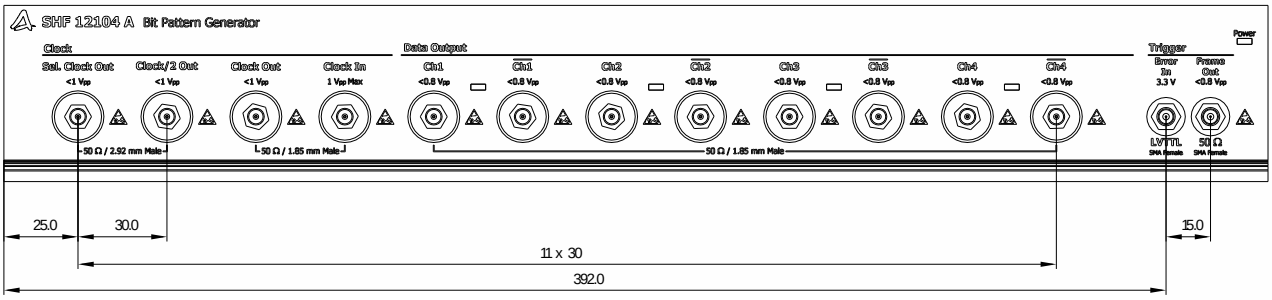


60 Gbps output at 200 mV

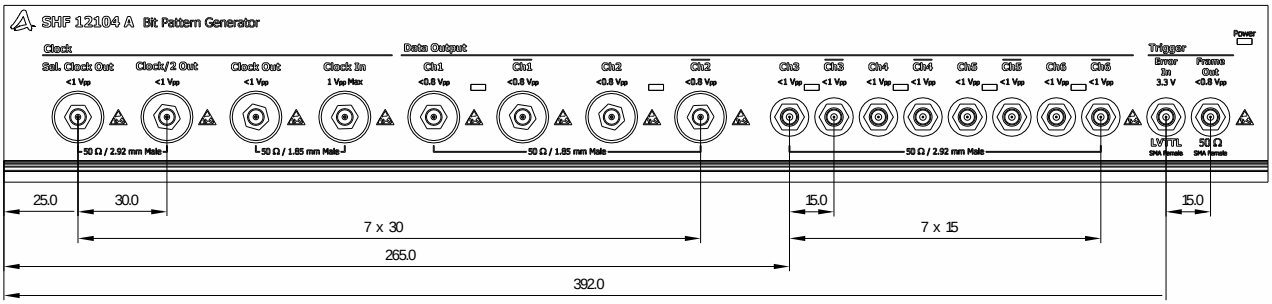
Outline Drawings



SHF 12104 A front panel for 33 Gbps output configurations

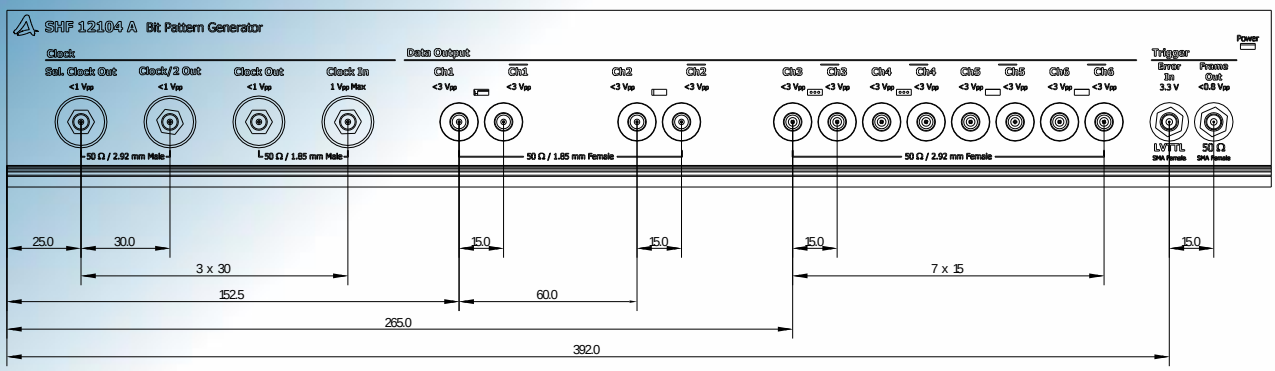


SHF 12104 A front panel for 60/64 Gbps output configurations

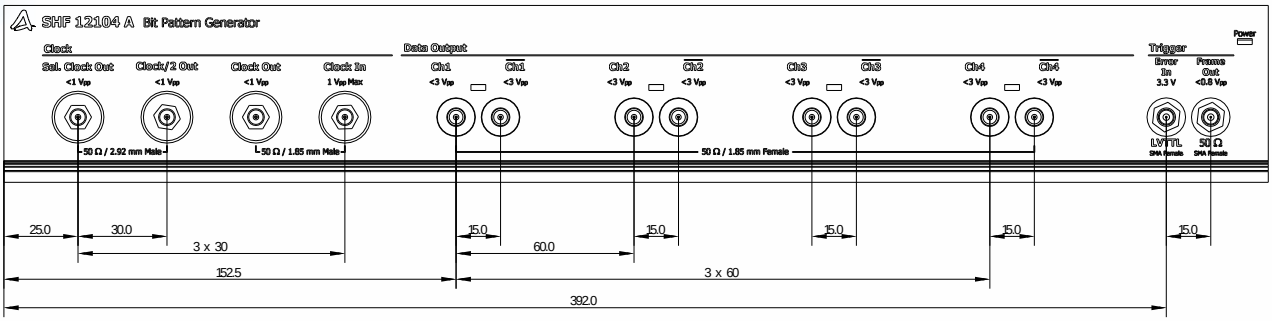


SHF 12104 A front panel for mixed configurations

All dimensions are specified in millimeters (mm).



SHF 12104 A front panel for mixed high voltage output configurations



SHF 12104 A front panel for 60/64 Gbps high voltage output configurations

All dimensions are specified in millimeters (mm).