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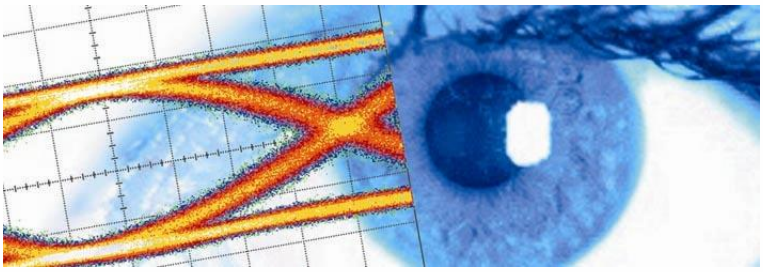


Datasheet

SHF 12103 A

128 Gbps Bit Pattern Generator

Description

The SHF 12103 A is a 128 Gbps bit pattern generator plug-in, which can be fitted into the SHF 10000 Series mainframes. It generates digital bit sequences such as standard pseudo-random bit sequences (PRBS) or user defined bit patterns at the data outputs. Many applications in research and development require these data streams for testing electrical/optical components or transmission systems for high speed digital data communication. A wide range of operating bit rates from 3-56 Gbps is covered by the generated data patterns. Depending on the configuration, the instrument features up to two 56 Gbps and/or up to four 32 Gbps outputs. An optional skew control is available for all configurations of the sub-rate data outputs.

The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The dual 56 Gbps outputs can operate at both full clock and half clock, so either a 28 GHz or a 56 GHz signal is required for 56 Gbps operation. The quad 32 Gbps outputs operate at full clock, so a 32 GHz signal is required for 32 Gbps operation.

Features

- Multiple synchronized but independent channels with high quality adjustable output signals
- Broadband operation up to aggregated 128 Gbps
- Eight built-in PRBS patterns and 1 Gbit user pattern memory to support user defined patterns
- Skew adjustment for subrate outputs
- Pattern hardware pre-coding for DQPSK transmission on subrate outputs
- Frame trigger output
- Operation by intuitive graphical user interface

Configurations and Options

Configurations of Data Outputs

- Single 56 – One differential output from 6 to 56 Gbps (two outputs in total)
- Dual 56 – Two differential outputs from 6 to 56 Gbps (four outputs in total)

Configurations of Subrate Data Outputs

- Dual 28 – Two differential outputs from 3 to 28 Gbps (four outputs in total)
- Quad 28 – Four differential outputs from 3 to 28 Gbps (eight outputs in total)
- Dual 32 – Two differential outputs from 3 to 32 Gbps (four outputs in total)
- Quad 32 – Four differential outputs from 3 to 32 Gbps (eight outputs in total)

All combinations of full and sub rate data outputs are possible. A later upgrade to the higher bit rate limit at the sub rate outputs and retrofitting additional outputs is possible at any time[1].

Options

- SC2 – Skew control for sub-rate outputs (dual-channel version)
- SC4 – Skew control for sub-rate outputs (quad-channel version)

[1] In case the maximum number of outputs is not already exceeded.

Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
56 Gbps Data Outputs						
Bit Rate		Gbps	6		56	
Maximum Output Level (Eye Amplitude)	V_{out}	mV	600	650	700	adjustable by up to -3 dB DC coupled ground referenced CML interface
Jitter (RMS)	J_{RMS}	fs		350 290	550 515	measured at 56 Gbps on scope display[2] deconvoluted[3]
Rise/Fall Time	$t_{r/f}$	ps			10.6 10	20%...80% on scope display[2] deconvoluted[4]
Crossing		%	46	50	54	at full output swing
Duty Cycle		%	47	50	53	of two consecutive eyes could be further optimized manually by software control
Connector Type		Ω		50		ruggedized 1.85 mm (V) male connector
28/32 Gbps Subrate Data Outputs						
Bit Rate		Gbps	3		28/32	depending on configuration
Maximum Output Level (Eye Amplitude)	V_{out}	mV		900[5]		adjustable by up to -6 dB AC coupled
Jitter (RMS)	J_{RMS}	fs		450 400	600 565	measured at 32 Gbps on scope display[2] deconvoluted[3]
Crossing		%	47	50	53	
Duty Cycle		%	47	50	53	of two consecutive eyes could be further optimized manually by software control
Connector Type		Ω		50		2.92 mm (K) female
Rise/Fall Time	t_r/t_f	ps			12.6 12	20%...80% on scope display[2] deconvoluted[4]
Inter-Channel Skew		%			10	of bit period @ bitrate

[2] Measured with Agilent 86100A with 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output

[3] Calculation based on typical jitter from oscilloscope data sheet : $J_{RMS\ deconvoluted} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$

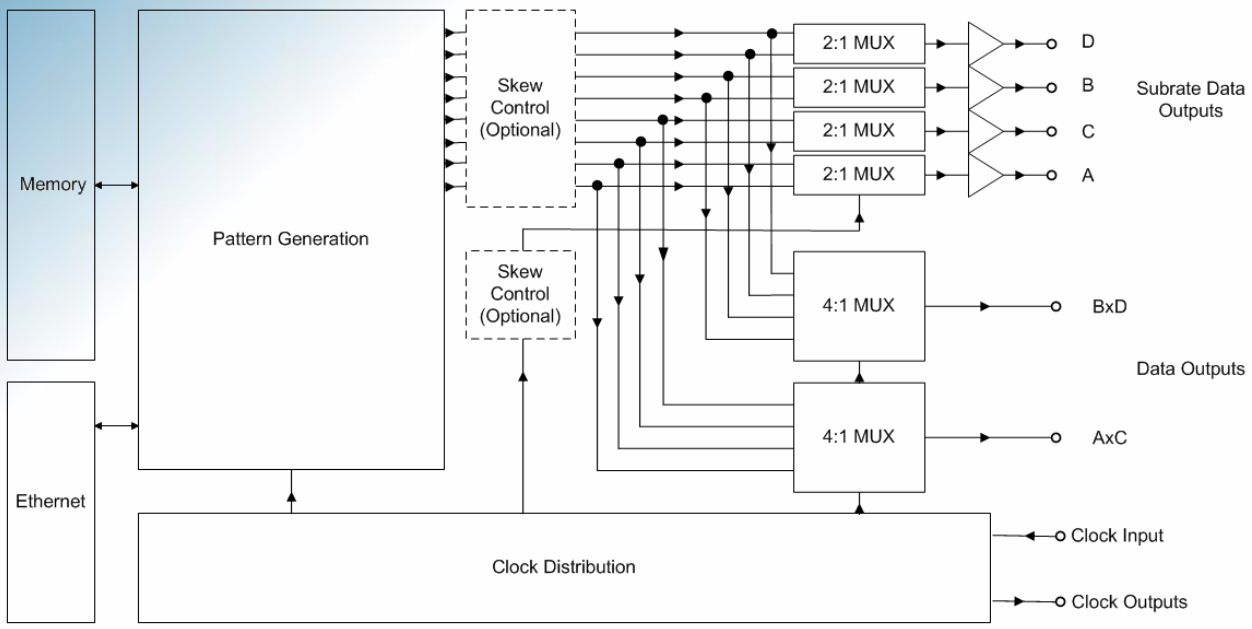
[4] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvoluted} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

[5] For PRBS patterns only. Due to the AC coupling certain user patterns may result in eye amplitudes of up to 2 V.

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Skew Control for 28/32 Gbps Subrate Data Outputs (optional)						
Skew Control Range		ps	-25	0	+25	adjustable in 0.1 ps-steps
Jitter (RMS)	J_{RMS}	fs		500 460	650 620	measured at 32 Gbps on scope display[2] deconvoluted[3]
Clock						
Connector Type Clock Input Clock Output Clock/2 Sel. Clock Output		Ω		50		 ruggedized 1.85 mm (V) male connector ruggedized 1.85 mm (V) male connector ruggedized 2.92 mm (K) male connector ruggedized 2.92 mm (K) male connector
Clock Input Frequency	f_{in_clock}	GHz	3 6 3		28 56 28/32	half clock mode full clock mode sub clock mode
Input Level	V_{in_clock}	mV_{pp}	600		1000	
Output Level Clock Clock/2 Selectable Clock	V_{out_clock}	mV_{pp}	 500 500 500	 600 600 600	 1000 1000 1000	 AC coupled AC coupled AC coupled
Output Frequency Clock Clock/2 Selectable Clock	f_{out_clock}	 GHz GHz GHz	 3 1.5 0.003		 56 28 14	 same as input frequency half of input frequency input frequency/N (N= 4, 8, 16, 32, 64, 128, 256, 512, 1024)
Pattern						
Output Pattern						ITU-T (CCITT) conform PRBS patterns at a length of 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 & 2^{31}-1 plus user defined patterns
User Pattern Memory Size[6]		Gbit			1	
User Pattern Granularity		Bit		1024		
Frame Trigger Output						
Connector Type		Ω		50		SMA female
Output Level Frame		mV		800		AC coupled

[6] See chapter *User Pattern Capabilities* for more details on the user pattern.

Block Diagram



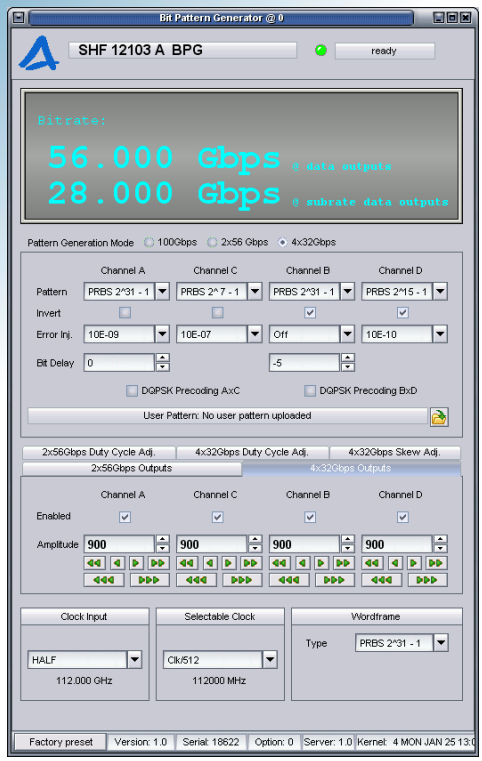
The pattern generator consists of two 4x16 Gbps pattern generation blocks which are synchronized to each other. The outputs of each pattern generation block are 2:1 multiplexed to generate two 32 Gbps outputs. In parallel the outputs of each pattern generation block are 4:1 multiplexed to generate the 56 Gbps outputs. In any configuration where 32 Gbps and 56 Gbps outputs are present at the same time, the 56 Gbps outputs will run at double the speed of the 32 Gbps outputs.

Up to 1 Gbit of user pattern will be stored in a 1024 bit wide memory. Each pattern generation block includes the multiplexers to generate the 4x16 Gbps data streams from the incoming 512 bit wide user pattern data.

The DQPSK precoders are part of the pattern generation blocks, so there is one DQPSK precoder for channels A and C and another one for channels B and D.

The clock distribution section processes the incoming clock signal to generate the clock out, clock/2 out, selectable clock out and word frame signals. Furthermore all clocks needed for the internal components will be generated here.

Output Adjustment Capabilities



Controlling the quad 32 Gbps outputs

Controlling the dual 56 Gbps outputs

Data Rate

The data rate of all outputs is continuously adjustable by a single external clock signal applied to the appropriate input. The 56 Gbps data outputs are always running at a data rate of twice the speed of the subrate outputs.

Output Amplitude

The output amplitude of each channel is adjustable independently.

Pattern Type

All PRBS and user patterns can be assigned individually to each channel.
The patterns of the 32 Gbps subrate outputs are depending on the 56 Gbps outputs; or vice versa (please refer to above block diagram). In case both, 32 Gbps and 56 Gbps outputs are used simultaneously each 56 Gbps output pattern will be virtually 2:1 multiplexed by two 32 Gbps outputs.

Inter-Channel Bit Delay

In case two or more PRBS patterns of the same length are selected it is possible to amend the starting point of each bit sequence (in 1 bit steps up to the total PRBS length).

Inter-Channel Skew (optional)

The timing of each of the 32 Gbps subrate channels can individually be fine adjusted in 0.1 ps steps (please see chapter Skew Control Function for more details).

Duty Cycle

The duty cycle of two consecutive eyes/bits is automatically set to 50%. However, in case the application requires a modification or a further optimization, this could be done with a few clicks.

Hardware DQPSK Precoding

When this checkmark is activated for a pair of 32 Gbps outputs it allows the user to run an error analyzer in PRBS mode while transmitting the data in a DQPSK modulation scheme.

User Pattern Capabilities

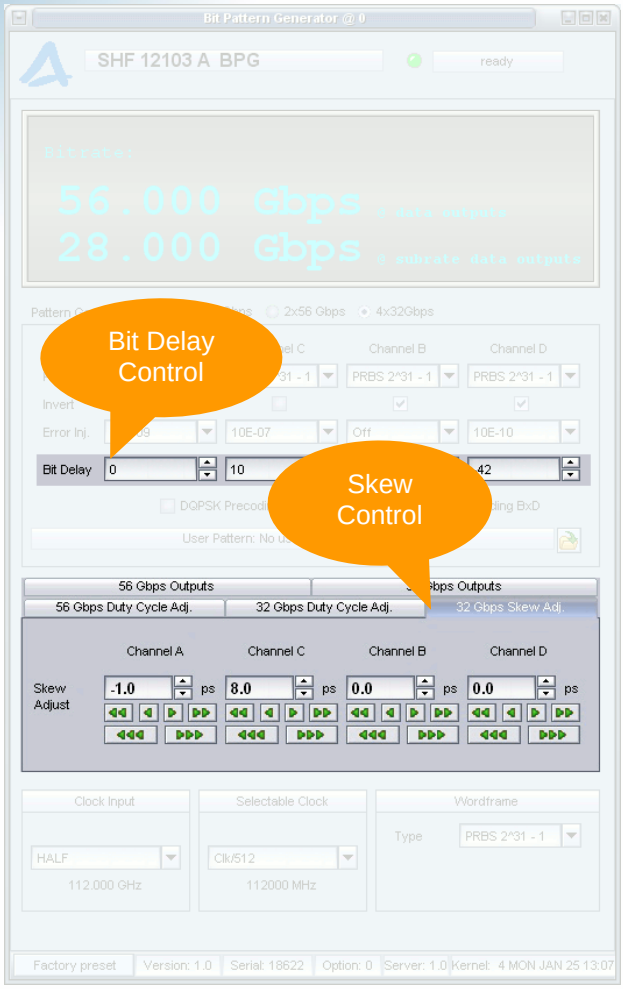
The SHF 12103 A has a built-in 1 Gbit user pattern memory which is attached to the pattern generation blocks by a 1024 bit wide interface to the pattern generation blocks. Data from the user pattern memory will be multiplexed to generate the 56 Gbps and 32 Gbps output data streams. Thus the pattern length of any user pattern uploaded to the user pattern memory has to be a multiple of 1024. User patterns not fulfilling this prerequisite will be repeated automatically by the provided Bert Control Center (BCC) software until the granularity of 1024 is met. For patterns up to 1 Mbit this is always possible. Patterns larger than 1 Mbit have to fulfill the following prerequisites:

Pattern length up to	Pattern length has to be a multiple of
1 Mbit	1
2 Mbit	2
4 Mbit	4
8 Mbit	8
16 Mbit	16
32 Mbit	32
64 Mbit	64
128 Mbit	128
256 Mbit	256
512 Mbit	512
1 Gbit	1024

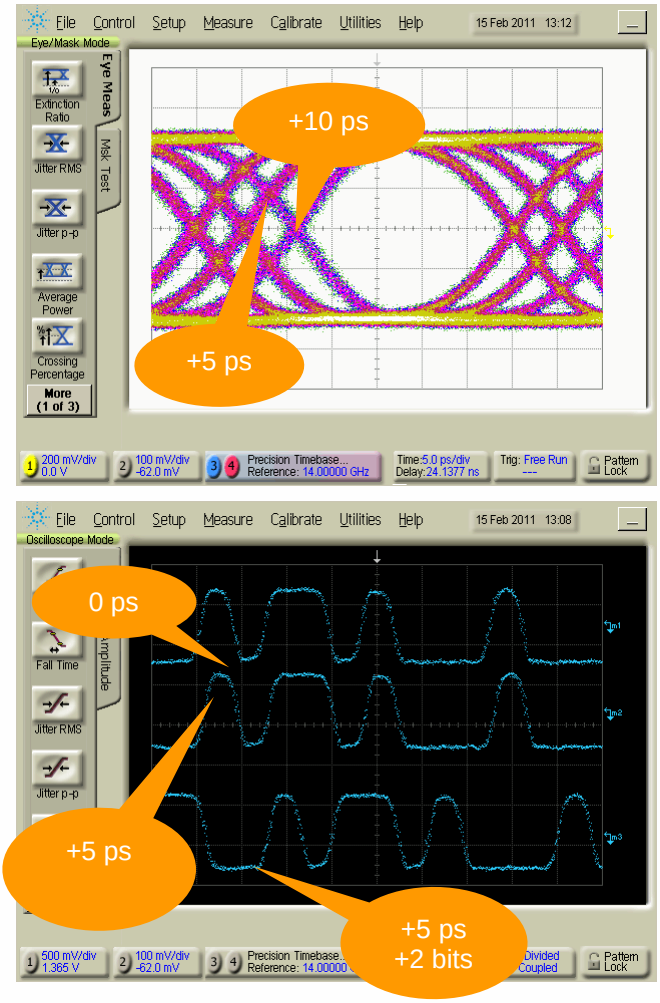
To load individual user patterns for each channel, the patterns have to be merged to upload these into the user pattern memory. This will be handled by the BCC software automatically. The user patterns of all channels have to be of the same size. This will be achieved by the software by repeating the user pattern for each channel until each pattern length is equal to the least common multiple of all patterns lengths. With all patterns having the same length, the BCC software will merge the patterns and will repeat the resulting pattern as described above until the granularity of 1024 bit is met.

Skew Control Function (Optional)

The skew control function allows adjusting the channel timing relative to each other. This is an extra feature on top of the integer bit delay that is already available. As a result, timing delay between individual subrate output channels can be extended greatly over many bit periods, with the skew function for fine adjustment. The figure below shows the BCC control software with this feature, and an example of delay between two subrate channels for skew within a bit and more than one bit.



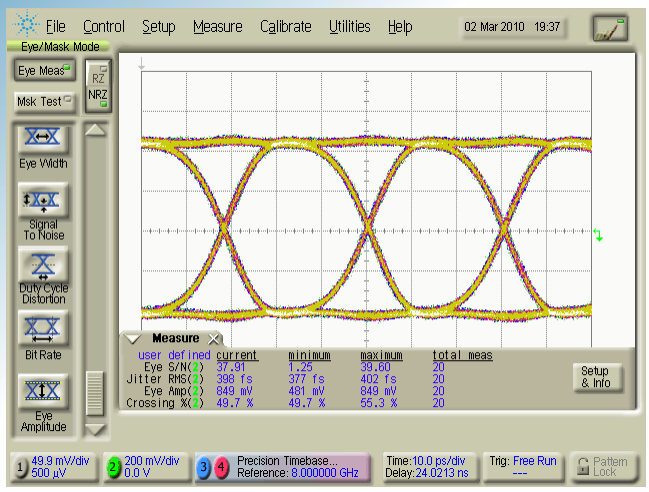
Skew control software representation



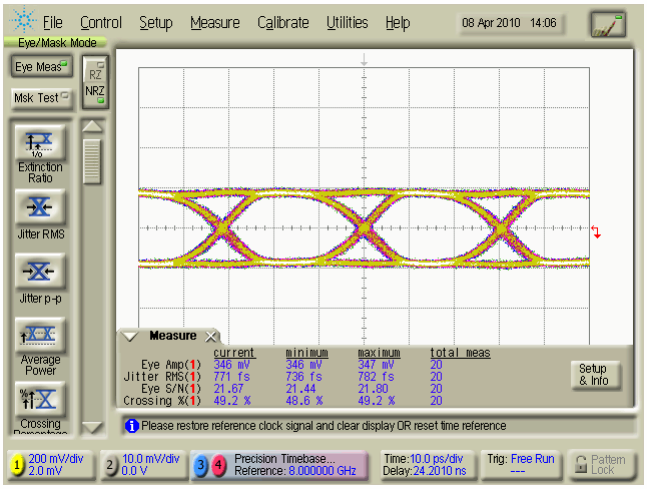
Integer bit delay & skew control

Typical Output Waveforms

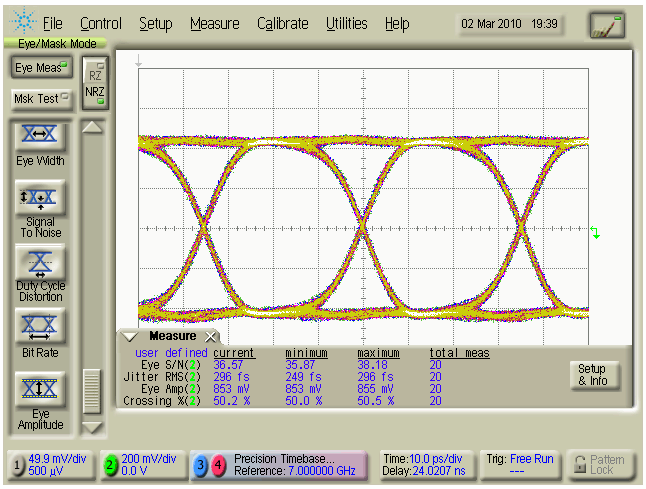
28/32 Gbps Data Output Signals



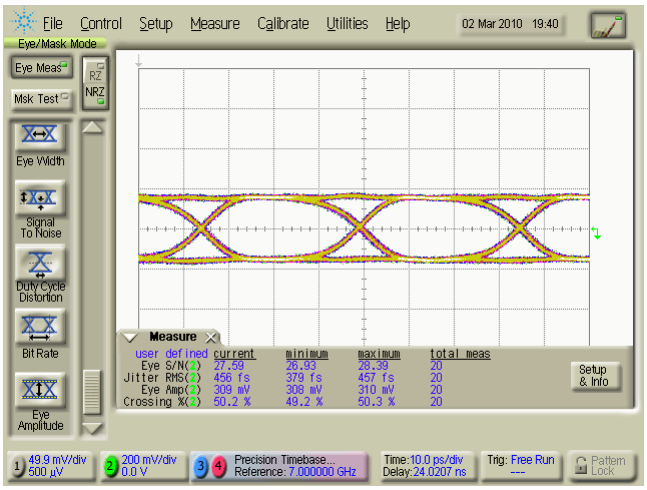
32 Gbps output eye at maximum output level



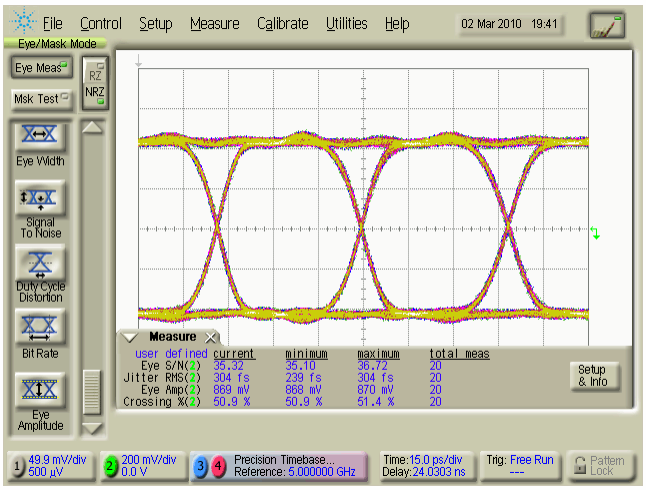
32 Gbps output eye at minimum output level



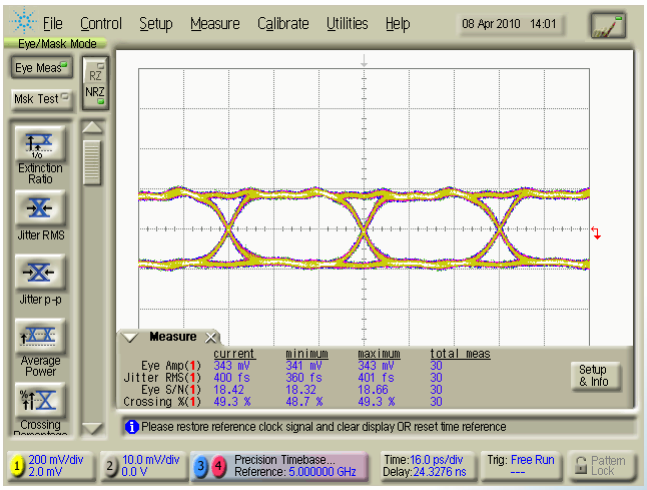
28 Gbps output eye at maximum output level



28 Gbps output eye at minimum output level

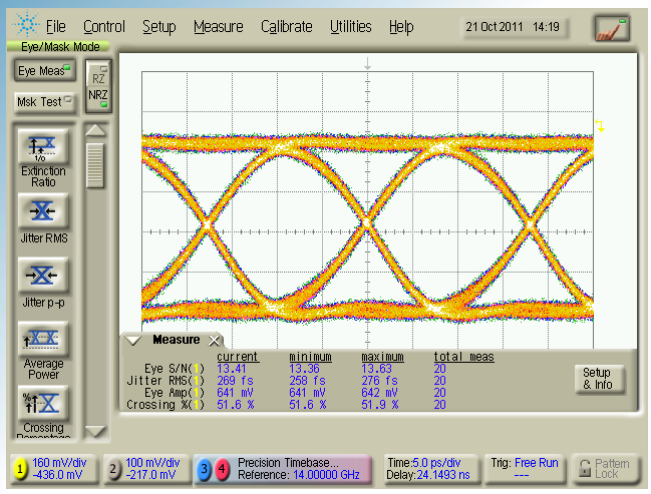


20 Gbps output eye at maximum output level

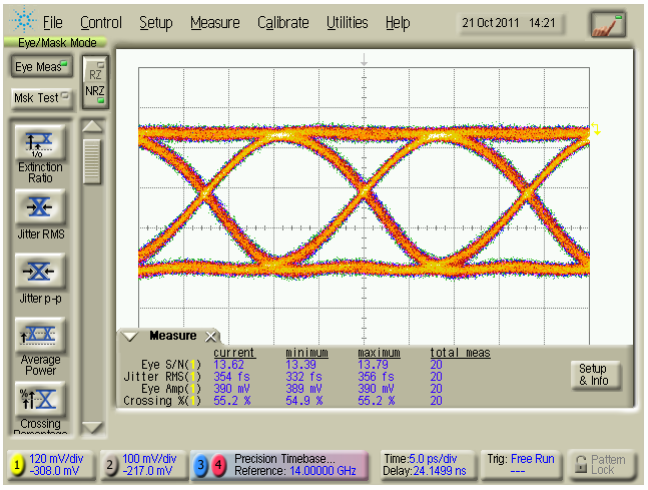


20 Gbps output eye at minimum output level

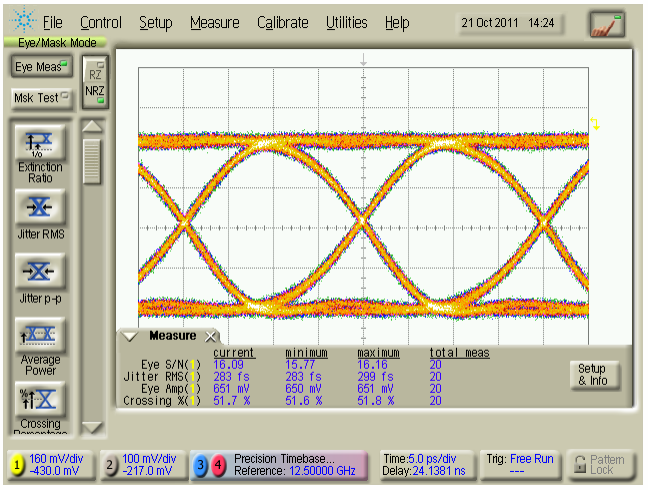
56 Gbps Data Output Signals



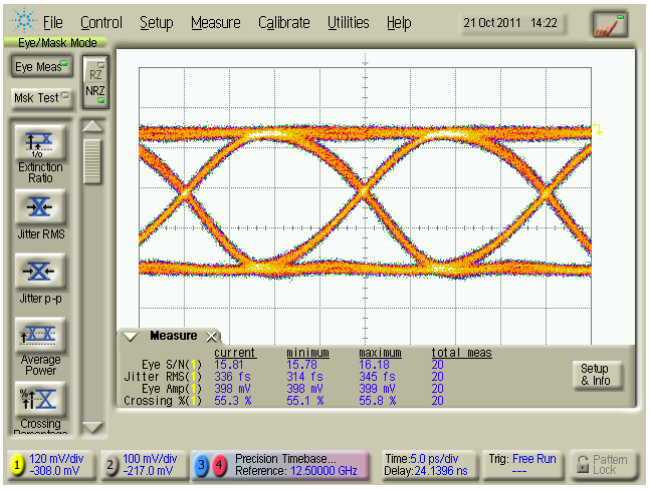
56 Gbps output eye at maximum output level



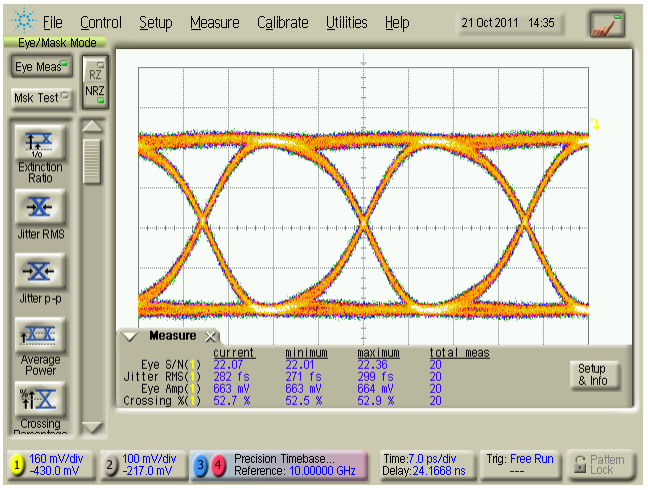
56 Gbps output eye at minimum output level



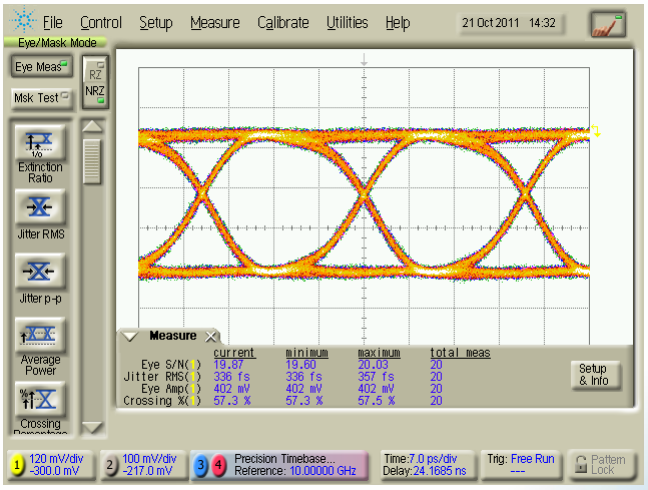
50 Gbps output eye at maximum output level



50 Gbps output eye at minimum output level



40 Gbps output eye at maximum output level



40 Gbps output eye at minimum output level