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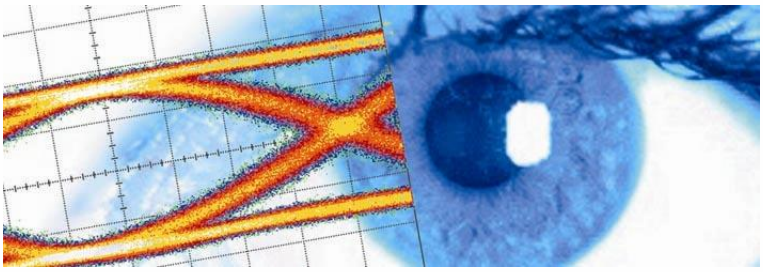

Datasheet

SHF 11125 A

Compact Dual-Channel 32 Gbps Error Analyzer

Description

The SHF 11125 A is a dual-channel 32 Gbps error analyzer (EA). It features two differential data inputs with a high sensitivity and a wide delay range.

The compact instrument analyzes PRBS patterns with lengths of 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, and 2^{31}-1. All operating data rates from 5 to 32 Gbps are supported. This allows bit error rate tests for a variety of different applications including, 100GbE and higher, 28 Gbps CEI, Infiniband®, Fiber channel as well as parallel channel data-com.

The operating bit rate is determined by a clock signal from an external clock source. The channels can work with a common clock to operate at the same or with an individual clock to enable operation at different data rates.

Its compact size and light weight allows a placement very close to the DUT.

Ease of Use

The SHF 11125 A is controlled over a standard Ethernet connection by an external computer (not part of the delivery). Every system comes along with the intuitive, easy to use BERT Control Center software (BCC). The BCC provides the user friendly interface for changing parameters and for taking measurements such as a quick auto-search, Q-factor, jitter or eye contour analysis.

Further the unit allows for additional customization to suit the intended test and measurement applications, be it for system R&D or in the production environment.

Features

- Two differential input channels
- 5 to 32 Gbps operation, ‘gap-free’
- PRBS 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, 2^{31}-1
- Individual or common clock input
- Two clock outputs for trigger purposes
- Compact size and low power consumption
- High Sensitivity and wide delay range
- Extensive measurement capabilities such as quick auto-search, Q-factor, jitter and eye-contour

Applications

- On-Wafer Testing
- CEI-28G
- 100G Ethernet
- Infiniband
- Fibre Channel ®
- High Speed Serial Backplane Applications

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Specifications – SHF 11125 A

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
32 Gbps Data Inputs						
Minimum Bit Rate	R_{min}	Gbps			5	
Maximum Bit Rate	R_{max}	Gbps	32	33		
Threshold Adjustment	$V_{threshold}$	mV	-240		240	Adjustable in 0.5 mV steps
Sensitivity[1]	V_{in}	mV		30	50	
Delay / Clock Phase Adjustment		ps	0		140	Adjustable in 0.1 ps steps
Clock Phase Margin[2]	CPM	°	200			
Max. Input Amplitude	V_{in}	mV_{pp}			800 1000	Single ended Differential Input AC coupled
Connectors						2.92 mm (K) female
Clock Inputs						
Frequency	f	GHz	2.5		16	Half clock operation
Input Level	P_{in}	dBm	0		4	
Connectors						2.92 mm (K) female
Clock Outputs						
Frequency	f	GHz	2.5		16	Clock
Output Level	V_{out}	mV	350	450	700	Clock/2, AC coupled
Connectors						2.92 mm (K) female

[1] Corresponds to the measured eye height on an Agilent 86100 C with 70 GHz sampling heads using 2^{31}-1 PRBS at a BER limit of 10^{-9}

[2] BER limit 10^{-9}, PRBS: 2^{31}-1, Eye Height: 100 mV_{pp}, Peak-to-Peak-Source-Jitter as displayed on an Agilent 86100 B with 70 GHz sampling heads and precision time base, calculated using the formula:

$$\text{Clock Phase Margin}[°] = 360° \cdot \frac{\text{Measured Clock Margin}[ps] - (\text{Peak - to - Peak - Source - Jitter}[ps])}{\text{Eye Length}[ps]}$$

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Pattern						
Input Pattern						ITU-T (CCITT) conform PRBS patterns at a length of 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 & 2^{31}

General						
Supply Voltage	Vee	V	11.5	12	12.5	
Power Consumption	P_{tot}	W		25		+12V switching power supply is included
Height	H	mm		64		
Width	W	mm		116		
Depth	D	mm		183		
Weight	m	g			500	
Case Temperature	T_{case}	°C			40	

Clock Distribution

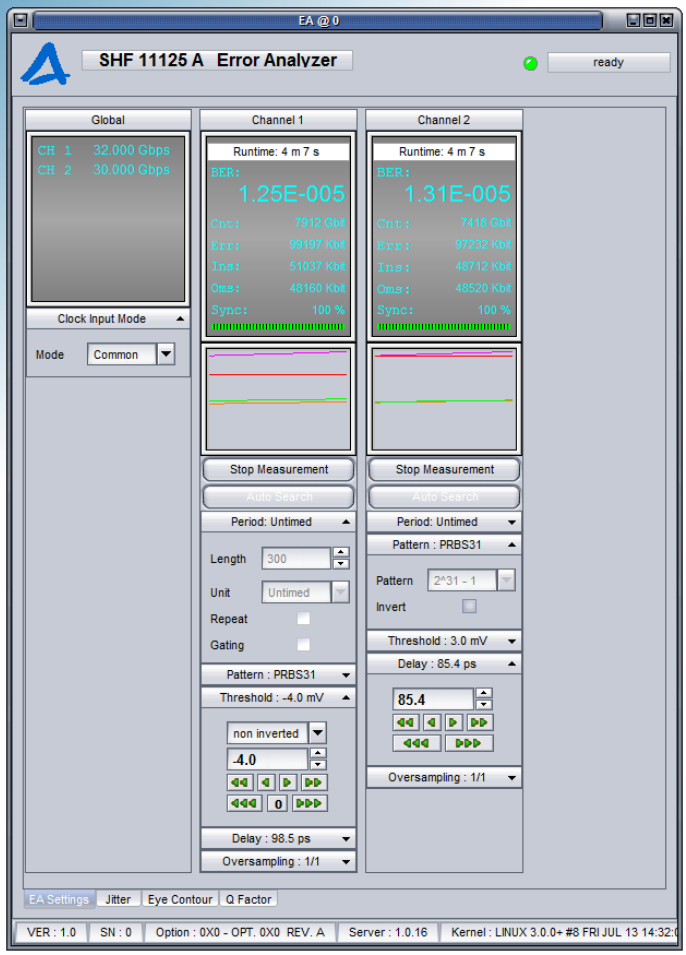
The operating bit rate is determined by a clock signal from an external clock source which is not part of the error analyzer. The error analyzer operates at half clock rate, e.g. a 15 GHz clock signal is required for 30 Gbps operation.

In common clock mode the unit operates with one single clock signal. In this case both data inputs operate at the same data rate. A phase change of the clock signal will result in the same phase change at both data inputs.

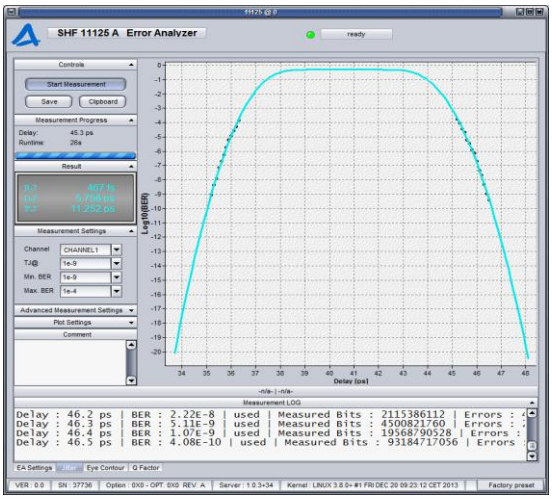
In individual clock mode each data input has his designated clock input. Thus the individual channels can work at different data rates. An asynchronous phase wander in the two channels will not require a delay adjustment during error analysis if the (recovered) individual clocks keep track. This is very useful even if both channels operate at the same data rate.

For trigger purposes each channel provides a copy of the input clock signal at the clock output at the rear panel of the instrument

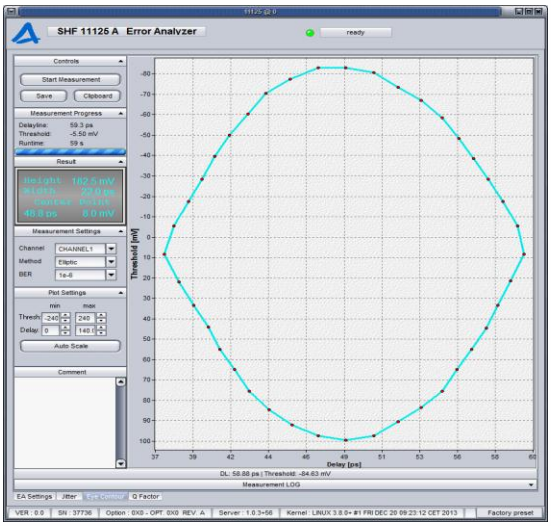
Graphical User Interface



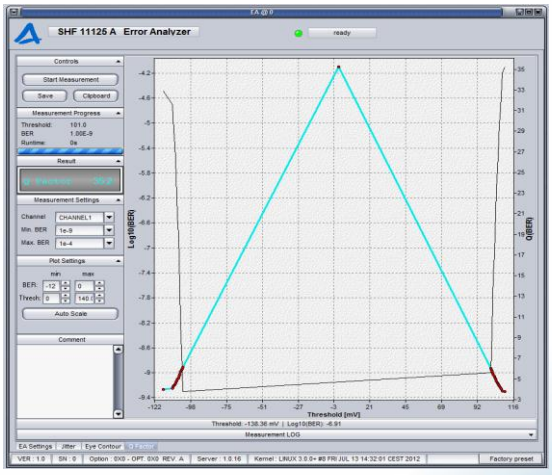
BERT Control Center Software Main Window



Jitter Measurement



Eye Contour Measurement



Q-Factor Measurement

Outline Drawing