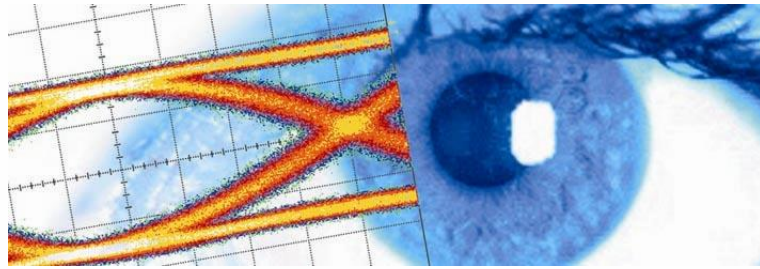# SHF Communication Technologies AG

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Datasheet
SHF 11104 A
Multi-Channel Error Analyzer

Description

The SHF 11104 A is a multi-channel 33/60/64 Gbps error analyzer (EA) plug-in, to be fitted in a SHF 10000 Series mainframes. It analyzes binary (NRZ) or PAM4 digital bit sequences. The data can be pseudo-random (PRBS) or user patterns.

A wide range of operating bit rates from 4.8-64 Gbps is covered. Depending on the configuration, the instrument features up to four 64 Gbps or up to eight 33 Gbps inputs, or a mix of 64 and 33 Gbps input channels. See selection table for possible configurations.

The operating bit rate range is determined by a clock signal from an external clock source such as the SHF 78210 D. The 60/64 Gbps inputs can operate at both full clock and half clock, so e.g. a 20 GHz or a 40 GHz signal is required for 40 Gbps operation. The 33 Gbps inputs operate at full clock only; therefore a 33 GHz signal is required for 33 Gbps operation.

Features

- Multiple 60/64 Gbps and 33 Gbps data input channels
- Broadband operation up to aggregated 264 Gbps
- Eight built-in PRBS patterns (2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 & 2^{31})
- Up to 8 Gbit user pattern memory per channel to support user defined patterns
- Individual auto search of optimum sampling point for each channel
- All inputs can be used in single ended or differential mode
- Q-factor analysis for each channel
- Jitter analysis for each channel
- Eye contour analysis for each channel
- PAM4 analysis capability for PRBS patterns and user patterns like PRBS13Q and SSPRQ
- Error trigger output
- Gating input for loop experiments
- Control by intuitive graphical user interface BERT Control Center (BCC)
- Individual clock input per channel for selected configurations

Applications

The SHF 11104 A is the ideal error analyzer (EA) for basically any application in R&D or production which needs to test high speed data streams for electrical/optical components or transmission systems. The flexible channel configuration possibilities, the broad band gap-free data rate coverage and the advanced features make this error analyzer the perfect fit e.g. for

- single channel applications
  e.g. OC-768/STM-256 (using 40 Gbps NRZ or DPSK), CEI 56G, Fiber Channel®, PCI Express, Serial ATA

- multi-channel applications
  e.g. OC-768/STM-256 (using 20 GBaud QPSK), 100GbE (using 32 GBaud DP-QPSK), 400 GbE (using 8x 56.2 Gbps)

- multi-level applications
  e.g. 100GbE (using 2x 28 GBaud PAM4), 400 GbE (using 8x 28 GBaud PAM4)

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Configurations and Options

The SHF 11104 A can be equipped in a variety of different configurations; either with 60/64 Gbps or 33 Gbps data inputs only or with both types of inputs fitted together in one plug-in.

60/64 Gbps Data Inputs

- Quad 60   - Four differential channels from 9.6 to 60 Gbps
- Dual 60   - Two differential channels from 9.6 to 60 Gbps
- Single 60   - One differential channel from 9.6 to 60 Gbps

- Quad 64   - Four differential channels from 9.6 to 64 Gbps
- Dual 64   - Two differential channels from 9.6 to 64 Gbps
- Single 64   - One differential channel from 9.6 to 64 Gbps

33 Gbps Data Inputs

- Oct 33   - Eight differential channels from 4.8 to 33 Gbps
- Quad 33   - Four differential channels from 4.8 to 33 Gbps
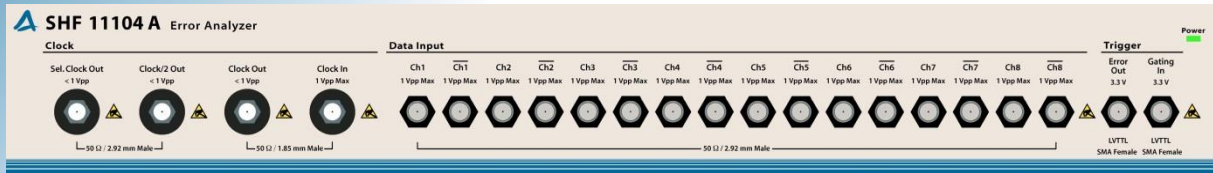- Dual 33   - Two differential channels from 4.8 to 33 Gbps

Available Combinations

	No 33 Gbps	Dual 33 Gbps	Quad 33 Gbps	Oct 33 Gbps
No 60/64 Gbps		✔ ℹ	✔ ℹ	✔
Single 60/64 Gbps	✔	✔	✔	
Dual 60/64 Gbps	✔	✔	✔	
Quad 60/64 Gbps	✔			

ℹ : Individual clock inputs to enable multi-channel analysis at different bit rates inclusive

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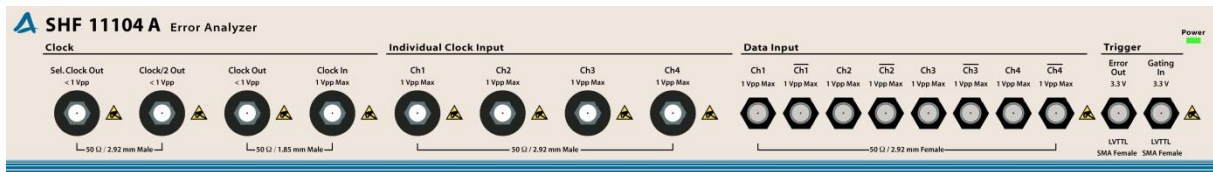the bandwidth company

Configuration Examples

SHF 11104 A in Configuration Oct 33
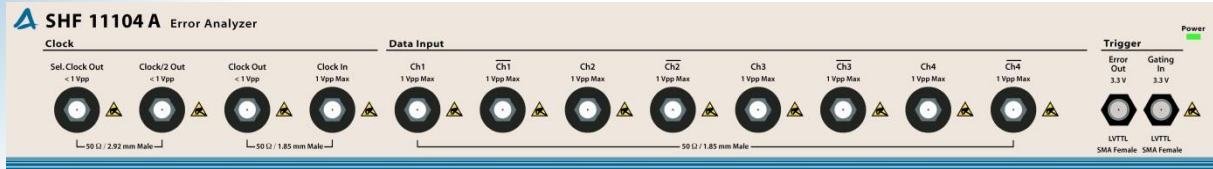
SHF 11104 A in Configuration Quad 60/64

SHF 11104 A in Configuration Quad 33 (with individual clock inputs)

Options

SHF offers matching external modules to de-multiplex a high speed signal into two data streams at half of the original high speed signal before applying the demultiplexed data to the SHF 11104 A.

Such an extender can be placed very close to or even directly at the device under test. In order to serve the individual configuration and testing needs SHF provides the modules without any cabling. However, we would be very happy to add the required clock and data cables tailored to the individual setups.

Option Extender SHF 621 A

One 60 Gbps data stream can be de-multiplexed externally by the SHF 621 A before being applied to two 30G input channels. For details please be referred to the data sheet of the SHF 621 A.

Specifications – SHF 11104 A

60/64 Gbps Data Inputs

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		8	9.6	
Maximum Bit Rate in 60 Gbps configuration		Gbps	60	62		Bit rates above 56 Gbps require half clock mode
Maximum Bit Rate in 64 Gbps configuration		Gbps	64	65		Bit rates above 56 Gbps require half clock mode
Minimum Baud Rate for PAM4 Measurements		GBaud		8	9.6	
Maximum Baud Rate for PAM4 Measurements		GBaud	32	33		
Threshold Adjustment	$V_{threshold}$	mV	-240		240	Adjustable in 0.5 mV steps
Sensitivity [1]	V_{in}	mV		25	50	Up to 64 Gbps
PAM4 Sensitivity[2]		mV		20	40	Up to 32 GBaud
Delay / Clock Phase Adjustment		ps	0		70	Adjustable in 0.1 ps steps
Clock Phase Margin [3]	CPM	°	200			
Max. Input Amplitude	V_{in}	mV_{pp}			900	AC coupled
Max. Input DC Voltage	V_{in_DC}	V	-5		+5	
Connectors						1.85 mm (V) male

Typical Sensitivity

Typical Clock Phase Margin

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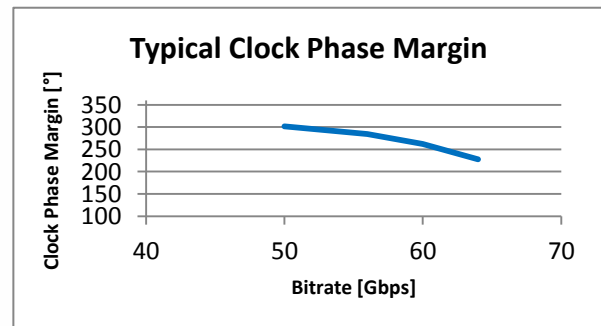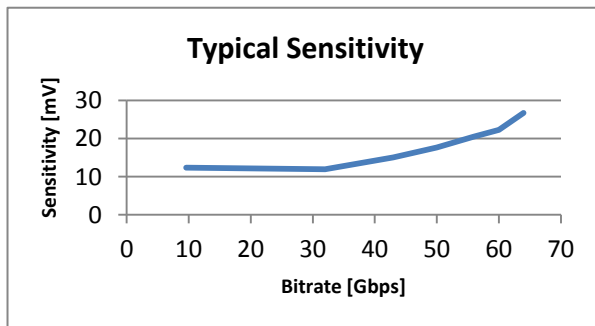
[1] Value corresponds to the measured eye height on an Agilent 86100 C with 70 GHz samplers using 2^{31}-1 PRBS at a BER limit of $10^{-9.}$

[2] Value corresponds to the measured eye heights of a symmetric PAM4 signal on an Agilent 86100 C with 70 GHz samplers using 2^{23}-1 PRBS at a BER limit of $10^{-9.}$
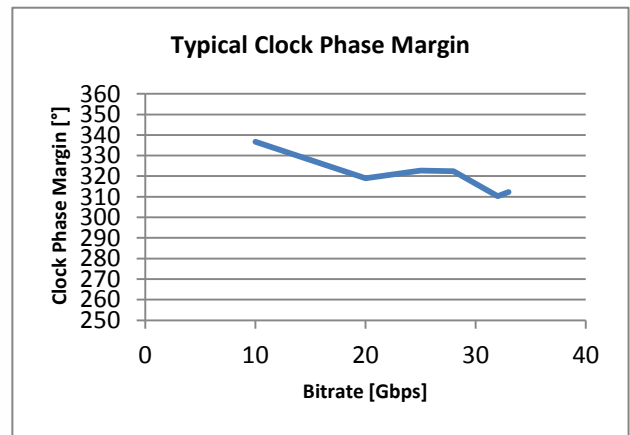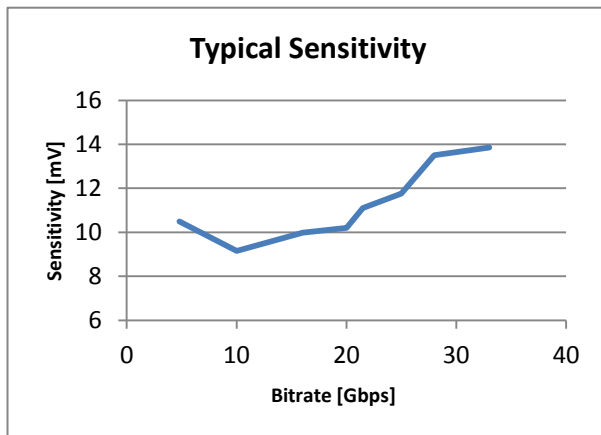
[3] BER limit 10^{-9}, PRBS 2^{31}-1, eye height 100 mV, Peak-to-Peak-Source-Jitter as displayed on an Agilent 86100 with 70 GHz sampling heads and precision time base, calculated using the formula:

$$\text{Clock Phase Margin}[°] = 360° \cdot \frac{\text{Measured Clock Margin[ps]} - (\text{Peak-to-Peak-Source-Jitter [ps]})}{\text{Eye Length [ps]}}$$

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33 Gbps Data Inputs

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Minimum Bit Rate		Gbps		4	4.8	
Maximum Bit Rate		Gbps	33	34		
Minimum Baud Rate for PAM4 Measurements		Gbps		4	4.8	
Maximum Baud Rate for PAM4 Measurements		Gbps	32	33		
Threshold adjustment	$V_{threshold}$	mV	-240		240	Adjustable in 0.5 mV steps
Sensitivity[4]	V_{in}	mV		15	30	
Sensitivity PAM4[5]					60	
Delay / Clock Phase Adjustment		ps	0		140	Adjustable in 0.1 ps steps
Clock Phase Margin[6]	CPM	°	250			
Max. Input Amplitude	V_{in}	mV_{pp}			900	AC coupled
Max. Input DC Voltage	V_{in_DC}	V	-5		+5	
Connectors						2.92 mm (K) female

Typical Sensitivity

Typical Clock Phase Margin

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[4] Value corresponds to the measured eye height on an Agilent 86100 with 70 GHz samplers using 2^{31}-1 PRBS at a BER limit of 10^{-9}.

[5] Value corresponds to the measured eye height of a symmetric PAM4 signal on an Agilent 86100 with 70 GHz samplers using 2^{23}-1 PRBS at a BER limit of 10^{-9}.

[6] BER limit 10^{-9}, PRBS 2^{31}-1, eye height 100 mV, Peak-to-Peak-Source-Jitter as displayed on an Agilent 86100 with 70 GHz sampling heads and precision time base, calculated using the formula:

$$\text{Clock Phase Margin}[°] = 360° \cdot \frac{\text{Measured Clock Margin}[ps] - (\text{Peak-to-Peak-Source-Jitter}[ps])}{\text{Eye Length}[ps]}$$

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Clock and Trigger Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Connector Type Clock Input Clock Output Clock/2 Output Selectable Clock Output		Ω		50		ruggedized 1.85 mm (V) male connector ruggedized 1.85 mm (V) male connector ruggedized 2.92 mm (K) male connector ruggedized 2.92 mm (K) male connector
Minimum Clock Input Frequency	f_{in_clock}	GHz			4.8 9.6	half clock mode full clock mode
Maximum Clock Input Frequency	f_{in_clock}	GHz	30 56			half clock mode full clock mode
Maximum Clock Input Frequency with Option "64 Gbps" Input	f_{in_clock}	GHz	32 56			half clock mode full clock mode
Clock Input Frequency Individual Clock	f_{in_clock}	GHz	2.4		16.5	for 33 Gbps inputs
Input Level	V_{in_clock}	mV$_{pp}$	600		1000	AC coupled
Output Level Clock Output Clock/2 Output Selectable Clock Output	V_{out_clock}	mV$_{pp}$	500 500 400	700 800 600	1000 1000 800	AC coupled, @P_{in} = 0 dBm AC coupled, AC coupled
Output Frequency Clock Clock/2 Selectable Clock Output	f_{out_clock}	GHz	4.8 1.2 0.0023		56 28 14	same as input frequency half of input frequency input frequency/N (N=4,8,16,32,64,128,256, 512,1024)
Gating Trigger Input						
Input Voltage High		V	2.0	3.3	5	LV TTL, SMA female
Input Voltage Low		V	0	0	0.8	LV TTL, SMA female
Error Trigger Output						
Output Voltage High		V	2.4	3.3	3.8	LV TTL, SMA female
Output Voltage Low		V	0	0	0.4	LV TTL, SMA female

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Pattern Specifications

Parameter	Symbol	Unit	Min.	Typ.	Max.	Comment
Input Pattern						ITU-T (CCITT) conform PRBS patterns at a length of 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 & 2^{31}-1 plus user defined
Real Time User Pattern Memory Size for 33 Gbps Data Inputs		Gbit			4	Per Channel See Chapter User Pattern Capabilities
Real Time User Pattern Memory Size for 60/64 Gbps Data Inputs		Gbit			8	Per Channel See Chapter User Pattern Capabilities
Real Time User Pattern Granularity for 33 Gbps Data Inputs		Bit		512		See Chapter User Pattern Capabilities
Real Time User Pattern Granularity for 60/64 Gbps Data Inputs		Bit		1024		See Chapter User Pattern Capabilities

Input Adjustment Capabilities
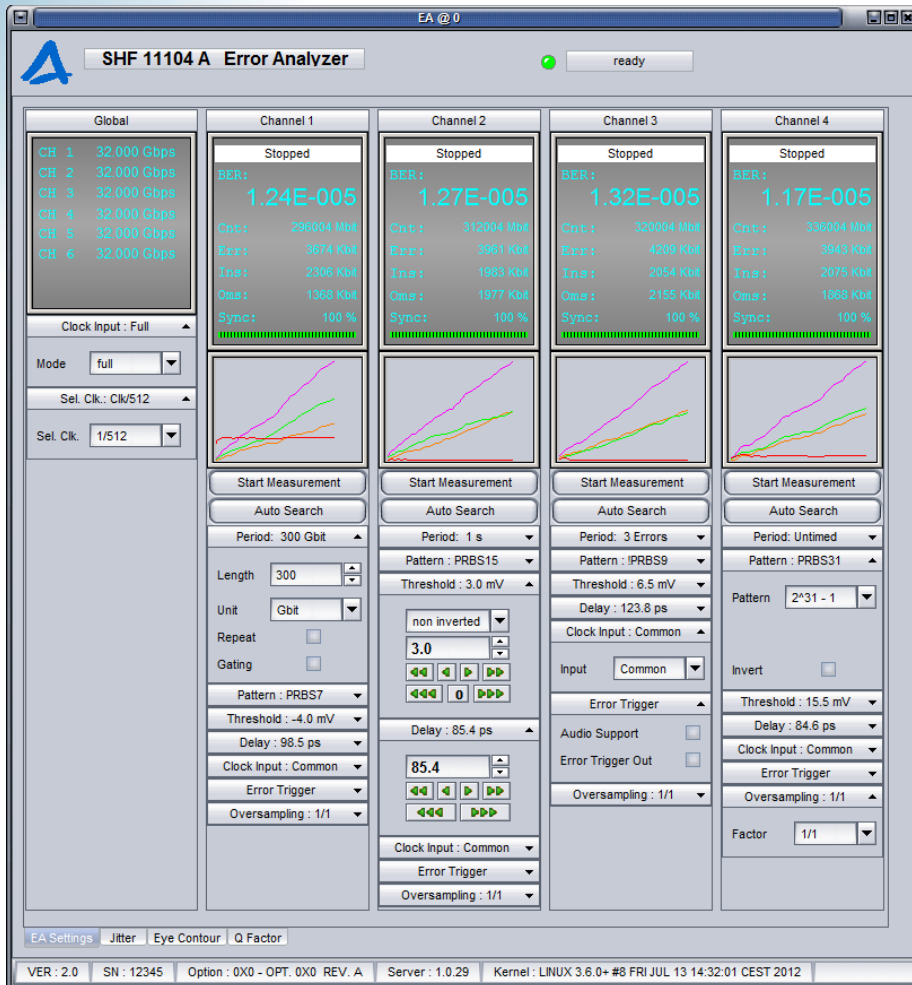
Data Rate

The data rate of all inputs is continuously adjustable by a single external clock signal applied to the clock input. The 60/64 Gbps data inputs are always running at a data rate of twice the speed of the 33 Gbps data inputs. For configurations Dual 33 and Quad 33 each channel may be driven by an individual clock allowing different bit rates for each channel.

Pattern Type

All PRBS and user patterns can be assigned individually to each channel.

Delay / Threshold

The decision point of each channel can be adjusted using the delay and threshold settings.

Auto Search

To facilitate finding the best decision point an auto search function is available to determine the delay and threshold values.

Error Trigger

If selected an error at one of the channels triggers a signal at the Error Trigger Output. Further an error rate dependent sound can be played. These features allow the optimization of the setup without having to watch the error rate on the BERT Control Center display.

User Pattern Capabilities

In addition to the pre-defined PRBS patterns, arbitrary user-defined patterns can also be analyzed.

The user pattern is analyzed in 'real time mode'. This means, the user does not need to load an externally created pattern into the error analyzer. One only has to define the length of the pattern and the error analyzer will capture and store the first incoming bit stream of this length into its internal memory. Subsequent incoming data is compared to the data stored within the internal memory. Therefore it is possible to measure a continuous bit stream without any gaps[7,8].

Granularity Requirement

The maximum available user pattern is 8,589,934,592 bit (1 Gigabyte, approx. 8 Gbit) per 60/64 Gbps channel and 4,294,967,296 bits (512 Mbyte, approx. 4 Gbit) per 33 Gbps channel. Due to the internal architecture of the error analyzer the user pattern lengths has to be a multiple of 1024 bits for the 60/64 Gbps inputs or 512 bits for the 33 Gbps inputs.

In case this granularity requirement is not met, the EA will automatically record the pattern as often as required until the condition is satisfied. For example, in case a 127 bit long data stream shall be analyzed, the length of the *real recorded pattern* is 127 * 1024 = 130,048 bits when using the 60/64 Gbps inputs.

For significantly longer patterns (patterns longer than 8,388,608 bits) in can happen that the *real recorded pattern* length does exceed the memory size, although the actual size of the user pattern is smaller than the available memory. The actually available user pattern memory is shown below.

Maximum user pattern (bits)	in case the word lengths is dividable by	
	60/64 Gbps inputs	33 Gbps inputs
8,589,934,592	1024	N/A
4,294,967,296	512	512
…	…	…
33,554,432	4	4
16,777,216	2	2
8,388,608	1	1

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[7] The details are documented in the application note: *Real time user pattern BER analysis with the SHF 11104A error analyzer.*

[8] The incoming data stream is internally de-multiplexed into sub-channels. Each individual sub channel requires an alternating pattern. As a consequence a 1010 pattern cannot be measured, as the sub-channels would see a constant '1' or '0' and no alternating pattern.

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Error Counting with Real Time User Pattern

Ideally the real recorded reference pattern used by the error analyzer should be error free. The conditions for error free reference patterns are described below.

The probability p to detect no errors within a bit stream of length n and a bit error ratio BER can be expressed by the following expression derived from the binomial distribution:

$$p = (1 - BER)^n$$

The following table lists the probability to receive an error free real recorded pattern for different pattern length for the 60/64 GBit/s input channels.

A PRBS 2^7 -1 pattern requires 127*1024= 130,048 Bits, a PRBS 2^{23}-1 pattern 8,388,607*1024 = 8,589,933,568 Bits to be recorded. The probability to record and assure an error-free segment depends on the lengths of the *real recorded pattern* and the actual BER.

BER	Pattern length: 1024 Bits	Probability (in %) to record error free pattern		
		Pattern length: 130,048 Bits (PRBS7*1024)	Pattern length: 33553408 Bits (PRBS15*1024)	Pattern length: 8,589,933,568 Bits (PRBS23 * 1024)
10^{-4}	90.266	0.000	0.000	0.000
10^{-5}	98.981	27.240	0.000	0.000
10^{-6}	99.898	87.805	0.000	0.000
10^{-7}	99.990	98.708	3.490	0.000
10^{-8}	99.999	99.870	71.496	0.000
10^{-9}	100.000	99.987	96.700	0.019
10^{-10}	100.000	99.999	99.665	42.359
10^{-11}	100.000	100.000	99.966	91.769
10^{-12}	100.000	100.000	99.997	99.145

Error free recorded user patterns cannot always be assured. For such cases a statistical approach interpreting the measurement data is possible[9].

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[9] The details are documented in the application note: *Real time user pattern BER analysis with the SHF 11104A error analyzer.*

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Jitter Measurements
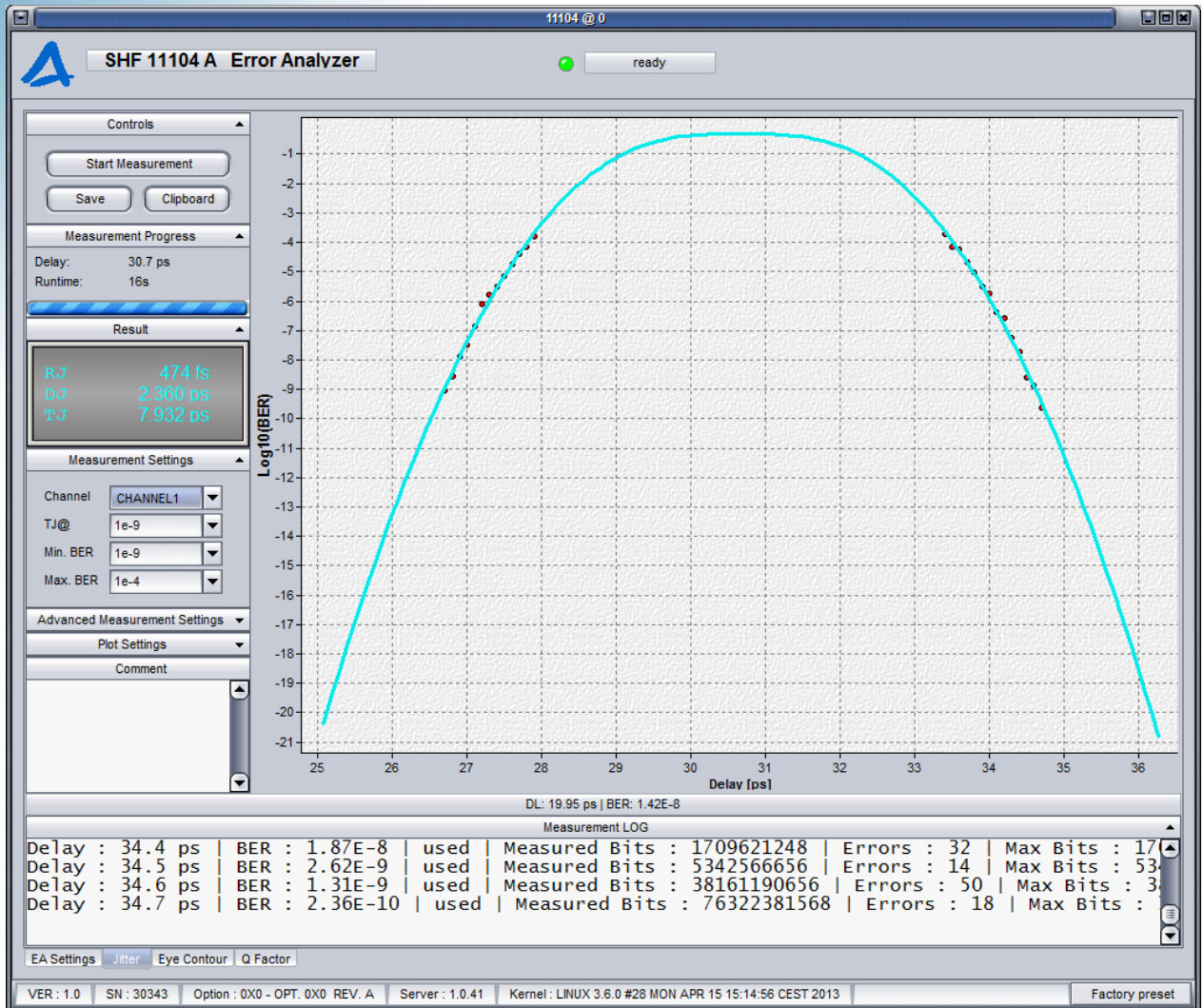
The SHF 11104 A has built-in jitter analysis functionality. This performs a BER scan and calculates random, deterministic and total jitter components from the measurement results. For further refinement of the results the BER scan parameters can be adjusted. There are two different algorithms available for the jitter calculation.

The results of the BER scan and the jitter analysis can be exported for further analysis.

Further information about this program and the theory used in deriving the jitter values can be found in the SHF application note "*Jitter Analysis using SHF 10000 Series BERT Equipment*" on our web site (www.shf.de/)

Eye Contour Scan
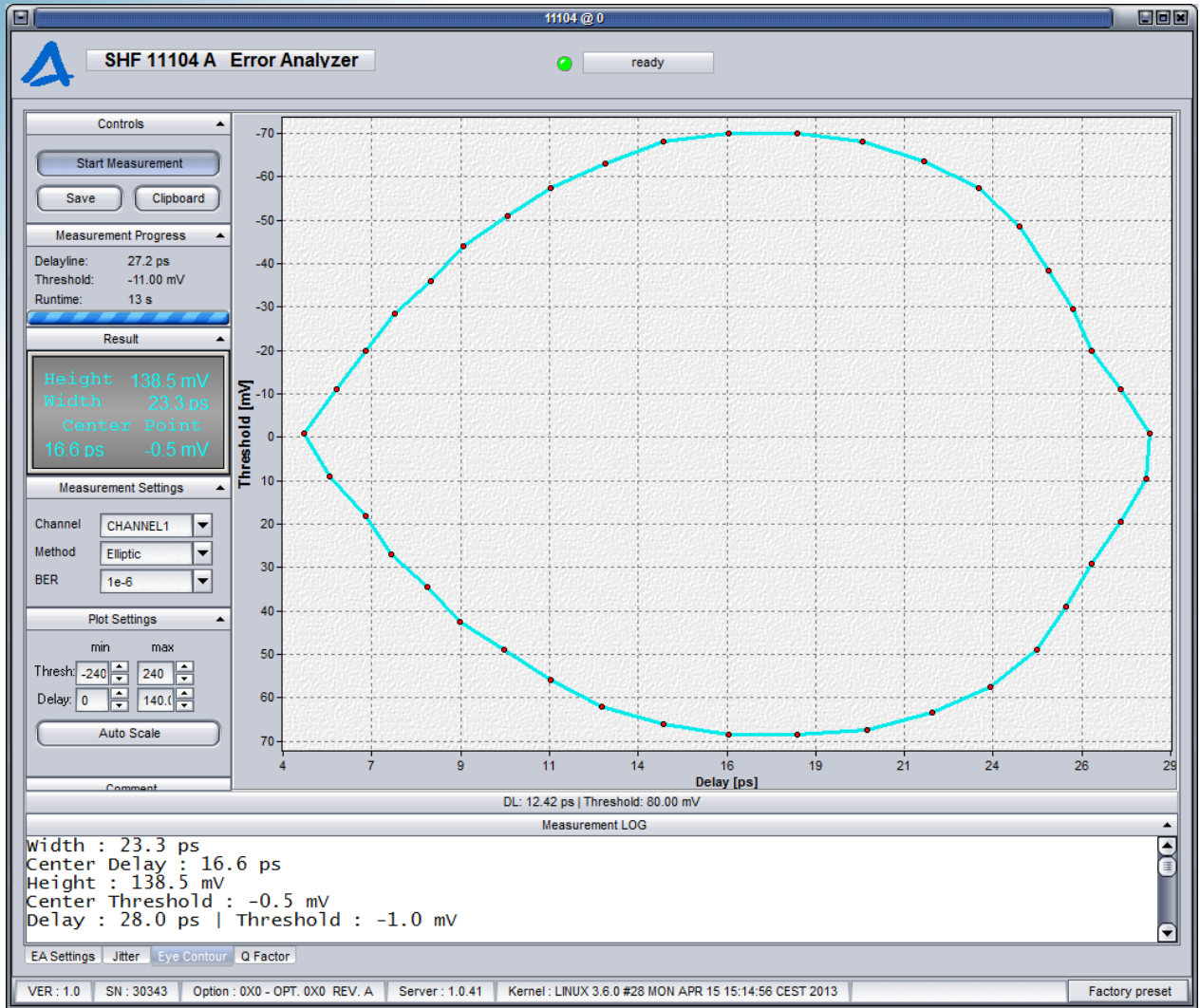
The SHF 11104 A has built-in eye contour scan functionality. This performs an eye scan along a user specified BER threshold. The eye scan algorithm also determines the center point of the detected eye which can be used as the decision point for further BER measurements.

The results of the eye contour scan can be exported for further analysis.

Q-Factor Measurement
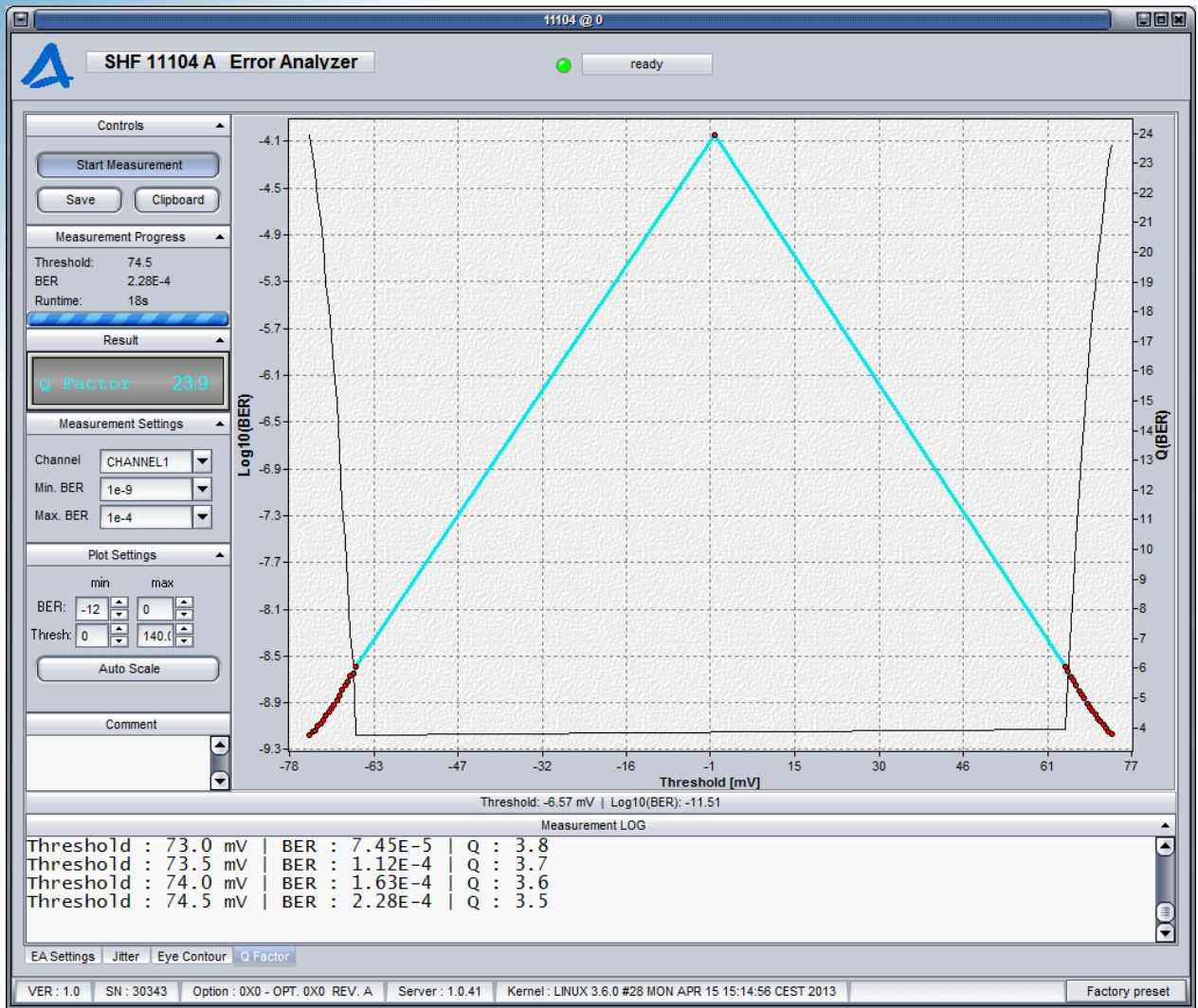
The SHF 11104 A has built-in Q-Factor analysis functionality. This performs a BER scan and will calculate the Q-Factor from the measurement results. For further refinement of the results the BER scan parameters can be adjusted.

The results of the BER scan and the Q-Factor analysis can be exported for further analysis.

PAM4 Measurements

The error analyzer can be used to analyze PAM4 signals of up to 32 GBaud.

To perform BER measurements of the PAM4 signal, the error analyzer successively samples all eye openings of the 4-level eye and calculates the individual bit error ratios. There are two operation modes for error counting:

Hardware Decoding (PRBS) Mode

For data streams generated from PRBS data without any encoding the error analyzer includes an internal hardware decoding where the EA synchronizes its internal reference generators to the two data streams coded into the PAM4 signal. In this mode the EA is able to detect data generated from a PRBS data stream up to PRBS 2^{31}-1.

Real Time User Pattern Mode

For coded PAM4 signal like QPRBS13 or non-PRBS patterns like SSPRQ the EA operates in real time user pattern mode. Please refer to the chapter *User Pattern Capabilities* for further details on the pattern length and operating principles.

In all modes the error analyzer offers an auto search algorithm determining the decision for each of the 4-level signal. This auto search algorithm can perform either a quick four point search or a more detailed eye contour scan as shown in the screenshot below. Jitter Measurements for each eye are supported as well as eye contour measurements.
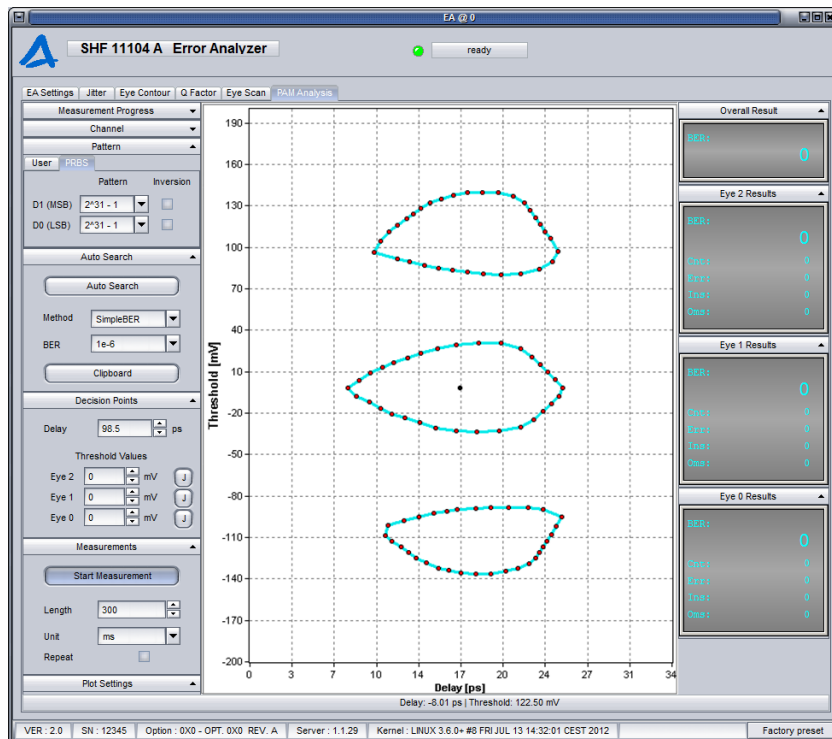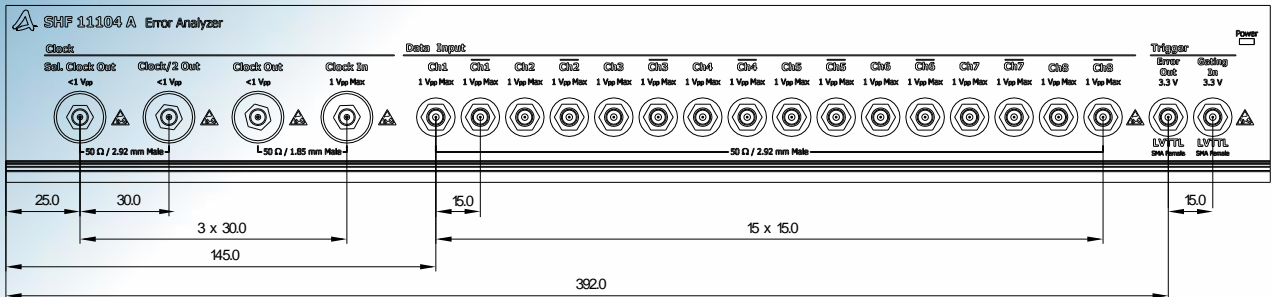

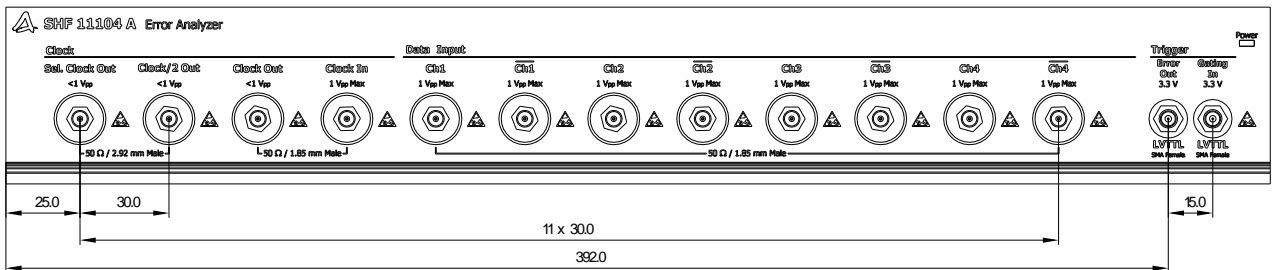For PAM4 signals the overall BER will be calculated according to the following formula:

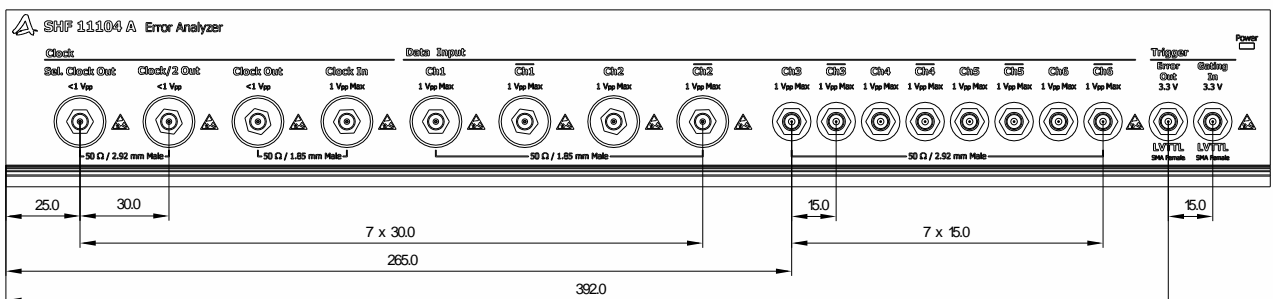$$BER_{Total} = \frac{1}{2} BER_{Eye2} + BER_{Eye1} + \frac{1}{2} BER_{Eye0}$$

Outline Drawings

SHF 11104 A front panel for 33 Gbps input configurations

SHF 11104 A front panel for 60/64 Gbps input configurations

SHF 11104 A front panel for mixed configurations

All dimensions are specified in millimeters (mm).