

# Data Sheet

## SHF 11106 A



## Error Analyzer



## Description

The SHF 11106 A is a multi-channel 64 GBaud Error Analyzer (EA). It analyzes binary (NRZ) or PAM4 digital bit sequences such as pseudo-random bit sequences (PRBS) or user defined bit patterns.

The instrument supports bit rates from 6 to 64 Gbps NRZ and baud rates from 6 to 64 GBaud (12 to 128 Gbps) PAM4 with continuous, gap-free operation. Depending on the configuration, the instrument features up to four independent 64 Gbps differential channels.

The operating bit rate is set by the clock signal from an external clock source. The inputs can operate at either full clock or half clock, for example, either a 64 GHz or a 32 GHz clock signal can be used for 64 Gbps operation.

The SHF 11106 A can be remotely controlled via an Ethernet interface using the SHF Control Center software provided by SHF or by custom software.

When a demultiplexer (DEMUX) extender head is attached, 120 Gbps NRZ signals can be connected as close as possible to the DUT.

## Features

- One to four data input channels
  - 64 Gbps NRZ (120 Gbps with remote head)
  - 64 GBaud (128 Gbps) PAM4
- Broadband operation up to an aggregated bit rate of 256 Gbps NRZ / 256 GBaud (512 Gbps) PAM4
- Nine built-in PRBS patterns ( $2^7-1$ ,  $2^9-1$ ,  $2^{10}-1$ ,  $2^{11}-1$ ,  $2^{13}-1$ ,  $2^{15}-1$ ,  $2^{20}-1$ ,  $2^{23}-1$  &  $2^{31}$ )
- Up to 16 Gbit user-defined pattern memory per channel
- Automatic search for the optimum sampling point for each channel
- All inputs can be used in single ended or differential mode
- Q-factor analysis for each channel
- Jitter analysis for each channel
- Eye contour analysis for each channel
- PAM4 analysis capability for PRBS patterns and user patterns like PRBS13Q and SSPRQ
- Control via intuitive graphical user interface SHF Control Center (SCC)
- Remote control via plain text TCP commands



## Applications

The SHF 11106 A is the ideal error analyzer or error detector for many R&D or production applications that require high speed test data streams for electrical/optical components or transmission systems. The flexible channel configurations, the wide gap-free data rate coverage and the advanced features make this Error Analyzer the perfect fit for

- single channel applications,  
*e.g., Fiber Channel®, PCI Express, Serial ATA*
- multi-channel applications,  
*e.g., 100GbE (using 4x32G DP-QPSK)*
- multi-level multi-channel applications using PAM4 mode  
*e.g., for 400GbE, 800GbE & 1.6TbE DWDM (e.g., using DP-16QAM or PAM4)*

## Configurations

The SHF 11106 A can be equipped in a variety of different configurations.

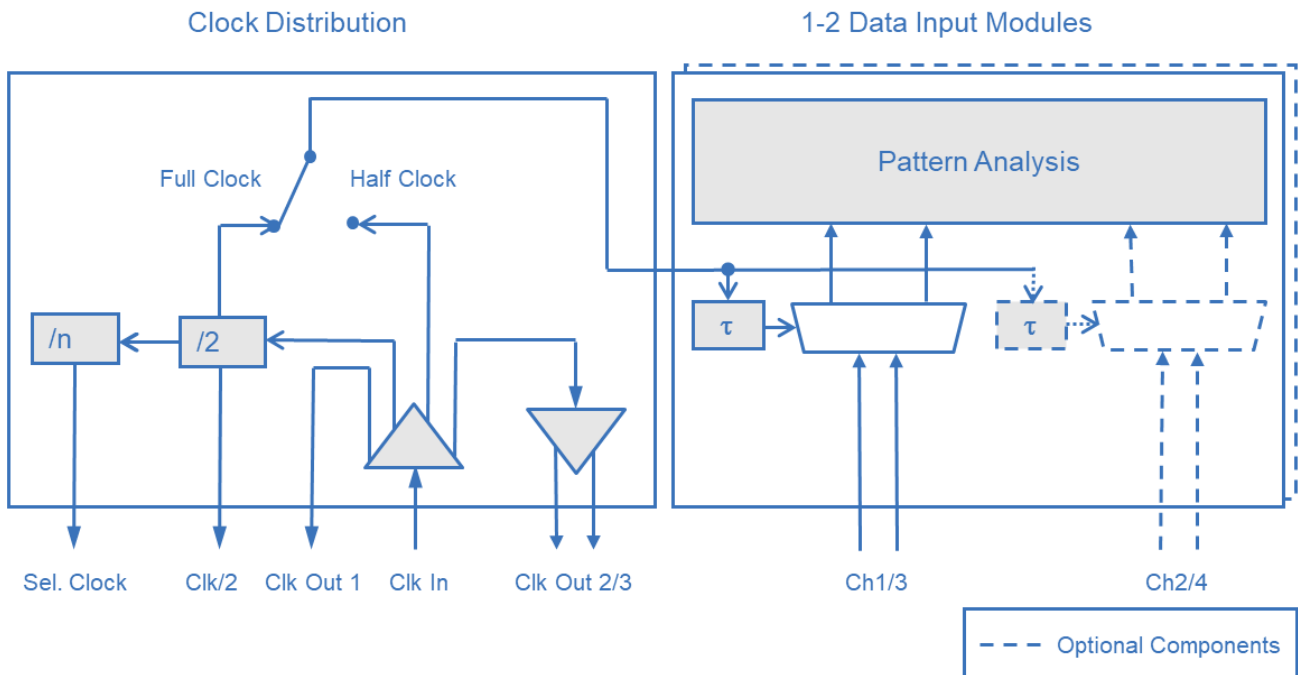
Single 64	– One differential input from 6 to 64 GBaud
Dual 64	– Two differential inputs from 6 to 64 GBaud
Triple 64	– Three differential inputs from 6 to 64 GBaud
Quad 64	– Four differential inputs from 6 to 64 GBaud

## Options

### Option Extender SHF 11221 A

One 120 Gbps data stream can be de-multiplexed externally by the SHF 11221 A before being applied to two 60 Gbps input channels. For details, please refer to the data sheet of the SHF 11221 A.

## Block Diagram



**Figure 1 - Block diagram of the SHF 11106 A**

The Error Analyzer internally consists of up to eight 32 Gbps pattern analysis blocks. The inputs of the Error Analyzer are 1:2 demultiplexed to generate two 32 Gbps data input streams. Each data input module includes two data input channels consisting of a delay line for delay control and a 1:2 DEMUX.

The clock distribution section processes the incoming clock signal to generate the clock out, clock/2 out, and selectable clock out signals. Full clock operation is enabled by selecting the full clock mode in the software, which divides the incoming clock signal by two.



## Specifications

### Absolute Maximum Ratings

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on RF Clock Input Port	V	$V_{DCin}$	-10		+10	AC coupled input <sup>1</sup>
External DC Voltage on RF Clock Output Ports	V	$V_{DCin}$	-10		+10	AC coupled outputs <sup>1</sup>
External DC Voltage on RF Data Input Ports	V	$V_{DCin}$	-10		+10	AC coupled inputs <sup>1</sup>

### Clock Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input						Connector Type: 1.85 mm (V) female connector 1.85 mm (V) female connector 2.92 mm (K) female connector 2.92 mm (K) female connector
Clock Output 1-3	$\Omega$			50		
Clock/2 Output						
Selectable Clock Output						
Minimum Clock Input Frequency		GHz	$f_{in\_clock\_min}$			
Maximum Clock Input Frequency	GHz	$f_{in\_clock\_max}$	32 64			half clock mode <sup>2</sup> full clock mode <sup>2</sup>
Clock Input Voltage	mV <sub>pp</sub>	$V_{in\_clock}$	630		900	AC coupled
Output Voltage Clock Output 1-3 Clock/2 Output Selectable Clock Output	mV <sub>pp</sub>	$V_{out\_clock}$	630 500 300	800 650 500	1000 900 700	AC coupled, @ P <sub>in</sub> =0 dBm AC coupled AC coupled
Output Frequency Clock Output 1-3 Clock/2 Output Selectable Clock Output	GHz GHz GHz	$f_{out\_clock}$	3 1.5 0.023		64 32 32	same as input frequency half of input frequency input frequency/N (N= 2, 4, 8, 16, 32, 64, 128)

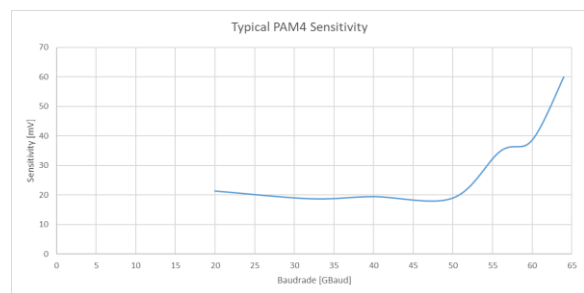
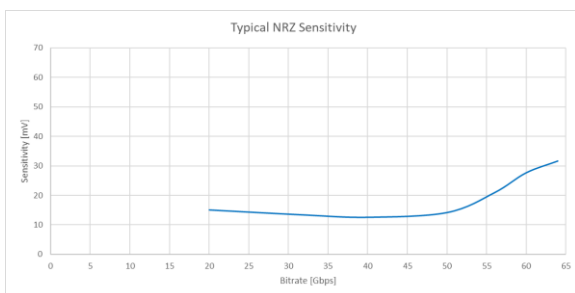
<sup>1</sup> If external bias voltages must be applied, the instructions in the application note 'DC Biasing Setups with Pattern Generators' must be followed

<sup>2</sup> The operating bit rate is determined by a clock signal from an external clock source which is not part of the Error Analyzer. The inputs can operate at both full clock and half clock, so e.g., a 20 GHz or a 40 GHz signal is required for 40 Gbps operation.



### Data Input Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Minimum Bit Rate	Gbps			2	6	
Maximum Bit Rate	Gbps		64	65		
Minimum Baud Rate for PAM4 Measurements	GBaud Gbps			2 4	6 12	
Maximum Baud Rate for PAM4 Measurements	GBaud Gbps		64 128			
Threshold Adjustment	mV	V <sub>threshold</sub>	-450		+450	Adjustable in 0.1 mV steps
Sensitivity <sup>3</sup>	mV	V <sub>sens_in</sub>		15 35	25 40 50	< 50 Gbps 50 to 60 Gbps > 60 Gbps
PAM4 Sensitivity <sup>4</sup>	mV			20	35 60 90	< 50 GBaud 50 to 60 GBaud > 60 GBaud
Delay Clock Phase Adjustment	ps		-35		+35	Adjustable in 0.1 ps steps
Clock Phase Margin <sup>5</sup>	°	CPM		tbd		
Maximum Input Amplitude	mV <sub>pp</sub>	V <sub>amp_in</sub>			900	
Maximum Input DC Voltage	V	V <sub>in_DC</sub>	-10		+10	
Connector Type	Ω			50		1.85 mm (V); female connector



<sup>3</sup> Value corresponds to the measured eye height on an Agilent 86100 C with 70 GHz samplers using 2<sup>31</sup>-1 PRBS at a BER limit of 10<sup>-9</sup>

<sup>4</sup> Value corresponds to the measured eye heights of a symmetric PAM4 signal on an Agilent 86100 C with 70 GHz samplers using 2<sup>23</sup>-1 PRBS at a BER limit of 10<sup>-9</sup>.

<sup>5</sup> BER limit 10<sup>-9</sup>, PRBS 2<sup>31</sup>-1, eye height 100 mV, Peak-to-Peak-Source-Jitter as displayed on an Agilent 86100 C with 70 GHz sampling heads and precision time base, calculated using the formula:

$$\text{Clock Phase Margin [}^\circ\text{]} = 360^\circ \cdot \frac{\text{Measured Clock Margin [ps]} - (\text{Peak-to-Peak-Source-Jitter [ps]})}{\text{Eye Length [ps]}}$$



### General Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Weight	kg	m			12	Fully Equipped
Dimensions	mm	WxDxH				340x480x146
Operating Temperature	°C	T <sub>OP</sub>	10		35	
Storage Temperature	°C	T <sub>ST</sub>	-20		70	@ 95 % RH max.
Working Humidity	%		20		90	Non condensing

### Rear Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Power Supply	V	U		48		48 V switching power supply is included
Power Consumption	W	P			120	Max. Configuration @48 V
Power Supply Connector						4 Pin Power DIN
Common Ground Connector						4 mm socket
Network Connectors						RJ-45 Ethernet
USB Connectors						For future use

### Front Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Auxiliary Power Output	V	U		-5 +5 +12		Max. 1.5 A Max. 1.5 A Max. 1.5 A
Auxiliary Power Connector						Lemo EPG.OB.304.HLN
Common Ground Connector						4 mm socket
Network Connector						RJ-45 Ethernet
USB Connectors						For future use



## Patterns

Pattern	Polynomial	Reference
PRBS $2^7-1$	$G(x) = 1 + x^6 + x^7$	
PRBS $2^9-1$	$G(x) = 1 + x^5 + x^9$	ITU-T O.150 5.1 IEEE 802.3 68.6.1
PRBS $2^{10}-1$	$G(x) = 1 + x^7 + x^{10}$	
PRBS $2^{11}-1$	$G(x) = 1 + x^9 + x^{11}$	ITU-T O.150 5.2
PRBS $2^{13}-1$	$G(x) = 1 + x + x^2 + x^{12} + x^{13}$	IEEE 802.3 94.3.10.8
PRBS $2^{15}-1$	$G(x) = 1 + x^{14} + x^{15}$	ITU-T O.150 5.3
PRBS $2^{20}-1$	$G(x) = 1 + x^3 + x^{20}$	
PRBS $2^{23}-1$	$G(x) = 1 + x^{18} + x^{23}$	ITU-T O.150 5.6
PRBS $2^{31}-1$	$G(x) = 1 + x^{28} + x^{31}$	ITU-T O.150 5.8 IEEE 802.3 49.2.8

## User Pattern Capabilities

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
User Pattern Memory size		Gbit			16	Per channel
User Pattern Granularity		Bit		256		For more details see Chapter User Pattern Capabilities



## Input Adjustment Capabilities

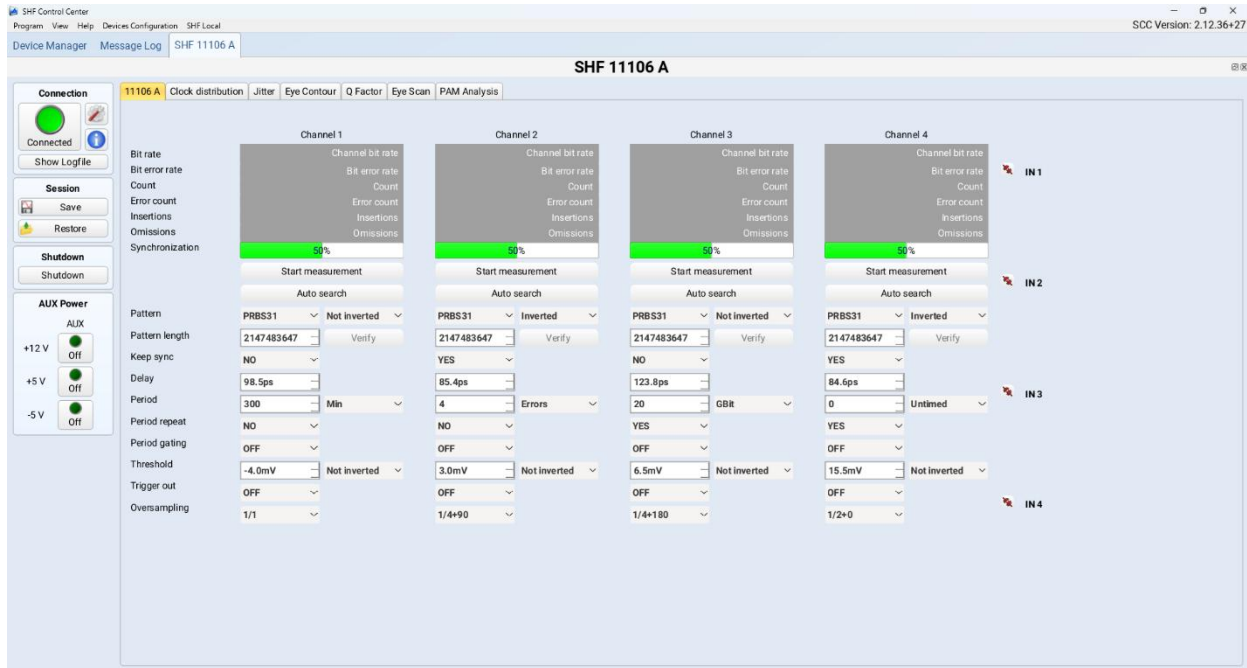


Figure 2 - SHF Control Center window for the SHF 11106 A

### Measurement Results

Bit Error Rate, Bit Count, Error Count (Insertions, Omissions, and Total) are displayed for detailed error diagnostics.

### Pattern Types

Pre-defined PRBS patterns from  $2^7-1$ ,  $2^9-1$ ,  $2^{10}-1$ ,  $2^{11}-1$ ,  $2^{13}-1$ ,  $2^{15}-1$ ,  $2^{20}-1$ ,  $2^{23}-1$ , and  $2^{31}-1$  are available. To analyze an arbitrary bit stream, 16 GBits of incoming data can be captured for comparison with subsequent data in real-time user pattern mode.

### Decision Point

Phase and data threshold can be set to optimize the decision point. An integrated auto-search routine will optimize phase and data threshold automatically and detect the incoming PRBS sequence.

### Measurement Period

The measurement period can be set in time, bits, or number of errors to be detected. Single, repeated, and untimed measurements are possible.

### AUX Power

Auxiliary power outputs are available to power external devices such as amplifiers or extension heads.



## User Pattern Capabilities

In addition to the pre-defined PRBS patterns, arbitrary user-defined patterns can also be analyzed.

The user pattern is analyzed in 'real-time mode'. This means, that the user does not need to load an externally created pattern into the Error Analyzer. The user only needs to define the length of the pattern and the Error Analyzer will capture and store the first incoming bit stream of this length into its internal memory. Subsequent incoming data is compared to the data stored in the internal memory. This enables continuous bit stream measurement without gaps<sup>6,7</sup>.

### Granularity Requirement

The maximum available user pattern length is 17,179,869,184 bits (2 Gigabyte; approx. 16 Gbit) per channel. Due to the internal architecture of the Error Analyzer the user pattern lengths must be a multiple of 256 bits.

If this granularity requirement is not met, the Error Analyzer will automatically record the pattern as often as required until the condition is satisfied. For example, if a 127-bit long data stream is to be analyzed, the length of the **actually recorded pattern** is  $127 * 256 = 32512$  bits.

For significantly longer patterns (patterns longer than 17,179,869,184 bits) it can happen that the **actually recorded pattern length** exceeds the memory size, although the actual size of the user pattern is smaller than the available memory. The available user pattern memory is shown below.

Pattern length up to	Pattern length has to be a multiple of
64 Mbit	1
128 Mbit	2
256 Mbit	4
512 Mbit	8
1 Mbit	16
2 Gbit	32
4 Gbit	64
8 Gbit	128
16 Gbit	256

Two Error Analyzer input channels (1&3, 2&4) share a common memory controller, consequently, their patterns must either be of the same length or be repeated until their least common multiple is reached.

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<sup>6</sup> The details are documented in the application note: *Real time user pattern BER analysis with the SHF 11104 A Error Analyzer*.

<sup>7</sup> The incoming data stream is internally de-multiplexed into sub-channels. Each individual sub channel requires an alternating pattern. As a consequence, a 1010 pattern cannot be measured, as the sub-channels would see a constant '1' or '0' and no alternating pattern.



### Error Counting with Real Time User Pattern

Ideally the recorded reference pattern used by the Error Analyzer should be error free. The conditions for error free reference patterns are described below.

The probability  $p$  to detect no errors within a bit stream of length  $n$  and a bit error ratio  $BER$  can be expressed by the following expression derived from the binomial distribution:

$$p = (1 - BER)^n$$

The following table lists the probability to receive an error free recorded pattern for different pattern lengths.

A PRBS  $2^7 - 1$  pattern requires  $127 * 256 = 32512$  Bits; a PRBS  $2^{23} - 1$  pattern  $8,388,607 * 256 = 2,147,483,392$  Bits. The probability to record and verify an error-free segment depends on the lengths of the **recorded pattern** and the actual BER.

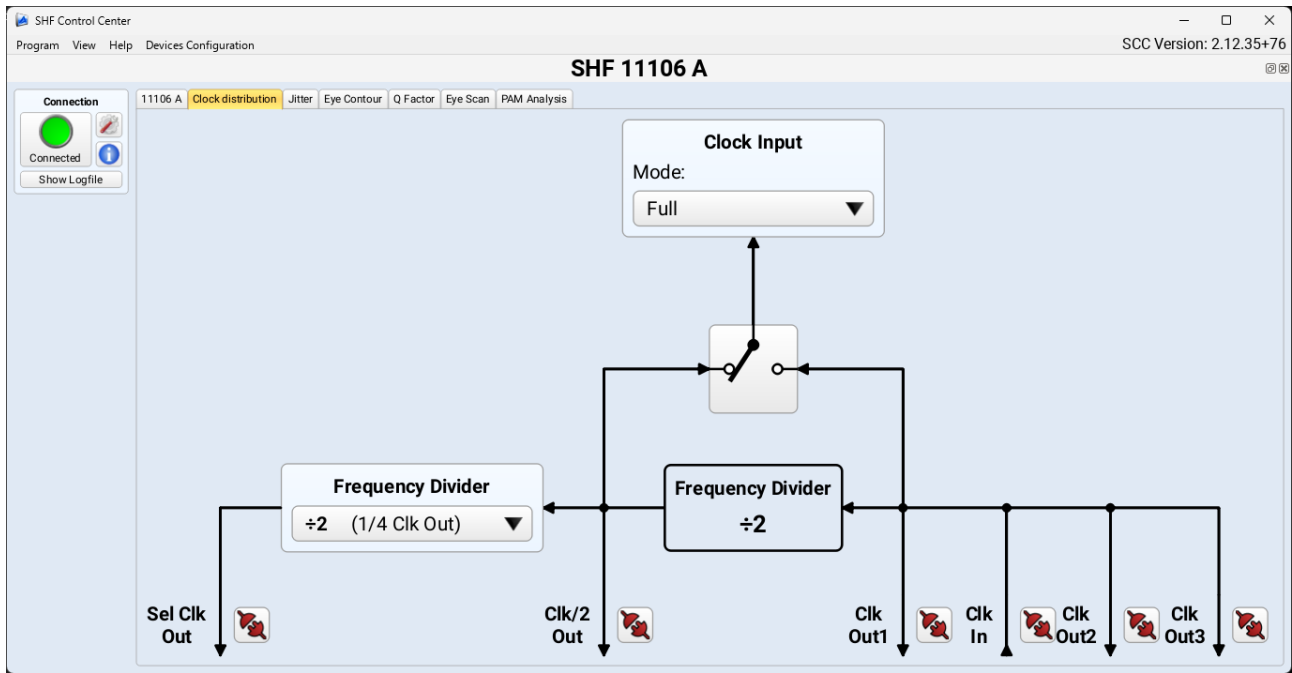
BER	Probability [%] to record error free pattern			
	Pattern length: 256 Bits	Pattern length: 32,512 Bits (PRBS7*256)	Pattern length: 8,388,352 Bits (PRBS15*256)	Pattern length: 2,147,483,392 Bits (PRBS23 * 256)
$10^{-4}$	97.472	3.872	0.000	0.000
$10^{-5}$	99.744	72.244	0.000	0.000
$10^{-6}$	99.974	96.801	0.023	0.000
$10^{-7}$	99.997	99.675	43.221	0.000
$10^{-8}$	100.000	99.967	91.954	0.000
$10^{-9}$	100.000	99.997	99.165	11.678
$10^{-10}$	100.000	100.000	99.916	80.674
$10^{-11}$	100.000	100.000	99.992	97.875
$10^{-12}$	100.000	100.000	99.999	99.785

Error-free recorded user patterns cannot always be guaranteed. For such cases a statistical interpretation of the measurement data is possible<sup>8</sup>.

<sup>8</sup> The details are documented in the application note: *Real time user pattern BER analysis with the SHF 11104 A Error Analyzer.*



## Clock Setup



### Clock Input

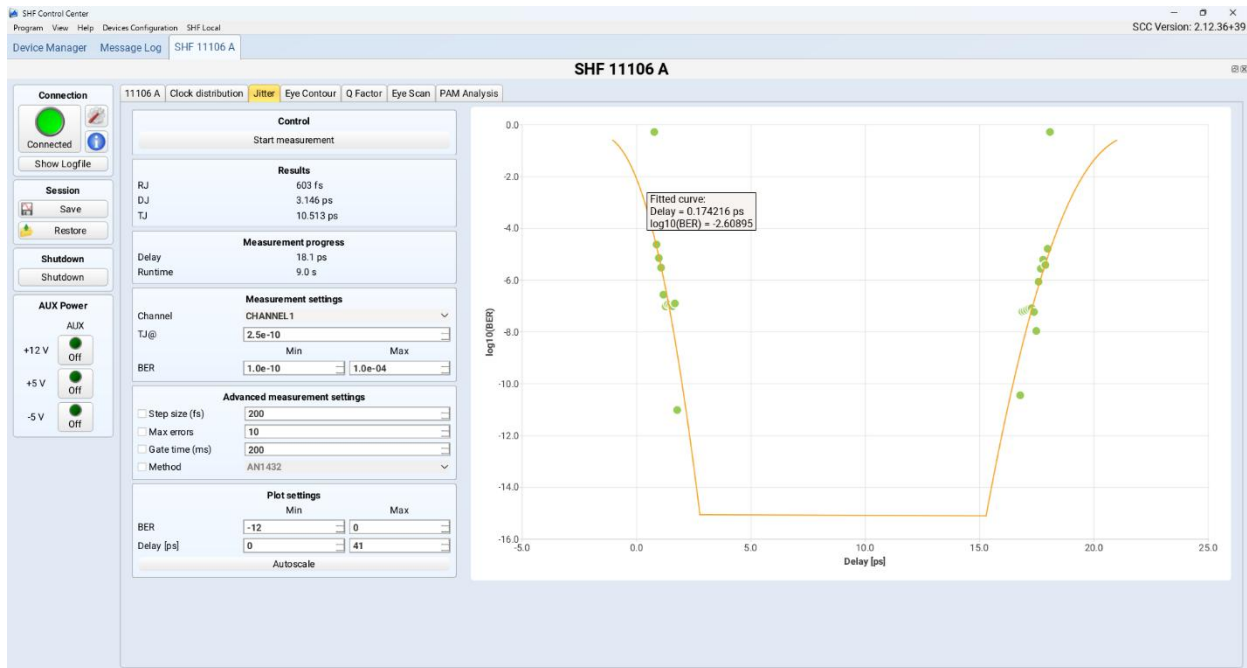
In full clock mode, the Error Analyzer requires a 64 GHz clock signal to analyze a 64 Gbps data signal. In half clock mode, a 32 GHz clock signal is required to analyze a 64 Gbps data signal. Internally the SHF 11106 A operates in half clock mode. When full clock mode is selected, an internal divider generates the half clock required internally from the externally provided full clock signal.

### Frequency Divider / Selectable Clock

The selectable clock output provides a divided clock signal derived from the clock input. A divider ratio of  $1/n$  with  $n = 2, 4, 8, 16, 32, 64,$  or  $128$  can be selected.



## Jitter Measurements



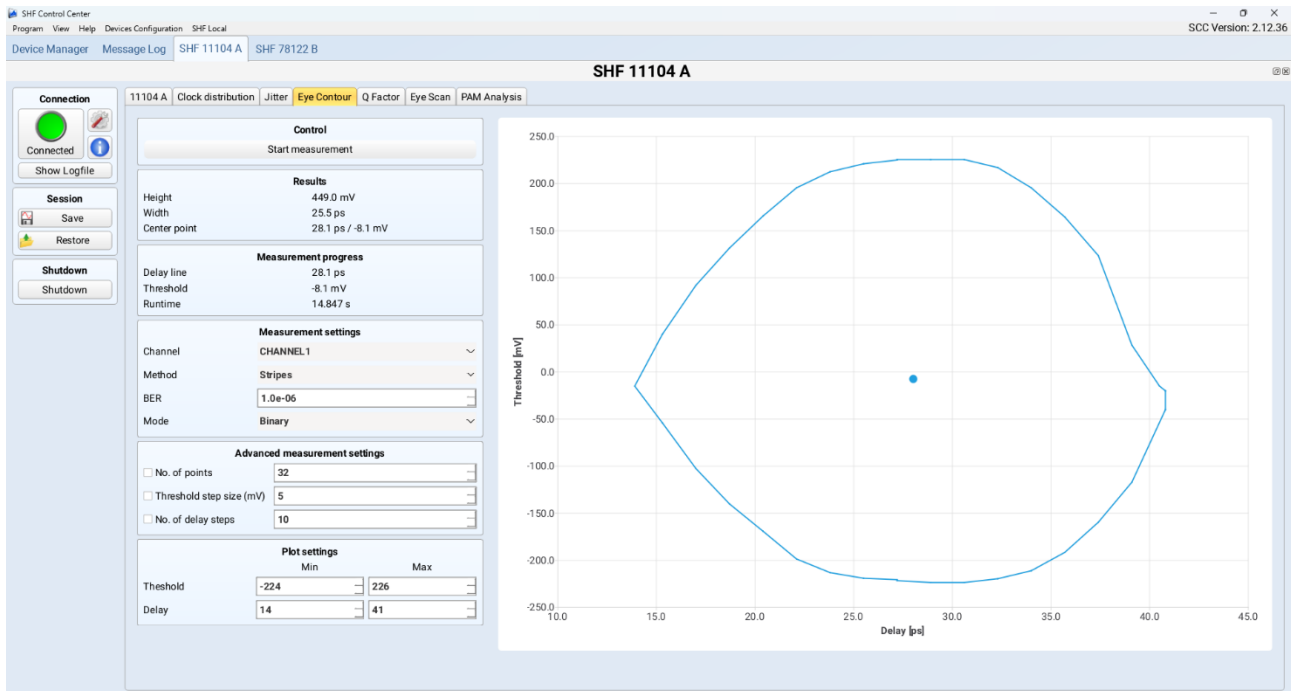
The SHF 11106 A has built-in jitter analysis functionality. It performs a BER scan and calculates random, deterministic, and total jitter components from the measurement results. The BER scan parameters can be adjusted. Two algorithms available for the jitter calculation.

The results of the BER scan and the jitter analysis can be exported for further analysis.

Further information about the jitter analysis and the theory underlying the jitter values can be found in the SHF application note “*Jitter Analysis using SHF 10000 Series BERT Equipment*” on the SHF web site ([www.shf-communication.com](http://www.shf-communication.com)).



## Eye Contour Scan

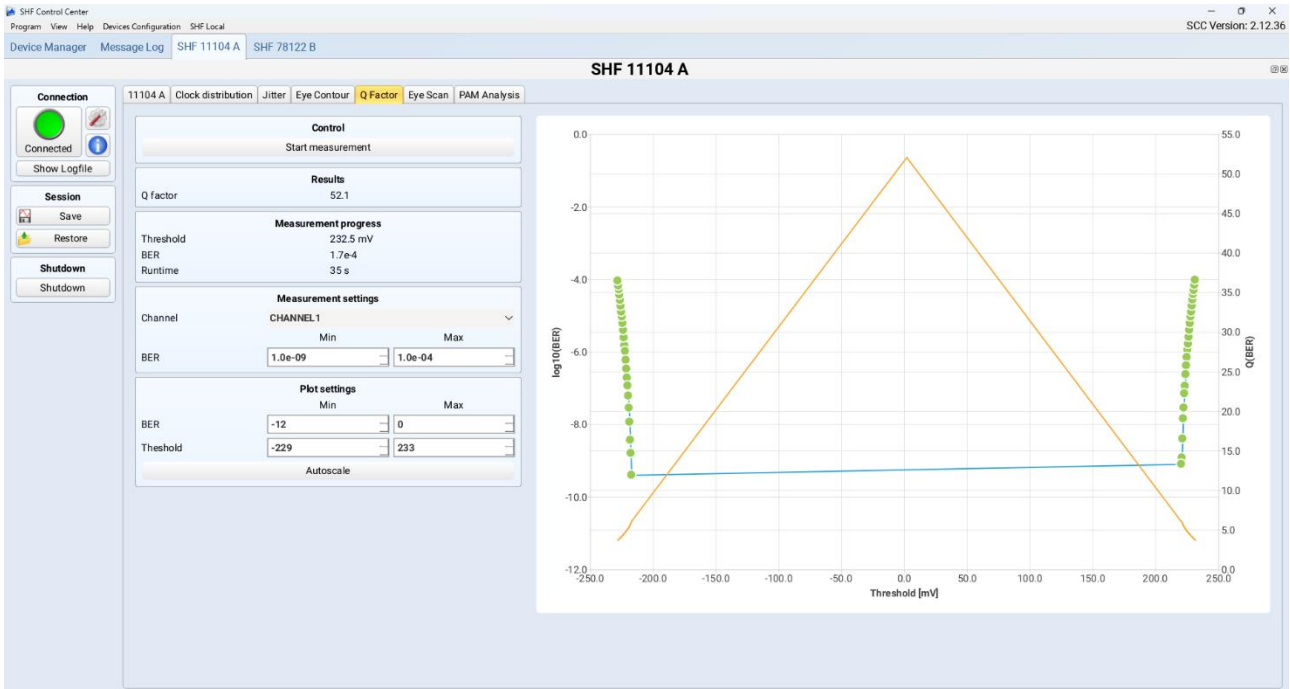


The SHF 11106 A has built-in eye contour scan functionality. It performs an eye scan along a user-specified BER threshold. The eye scan algorithm also determines the center of the detected eye which can be used as the decision point for subsequent BER measurements.

The results of the eye contour scan can be exported for further analysis.



## Q-Factor Measurement

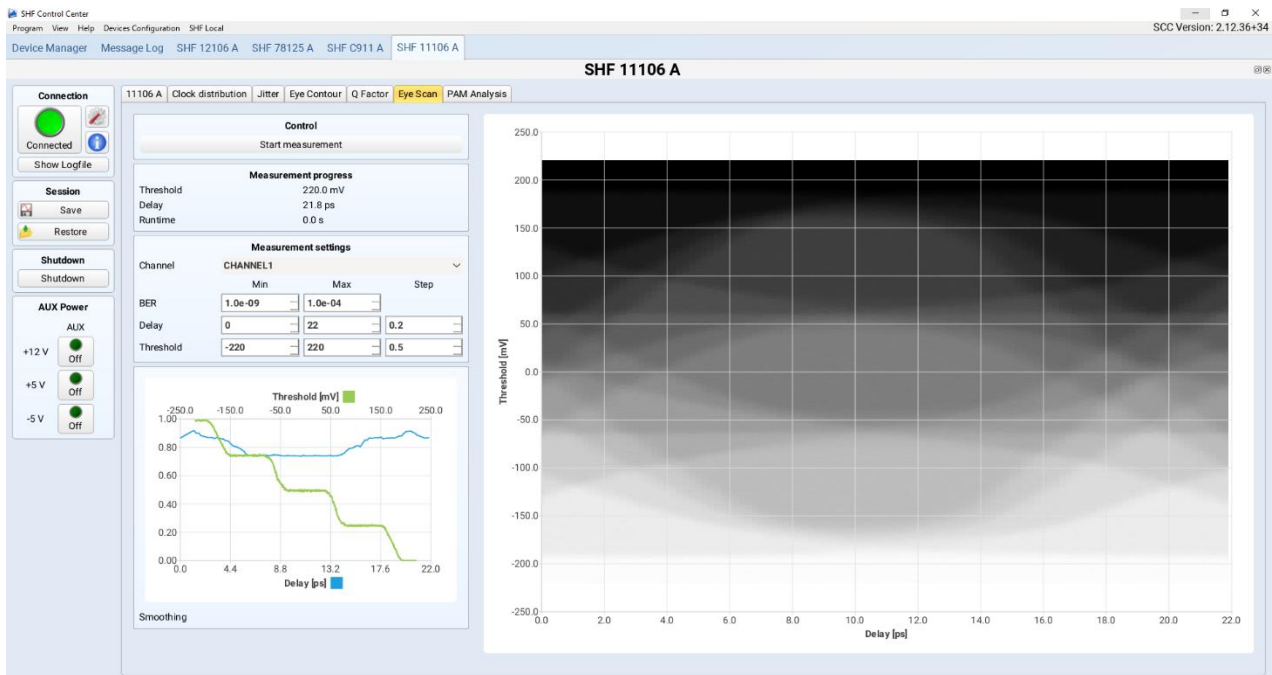


The SHF 11106 A has built-in Q-Factor analysis functionality. It performs a BER scan and calculates the Q-Factor from the measurement results. The BER scan parameters can be adjusted for further refinement.

The results of the BER scan and the Q-Factor analysis can be exported for further analysis.



## Eye Scan

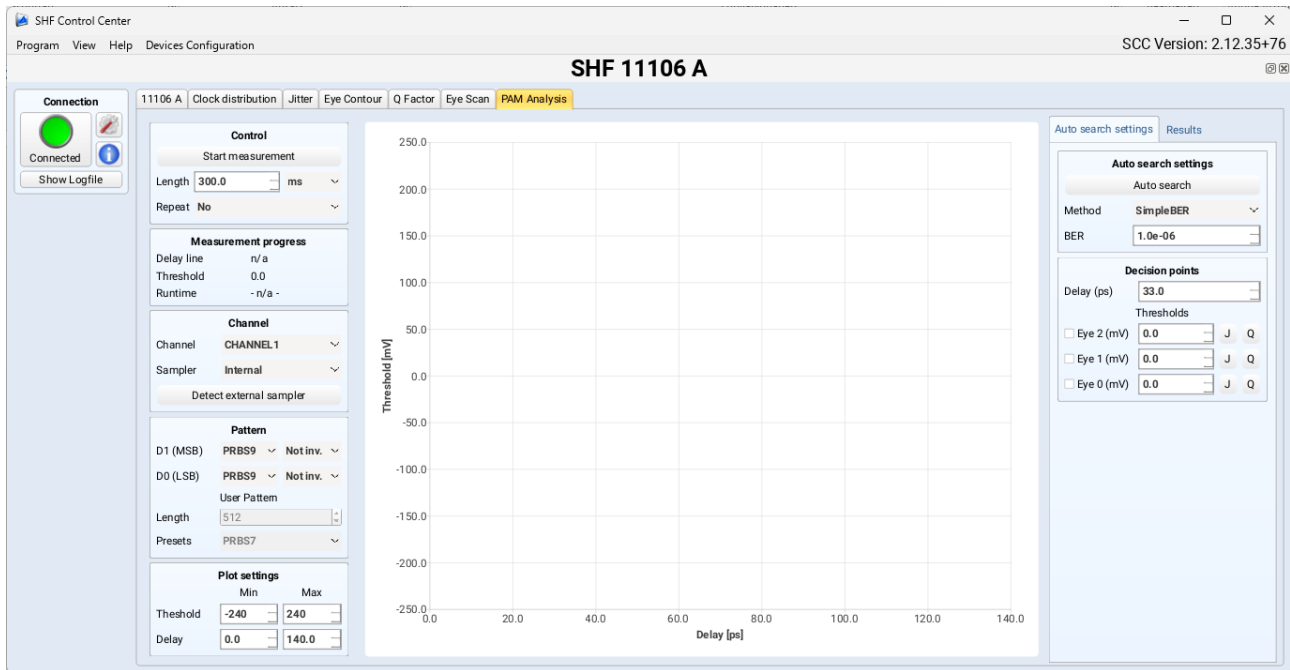


The SHF 11106 A has built-in Eye Scan functionality. It performs a scan over delay and threshold and displays an oscilloscope-like image based on the measurement results.

The results of the eye scan can be exported for further analysis.



## PAM4 Measurements



The Error Analyzer can be used to analyze PAM4 signals of up to 64 GBaud.

To perform BER measurements of the PAM4 signal, the Error Analyzer successively samples all eye openings of the 4-level eye and calculates the individual bit error rates. Two operation modes are available for error counting:

### Hardware Decoding (PRBS) Mode

For data streams generated from PRBS data without additional encoding the Error Analyzer includes an internal hardware decoder that the Error Analyzer synchronizes its internal reference generators with the two data streams encoded into the PAM4 signal. In this mode the Error Analyzer is able to detect data generated from a PRBS stream up to PRBS  $2^{31}-1$ .

### Real Time User Pattern Mode

For coded PAM4 signals such as QPRBS13 or non-PRBS patterns such as SSPRQ the Error Analyzer operates in real-time user pattern mode. Please refer to the chapter *User Pattern Capabilities* for further details on the pattern length and operating principles.

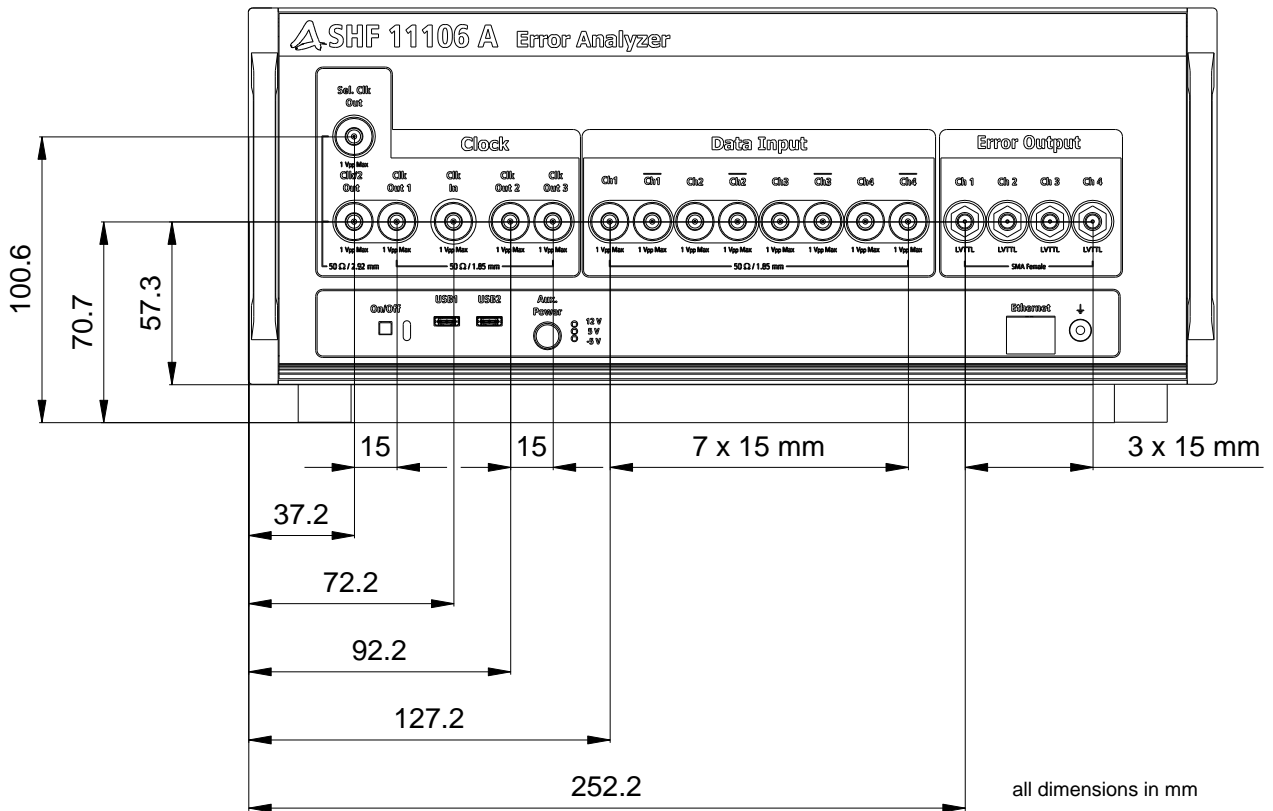
In all modes the Error Analyzer offers an auto-search algorithm determining the decision point for each eye of the 4-level signal. This auto-search algorithm can perform either a quick four-point search or a more detailed eye contour scan as shown in the screenshot below. Jitter measurements for each eye are supported, as are eye contour measurements.

For PAM4 signals the overall BER will be calculated according to the following formula:

$$BER_{Total} = \frac{1}{2}BER_{Eye2} + BER_{Eye1} + \frac{1}{2}BER_{Eye0}$$

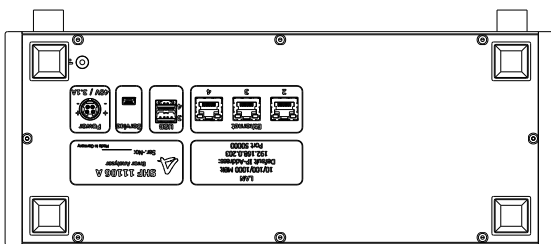
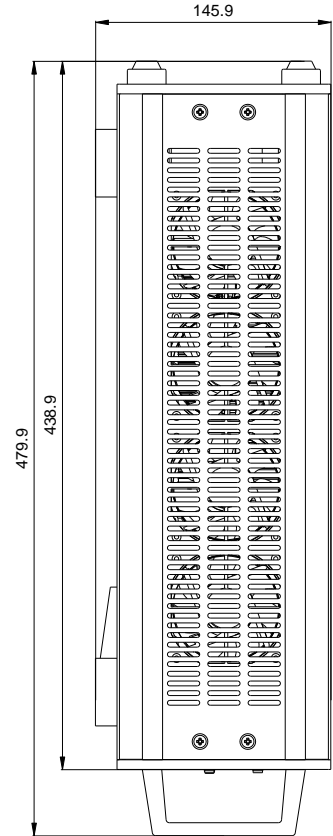
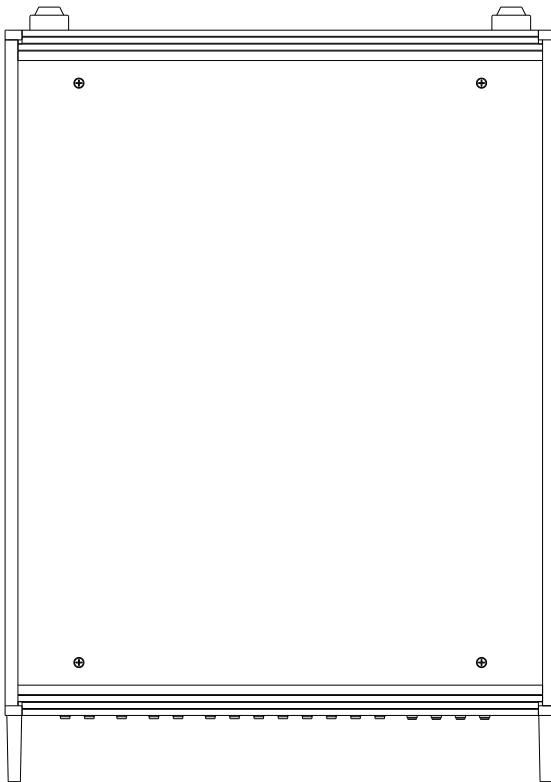
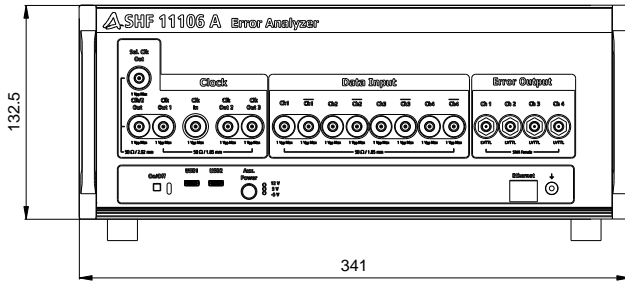


## Outline Drawing – Front Panel





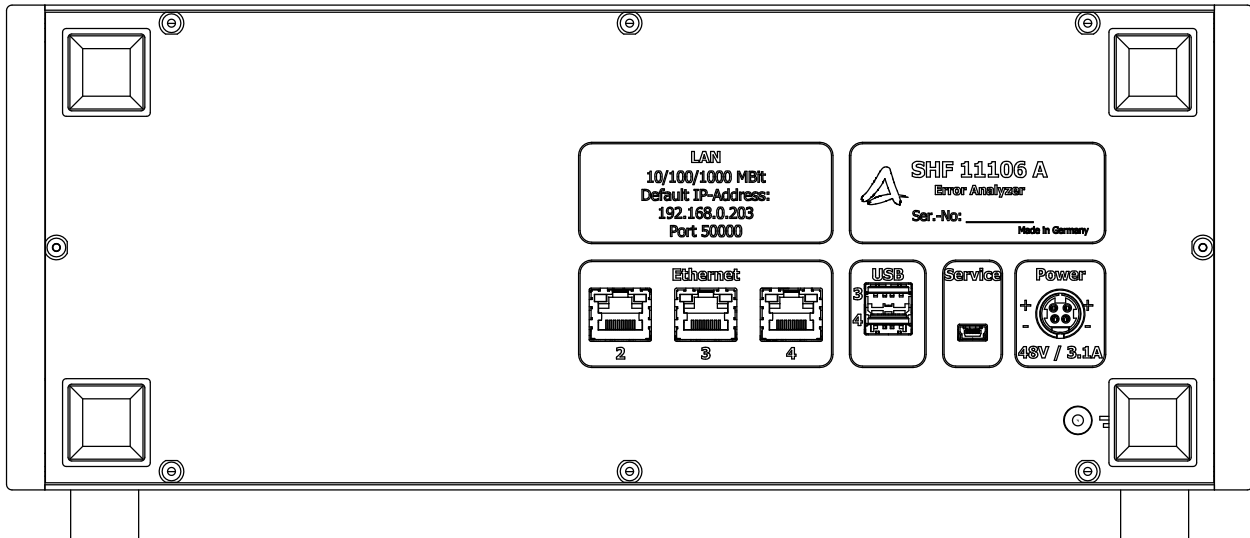
## Outline Drawing - Case



all dimensions in mm



## Outline Drawing – Back Panel





**SHF Communication Technologies AG**

Wilhelm-von-Siemens-Str. 23 D | 12277 Berlin | Germany

+49 30 772 051 0

[sales@shf-communication.com](mailto:sales@shf-communication.com)

[www.shf-communication.com](http://www.shf-communication.com)