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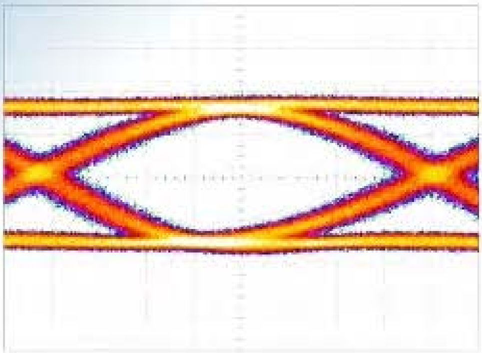

Application Note

AN-Burst-1

Fiber Loop Experiments with SHF BERT Systems

Introduction

Recirculating fiber loop experiments allow the simulation of transmission of an optical signal through thousands of kilometers of optical fiber to be performed in the laboratory. This application note describes a setup of such an experiment which can be used with SHF BERT systems.

Setup

A typical outline for recirculating loop experiments is shown in Figure 1. It consists of three stages: the data source, the transmission stage and the data receiver.

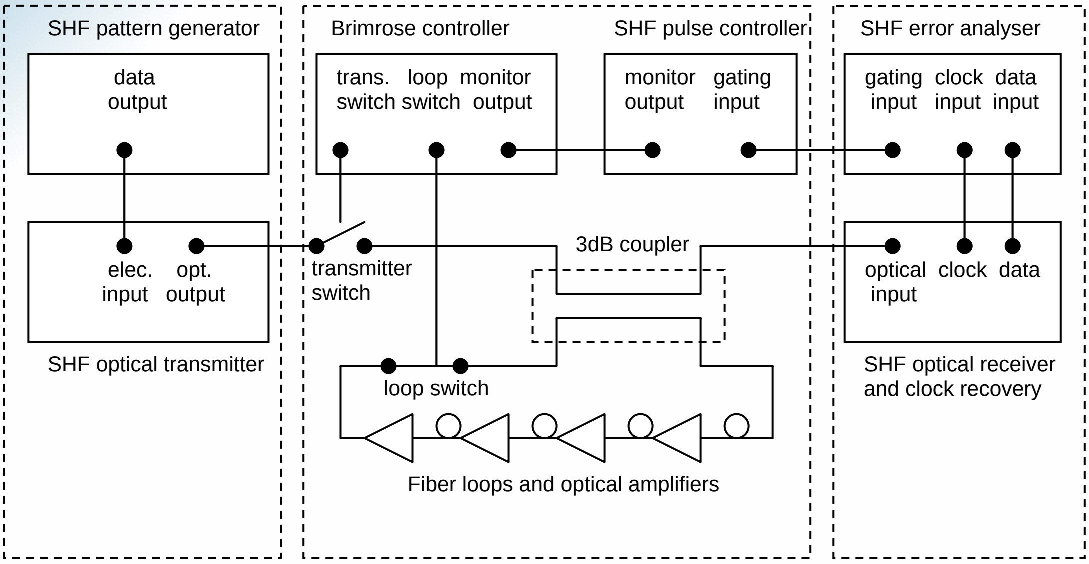

Figure 1: Setup for recirculating fiber loop experiments

Data source

The data source in this case contains a bit pattern generator and an electrical to optical converter. Most commonly, the data will be a PRBS pattern. User generated patterns can also be used if both the pattern generator and error analyzer support them. The format of the data is also determined in this stage. Possible data formats which can be transmitted using SHF products are NRZ, RZ, carrier suppressed (CS-) RZ, duobinary and DPSK.

Data transmission

The transmission stage is made up of the fiber loop with a controller to fill and empty the loop, a coupler to allow the signal in the loop to be monitored and a pulse controller to gate the error analyzer.

The Brimrose controller allows the loop to be filled with data. Initially, the transmitter switch is closed and the loop switch opened. Data from the data source runs into the loop; this takes about 500µs for a 100km loop. The transmitter switch is then opened and the loop switch closed so that the data recirculates around the loop. Since the time taken to complete one loop is known, the time taken to complete *x* loops can be calculated, and thereby the total distance traveled by the data. To ensure a low insertion loss, high speed and high extinction ratio, the switches are usually acousto-optic modulators.

To start to analyse the data after a certain time (and therefore distance), the error analyzer needs to know when to start operating. The SHF Burst Controller provides the signal to start. It has a connector marked "Monitor Out" which should be connected to the Monitor output of the Brimrose controller. When the Brimrose controller closes the loop switch and opens the transmitter switch, it sends a signal to the SHF Burst Controller. The Burst Controller then starts a timer, which is set by the user to a value between 0…999999µs. When it reaches its set time, it sends a signal to the gating input of the error analyser to start measuring. Figure 2 gives a graphical view of how the timing works.

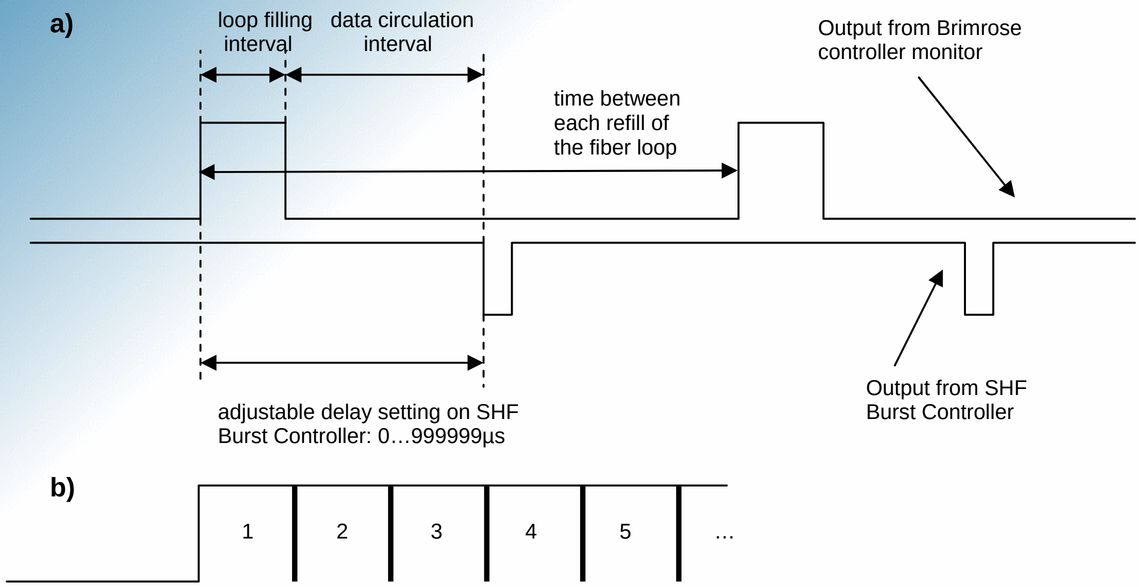

Figure 2

a) The SHF Burst Controller starts timing with the positive going pulse from the Brimrose controller. When the Burst Controller completes its time, it send a negative going pulse to the error analyzer to start the measurement.

b) The number of times that the data circulates through the loop. In this example, the error analyzer starts measuring at the start of cycle 4.

Data receiver and analysis

The receiver is a photodiode with an amplifier to boost the signal strength. A clock signal must be extracted from this signal to drive the error analyzer, so a clock recovery module is necessary. The signal and clock are then fed into the error analyzer which detects any errors which have appeared during transmission of the signal.

To make measurements in the fiber loop experiment, the Burst Gating Mode needs to be used on the instrument. In this mode, the following parameters need to be set:

Burst Length: this defines how long the instrument measures after receiving a signal from the SHF Burst Controller. This value should be equal to (or slightly less than) the length of one cycle in the recirculating loop.

Burst Cycle: This counts the number of cycles that are measured, e.g. the data circulates through the loop *x* times (as determined by the Burst Controller), and is then measured. After refilling, the next time the data has traveled *x* times through the loop, it is measured again. This repeats for the required number of cycles. The total *measurement* time is thereby Burst Length X Burst Cycle.

Burst Timeout: This is necessary to stop the analyzer from hanging if it fails to synchronise with the data signal. If it receives the instruction to start measuring (from the gating input) but cannot synchronise, it will wait forever to try to start measuring. This setting tells the analyzer to give up trying to synchronise after a certain time.

Note on clock recovery

To extract a clock signal from the data, a PLL based clock recovery unit must be used in conjunction with SHF error analysers. A simple filter-based clock recovery system is not suitable, as the data stream might not allow a suitable clock signal to be recovered to synchronise the analyser.

The SHF 11120 A can lose its synchronisation if the data signal disappears for longer than 8µs. It can then take up to 1.5ms to re-synchronise. Care should be taken to avoid gaps longer than 8µs between data cycles.