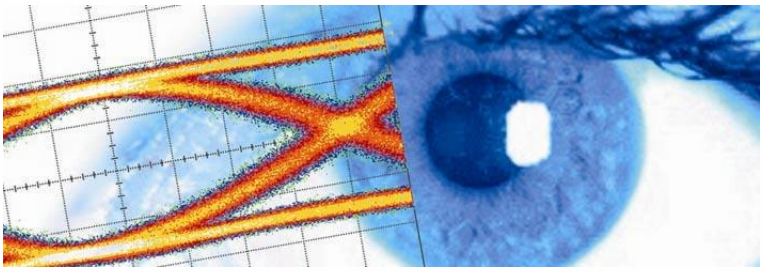
SHF Communication Technologies AG

Wilhelm-von-Siemens-Str. 23D • 12277 Berlin • Germany

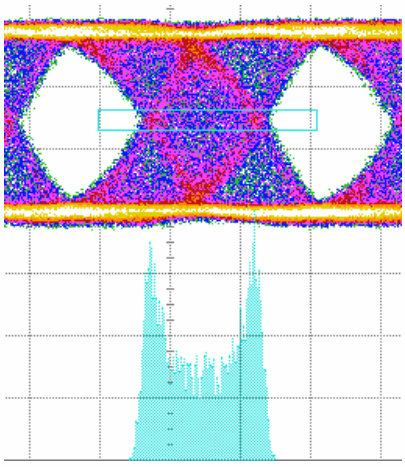
Phone +49 30 772051-0 • Fax ++49 30 7531078

E-Mail: sales@shf.de • Web: http://www.shf.de



Application Note

Jitter Injection using the Multi-Channel BPG SHF 12103/12104



Introduction

The characterization of jitter tolerance and jitter transfer on high-speed communication components is essential to ensure low bit error rate transmission and compliance with telecommunication industry standards. A jitter tolerance test specifies the limits of timing jitter a network device is required to tolerate without performance degradation. A typical test as detailed by several standards comprises the generation of a jittered data signal with a sinusoidal jitter component of a certain frequency and amplitude. Figure 1 shows four examples of jitter frequency masks as defined in the IEEE 802.3ba Ethernet standard for 40 and 100 Gbit/s, and the ITU-T G.8251 OUT-3 standard for 10 and 40 Gbit/s [1], [2]. The jittered data signal is applied to a device under test (DUT) to analyze if the performance is maintained under certain jitter stress limits given in the standard.

This application note presents the experimental setups that allow the injection of deterministic sinusoidal jitter with a pre-defined peak-to-peak jitter amplitude and jitter frequency using either the SHF 12103 A or the 12104 A bit pattern generator (BPG) and a minimal number of external components. The first sections of this note concentrate on sinusoidal jitter, whereas other jitter types are briefly covered in the last section. An overview of the various jitter types may be found in several textbooks on this topic, e.g. [3].

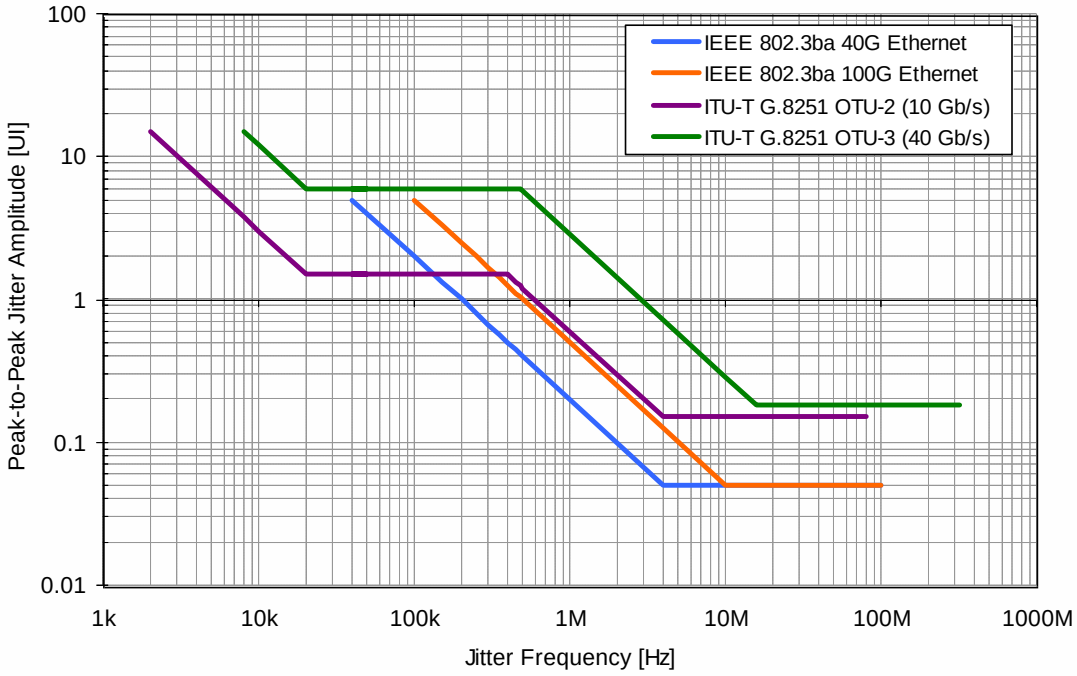


Figure 1: Sinusoidal jitter tolerance masks as defined in relevant communication industry standards [1], [2].

Principle of Jitter Generation

Deterministic sinusoidal jitter can be interpreted as a harmonic frequency modulation (FM) of the signal with a sine wave of a certain frequency and amplitude. The principle of jitter generation by frequency modulation is illustrated in Figure 2. An ideal clock signal as shown in Figure 2(a) is frequency modulated using the sine wave shown in Figure 2(b) which results in the jittered clock signal shown in Figure 2(c). The frequency and the amplitude of the FM input signal will determine the properties of the jittered clock. The jitter frequency f_{jitter} is set by the frequency of the FM input signal.

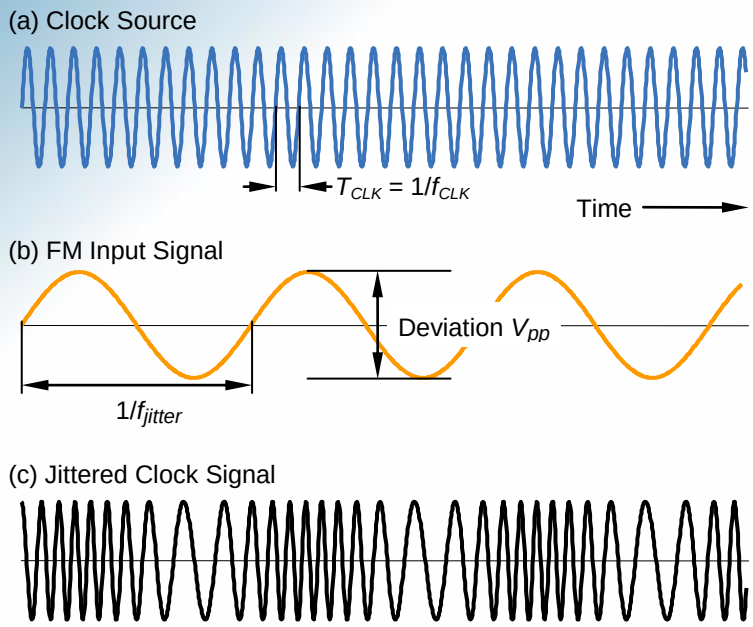


Figure 2: Generation of a jittered clock signal by sinusoidal frequency modulation.

The peak-to-peak jitter amplitude A_{pp} is commonly measured in unit intervals (UI) where 1 UI corresponds to the bit duration T_B of the data signal. Given a jitter amplitude value in seconds, A_{pp} is obtained in UI using

$$A_{pp} = \frac{\Delta T}{T_B} \tag{1}$$

where T_B is the inverse of the bit rate. For example, a peak-to-peak jitter amplitude of 0.5 UI is equivalent to 20 ps for a 25 Gbit/s data signal (T_B = 40 ps).

The jitter amplitude is controlled by the amplitude V_{pp} of the FM input signal. The FM frequency deviation ΔF is proportional to V_{pp} as shown in Figure 2.

Theoretically, the jittered clock signal c(t) of Figure 2(c) may be described by

$$c(t) = \hat{C} \sin\left[2\pi\, f_{CLK}\, t - \eta \cos\left(2\pi\, f_{jitter}\, t\right)\right], \tag{2}$$

where f_{CLK} is the clock frequency in Hz, η is the modulation index and f_{jitter} is the jitter frequency in Hz. The modulation index is related to the FM frequency deviation ΔF by

$$\eta = \frac{\Delta F}{f_{jitter}}. \tag{3}$$

The jitter peak-to-peak amplitude A_{pp} is related to the modulation index by

$$A_{pp} = \frac{\eta}{\pi}, \tag{4}$$

where A_{pp} is measured in UI.

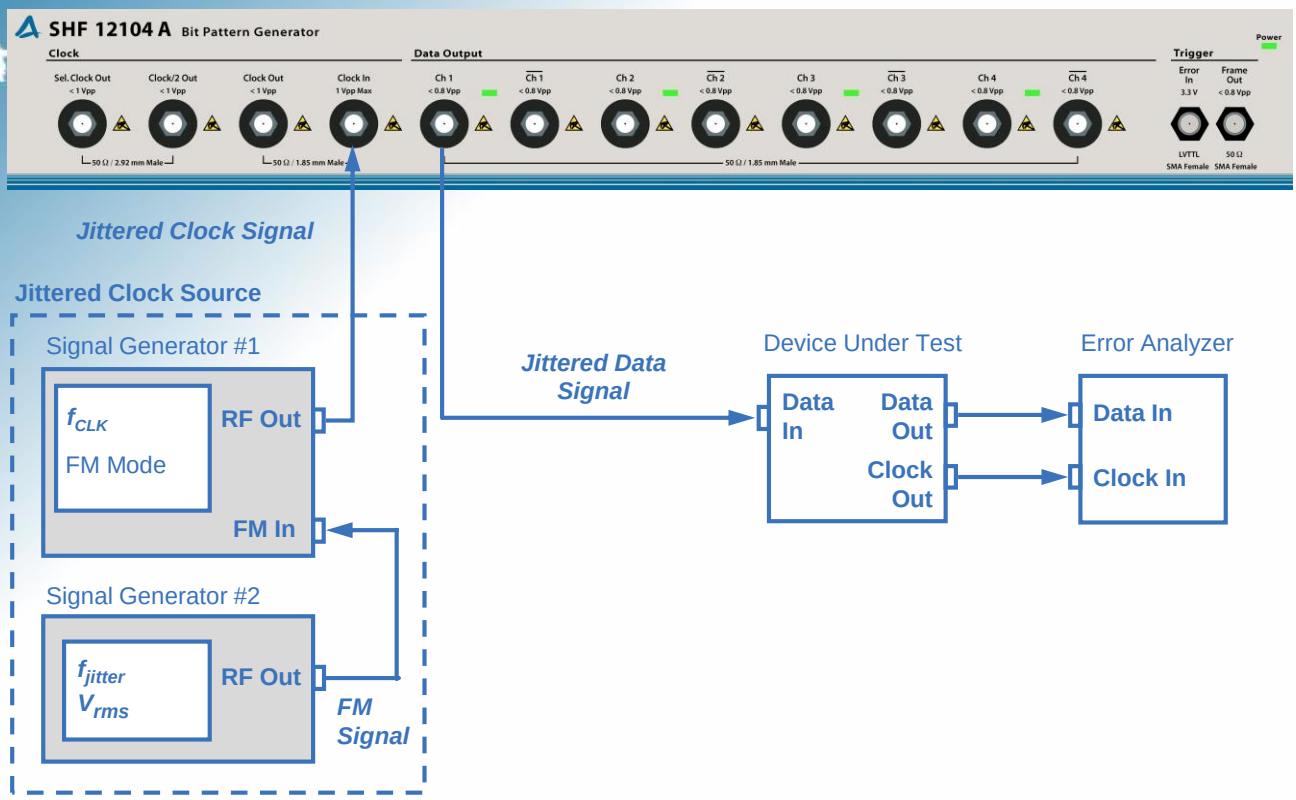


Figure 3: Jitter tolerance setup using the SHF 12104 A BPG.

Jitter Injection Measurement Setup

In practice, a jittered clock signal may be generated using a signal generator with an FM input. The setup is shown in Figure 3. Two signal generators are required to form a jittered clock source. The first generator produces a high-frequency clock signal at f_{CLK}, whereas the second may be a lower speed signal generator that modulates the frequency of the clock signal at f_{jitter}.

The jittered clock signal is connected to the clock input of the SHF 12103 A or 12104 A BPG. The clock jitter is transferred to all the data outputs of the BPG (as will be confirmed below). The jittered data signals may be applied to the DUT to determine the jitter tolerance. Depending on the specific jitter tolerance test requirement, the output of the DUT is evaluated using the adequate test equipment such as an error analyzer.

Using this setup, a jittered data signal with specified jitter frequency and amplitude may be generated by varying the signal frequency f_{jitter} and the amplitude level V_{rms} at signal generator #2. Practical limitations arise due to the finite modulation bandwidth and linearity. Therefore, the calibration and verification of the clock source are mandatory.

Calibration and Verification of the Injected Jitter

In order to create an accurate jitter signal for a specific task, the parameters of the setup presented in Figure 3 need to be calibrated and verified. We will describe how to determine the settings of generator #2 for the generation of jitter with a desired frequency and amplitude. Also, the limitations of this jitter generation technique are discussed. The accuracy and the characteristics of the jittered data signal may be verified using an oscilloscope in the time domain. Additional verification can be achieved by analyzing the spectrum of the jittered clock signal.

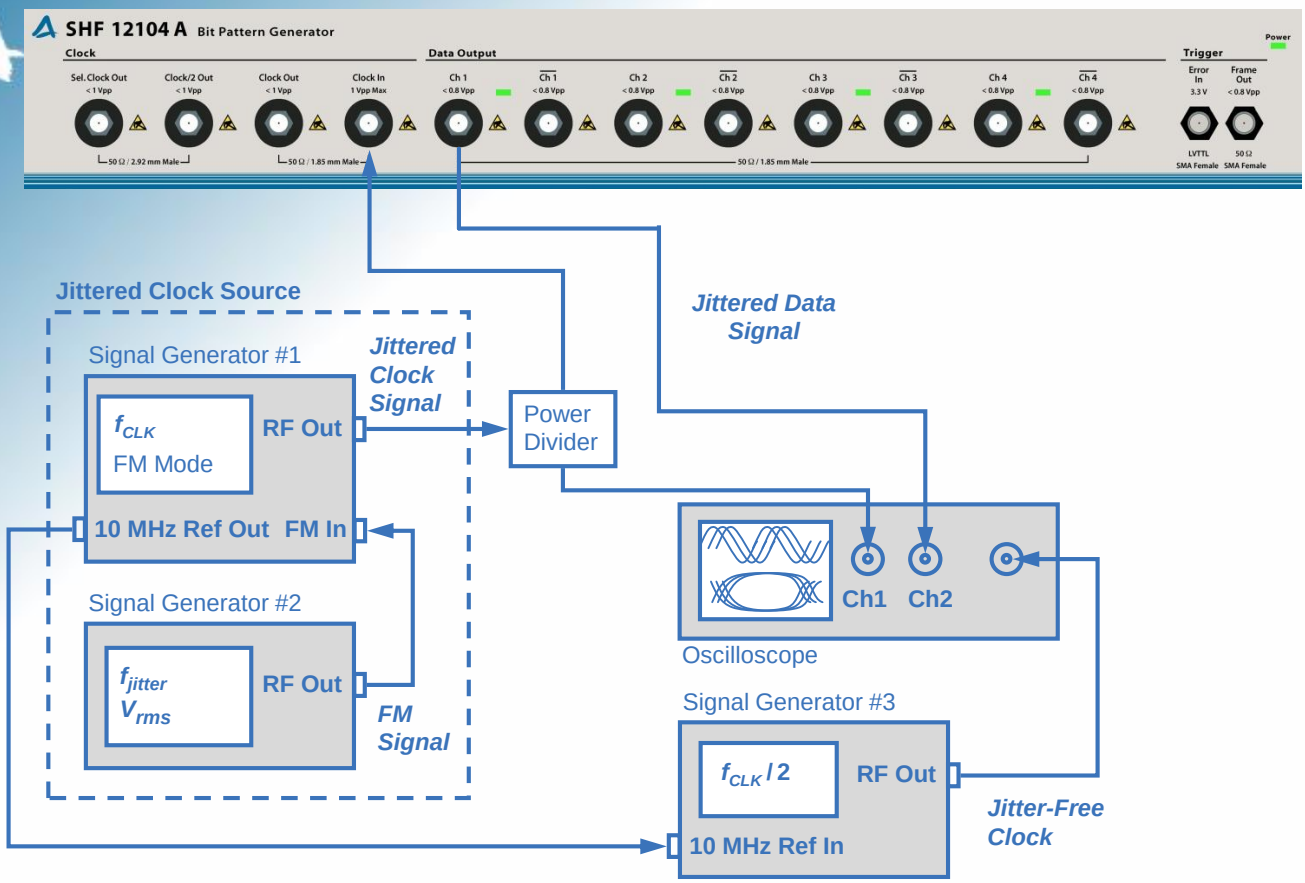


Figure 4: Jitter calibration and verification setup for the time-domain analysis of jittered signals.

Time-Domain Jitter Measurement

For the time-domain analysis of the jittered output waveform, a modified setup is used as shown in Figure 4. The procedure for setting up the jittered clock source depends on the signal generator models to be used. Here, an Anritsu 68197C is used as signal generator #1. The FM function of the 68197C is enabled using the following parameters:

- Mode: Locked Low Noise
- Impedance: 50 Ω
- Source: Front.
- Sensitivity: up to 20 MHz/V

The FM input signal is provided by the lower speed signal generator #2. Remember that, typically, the jitter frequency ranges from a few kHz to several hundreds of MHz. Here, a HAMEG HM8135 is used. The jitter frequency and amplitude are programmed on the HM8135 by varying the signal frequency and RMS level.

The jittered clock and data output signals are visualized and characterized on an Agilent 86100A sampling oscilloscope. In order to derive a jitter-free trigger signal, a third signal generator is synchronized to signal generator #1 using the 10 MHz reference port. The trigger signal is connected to the time base input of the sampling oscilloscope.

As an example, the setup was adjusted to generate sinusoidal jitter with an amplitude of A_{pp} = 0.47 UI and a frequency of f_{jitter} = 1 MHz at a clock frequency of f_{CLK} = 28 GHz and a bit rate of 28 Gbit/s. The jitter amplitude is verified using the time markers on the oscilloscope. The time difference ΔT is measured as the maximum deviation at a defined instant of the waveform. The jitter amplitude A_{pp} is calculated using Equation (1).

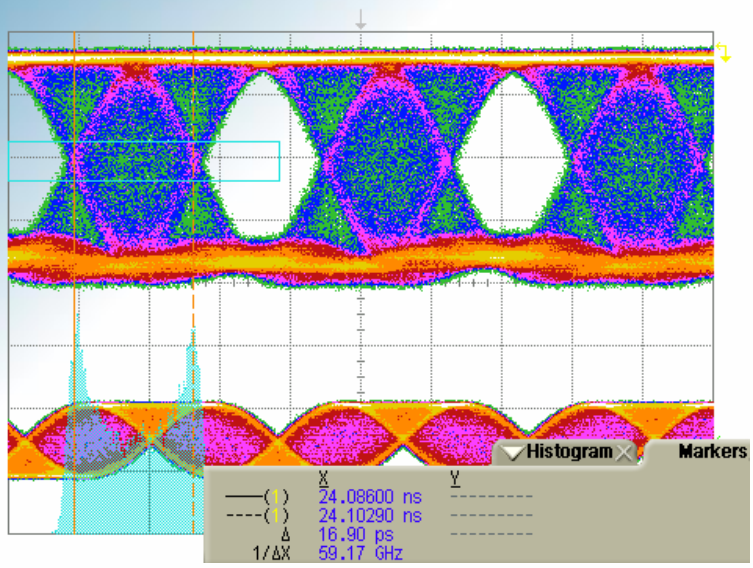


Figure 5: Jittered clock eye diagram with 0.47 UI jitter amplitude at 28 GHz clock frequency (bottom) and jittered PRBS data eye at 28 Gbit/s with the same amount of jitter transferred from the clock (top).

Figure 5 shows the eye diagrams of the jittered clock and data waveforms measured using the presented setup. The jitter on the clock is transferred to the jitter on the data signals. Clearly, a deterministic jitter of 16.9 ps is measured on the data signal which corresponds to 0.47 UI according to Equation (1). The shape of the histogram shown in Figure 5 is typical of sine-wave jitter [4].

Jitter Transfer from the Clock Signal to the BPG Data Output

Due to its clock distribution circuitry, the SHF 12103 A and SHF 12104 A pattern generators transfers the jitter correctly from the clock signal to the PRBS data signal over the relevant range of jitter frequencies and amplitudes. The setup shown in Figure 4 was used to measure the clock jitter amplitude $A_{pp,clk}$ and the data jitter amplitude $A_{pp,data}$ for seven different jitter frequencies (8 kHz, 100 kHz, 500 kHz, 1 MHz, 4 MHz, 10 MHz, and 16 MHz) at 28 Gbit/s using a 28 GHz clock. At each frequency, up to five jitter amplitude value pairs were measured. The results showed that the jitter properties (jitter type, frequency and amplitude) of the clock signal are transferred unaltered to the data output signal. It will be discussed below that for the presented lab setup the largest achievable jitter amplitude and frequency are limited by signal generator #1.

Frequency-Domain Jitter Measurement

The jitter amplitude measurement on the oscilloscope is limited to 2 UI since the signal or clock edges cannot be identified in the eye above 2 UI. For larger amplitudes, spectrum based techniques can be used. For the spectral analysis of the jittered clock, a setup according to Figure 6 is used. The jittered clock is connected to a spectrum analyzer for the analysis of the FM spectrum.

Jitter frequency and amplitude can be verified on the spectrum analyzer in the frequency domain using the so called Bessel “nulls” method which is detailed in [5]. An important property of the frequency-modulated clock signal spectrum is that the amplitude of the carrier becomes zero at defined jitter amplitudes. From FM theory it can be shown that a carrier zero occurs whenever the modulation index η is equal to the roots of the Bessel function J_0. The first four roots are at η = 2.40, 5.52, 8.65, 11.79. Note that the modulation index is related to the jitter amplitude by Equation (4). For example, at a jitter frequency of f_{jitter} = 1 MHz, the first carrier zero occurs at a jitter amplitude of A_{pp} = 2.4/π = 0.76 which is equivalent to ΔT = 27.3 ps at f_{CLK} = 28 GHz. Using the Bessel “nulls” method, specific values of A_{pp} can be measured very accurately.

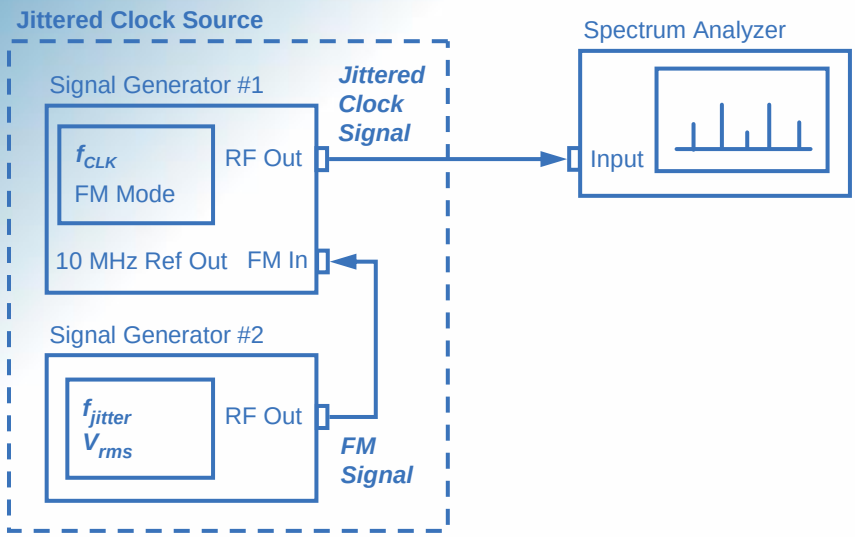
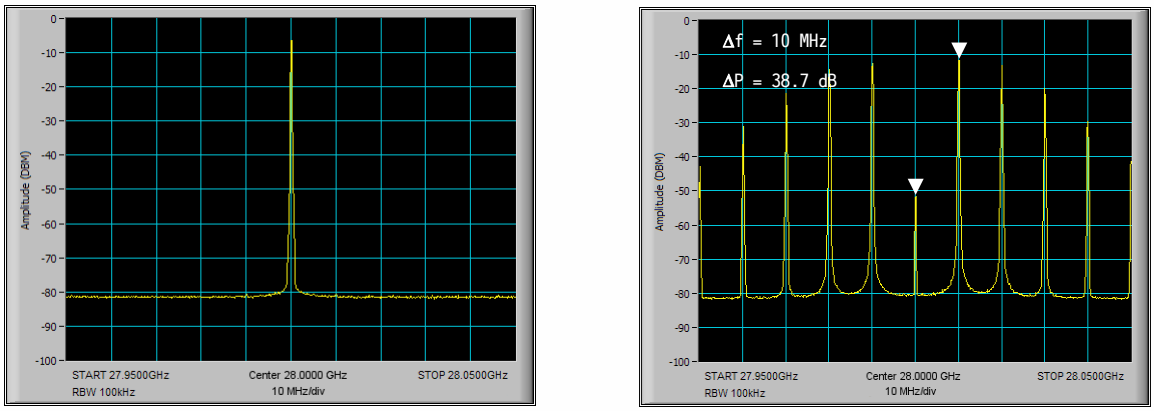
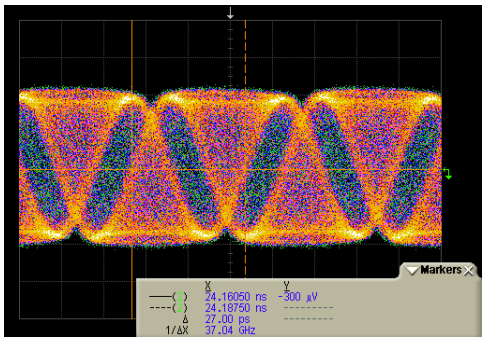


Figure 6: Jitter calibration and verification setup using a spectrum analyzer.

Figure 7(a) shows a measured spectrum of the clock signal without FM, i.e. the carrier spectral component is located at 28 GHz. Figure 7(b) illustrates the carrier zero in the spectrum of the FM modulated clock at a modulation index of η = 2.4. The spectrum shows a ratio of the carrier and the first sideband of $20\times\log(J_1/J_0) > 38$ dB which corresponds to less than 1% deviation error. Figure 7(c) displays a screen capture of the oscilloscope showing the corresponding eye diagram in the time domain. Clearly, a jitter amplitude of 27 ps is achieved which is equivalent to 0.76 UI.



(a) **(b)**



(c)

Figure 7: Spectra of (a) unmodulated 28 GHz clock and (b) FM modulated clock with 10 MHz jitter frequency showing the first carrier zero. (c) Corresponding clock eye diagram with 0.76 UI jitter amplitude (27 ps).

Characterization of the Jitter Generation Setup

At a fixed f_{jitter} and f_{CLK}, the voltage rms level V_{rms} on signal generator #2 determines the jitter amplitude. Inside generator #1, the FM input is usually applied to the voltage controlled oscillator. Practical limitations arise due to the finite modulation bandwidth and the limited linearity range between FM input amplitude V_{rms} and the actual modulation index of the output. Therefore, the relation between the FM input voltage amplitude and the jitter amplitude should be characterized experimentally for a given combination of signal generators.

The following steps describe a possible technique to characterize the jitter amplitude versus the FM input amplitude V_{rms} using the setups shown in Figure 4 and 6.

- Set the clock frequency of the signal generator #1 such that the specified bit rate is generated at the SHF 12103 A or SHF 12104 A.
- In order to derive a trigger signal, set the frequency of the signal generator #3 to an adequate value depending on the clock frequency and the trigger requirements. Typically, the trigger frequency is half or a quarter of the clock frequency.
- Set the jitter frequency on signal generator #2 to the frequency f_{jitter} at which you want to inject the sinusoidal jitter.
- Adjust the FM amplitude level V_{rms} on generator #2, and the FM modulation sensitivity S on generator #1. Measure the jitter amplitude A_{pp} on the oscilloscope or on the spectrum analyzer until the desired jitter amplitude is created. The result is a set of values for V_{rms}, S and A_{pp}.

As a result, a range of amplitude values A_{pp} can be determined as a function of f_{CLK}, f_{jitter}, S and V_{rms}. These results can then be used for jitter injection measurements.

Jitter Generation Example

The jitter amplitude of a clock signal was measured for jitter frequencies of 500 kHz, 1 MHz, 4 MHz and 10 MHz using the time-domain and frequency-domain methods described above. The clock frequency was set at 28 GHz. Figure 8 summarizes the results by showing the measured jitter amplitude of the clock signal in UI as a function of the normalized FM level. It is convenient to define the normalized FM amplitude level ℓ_{FM} as follows

$$\ell_{FM} = \frac{V_{rms} S}{f_{jitter}} \ , \tag{5}$$

where

- V_{rms} is the rms voltage level of the FM signal at the signal generator #2 in Volts
- f_{jitter} is the frequency of the FM signal at the signal generator #2 in MHz
- S is the sensitivity of the FM modulation at the signal generator #1 in MHz/V. In the case of the Anritsu 68197C, the sensitivity is adjustable.

The linear fit shown in Figure 8 is determined empirically and is given by

$$A_{pp} = 0.45 \ell_{FM} \ . \tag{6}$$

Note that this relation is only valid in a certain jitter frequency range and depends on the specific set of instruments.

By assuming that the linear relation is valid, Equations (5) and (6) may be used to derive the necessary FM signal generator settings for a desired jitter amplitude and frequency at a clock frequency of 28 GHz. For example, if a jitter injection of 1.5 UI at f_{jitter} = 1 MHz is required, the normalized FM level is obtained ℓ_{FM} = 3.3. For a sensitivity of S = 20 MHz/V, the signal generator #2 is set to an absolute rms level of

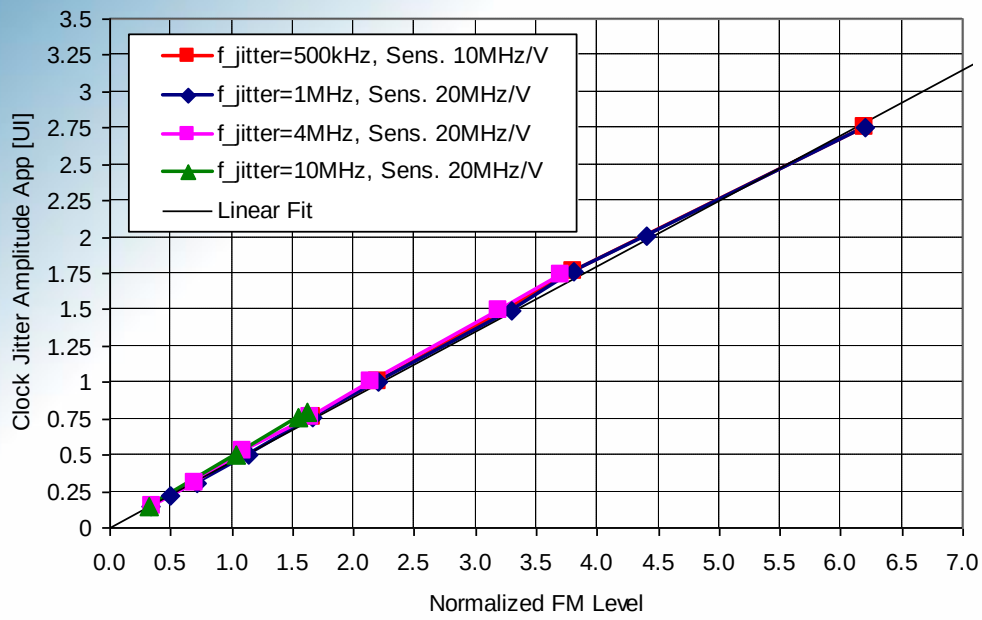


Figure 8: Jitter amplitude imposed on a 28 GHz clock signal versus the normalized FM level obtained using the presented jitter injection setup for a range of jitter frequencies.

$V_{rms} = f_{jitter} \times \ell_{FM} / S$ = 165 mV. Note that the validity of Equation (6) depends on the clock frequency and the jitter frequency range. It should be calibrated in the range of interest.

The measurements show that the largest achievable modulation index and, hence, jitter amplitude and frequency are limited by the FM modulation bandwidth of the Anritsu signal generator. With increasing jitter frequency the maximum achievable jitter amplitude decreases due to the signal generator's FM deviation limit. The Anritsu 68197C will either give a locking error or a warning to reduce the input voltage level. The frequency deviation limit can be taken from the signal generator's data sheet or may be determined experimentally.

By combining the information from the data sheet of the signal generator and the measurement results, Figure 9 shows the achievable jitter amplitudes versus frequency using the Anritsu 68197C. At a number of selected jitter values, the correct jitter transfer was verified on both the SHF 12103 A and SHF 12104 A data output.

Further, it was tested if the generated jittered data signals are still error-free. For this experiment, the jittered clock signal was used to clock both the pattern generator and the error analyzer. This ensures that the error analyzer is not affected by the jitter. Error-free operation was successfully verified for the measured points shown in the graph in Figure 9.

For comparison, the jitter standards requirements from Figure 1 are added. Clearly, the requirements at lower frequencies are easily met. However, jitter frequencies above 10 MHz exceed the FM modulation bandwidth of the Anritsu 68197C signal generator.

Jitter Injection up to 1 GHz Using SHF 78210 / 78120

In order to use the jitter injection capabilities of the SHF 12103 A or SHF 12104 A up to 1 GHz, we developed the SHF 78210 / 78120 Synthesized Clock Generator series which feature a modulation input with 1 GHz bandwidth to apply arbitrary jitter with up to 60 ps amplitude to the clock signal. The setup is shown in Figure 10. The jittered clock signal is fed into the BPG clock input.

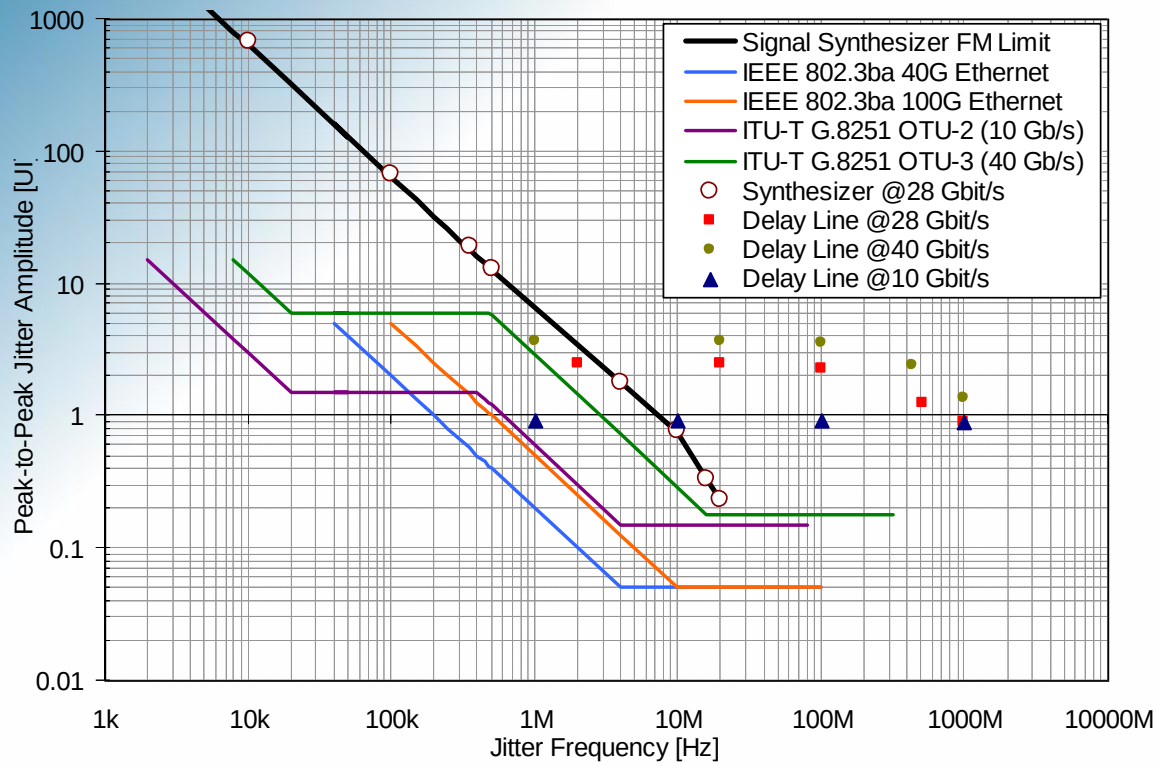


Figure 9: Maximum achievable sinusoidal jitter amplitude versus jitter frequency using the SHF 12103 A or SHF 12104 A BPG.

By analyzing the eye diagram and the spectrum, it was confirmed that the jittered data signal contains the same amount of jitter as the clock input under all specified operating conditions. Additionally, error-free pattern generation was successfully verified for the delay line jitter injection technique for the measured points shown in Figure 9. This confirms that both the 12103 A and the 12104 A are jitter-transparent in the sense that they transfer the clock jitter unaltered to the generated data signal.

Note that the modulation port of the SHF 78210 / 78120 not only supports sinusoidal but arbitrary jitter types such as random jitter, rectangular (peak-to-peak) jitter or bounded uncorrelated jitter. Simply replace the signal generator #2 by an arbitrary waveform generator (AWG). Setting the AWG to NOISE will produce random jitter, for example. Further details can be found in the datasheets of the SHF 78210 / SHF 78120 at www.shf.de.

The SHF 78210 operates as a module in existing SHF BERT mainframes and the SHF 78120 provides the same functionality in a standalone bench-top device. For further information, please contact our sales team:

SHF Communication Technologies AG
Wilhelm-von-Siemens-Str. 23 D
12277 Berlin, Germany

phone: +49 30 772051-0
fax: +49 30 7531078
email: sales@shf.de.
web: www.shf.de

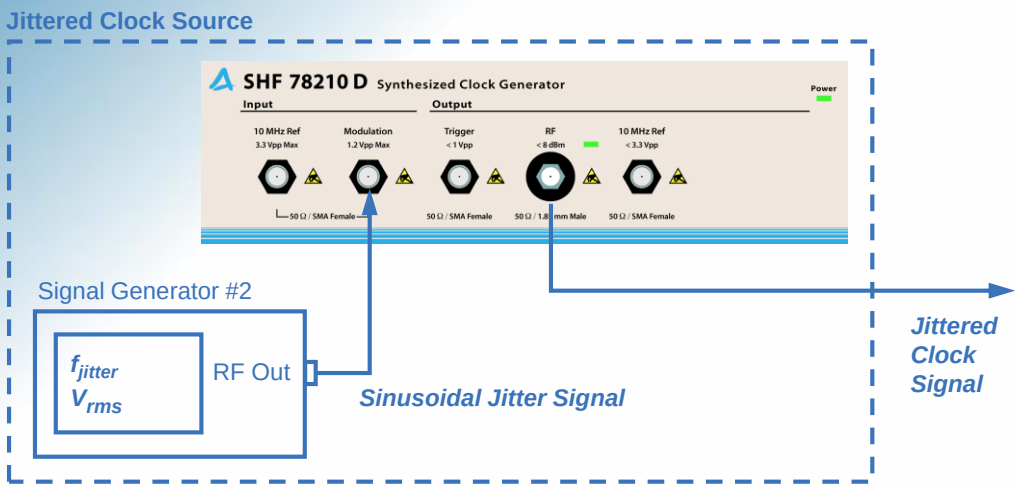


Figure 10: Jittered clock source using SHF 78210 D.

Conclusion

Jitter tolerance test setups were presented using the SHF 12103 A or SHF 12104 A, the SHF 78210 or 78120 clock generators and the FM function of an external signal generator. It was demonstrated that the SHF pattern generators are jitter transparent, i.e. they correctly transfer the jitter from the clock signal to the data output signal over the entire considered jitter frequency and amplitude range. The setups enable sinusoidal jitter injection tests as required by many telecommunication standards such as 100G Ethernet and 40 GBit/s OTN. Several hundreds UI of jitter amplitude can be generated at lower jitter frequencies in the 10 kHz range using the FM technique. The maximum sinusoidal jitter frequency was limited to 10 MHz due to the signal generator's FM bandwidth. To overcome this limit and for injection of other jitter types, SHF offers the 78210 / 78120 Synthesized Clock Generator which feature a Modulation port with 1 GHz bandwidth and up to 60 ps jitter amplitude. The proposed jitter injection setups meet the standards requirements with sufficient margin.

References

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